

1 key Touch Pad Detector IC

Outline

- The TTP233D TonTouch™ is a touch pad detector IC which offers 1 touch key. The device built-in regulator for touch sensor. Stable sensing method can cover diversity conditions. The touching detection IC is designed for replacing traditional direct button key with diverse pad size. Low power consumption and wide operating voltage are the contact key features for DC or AC application.

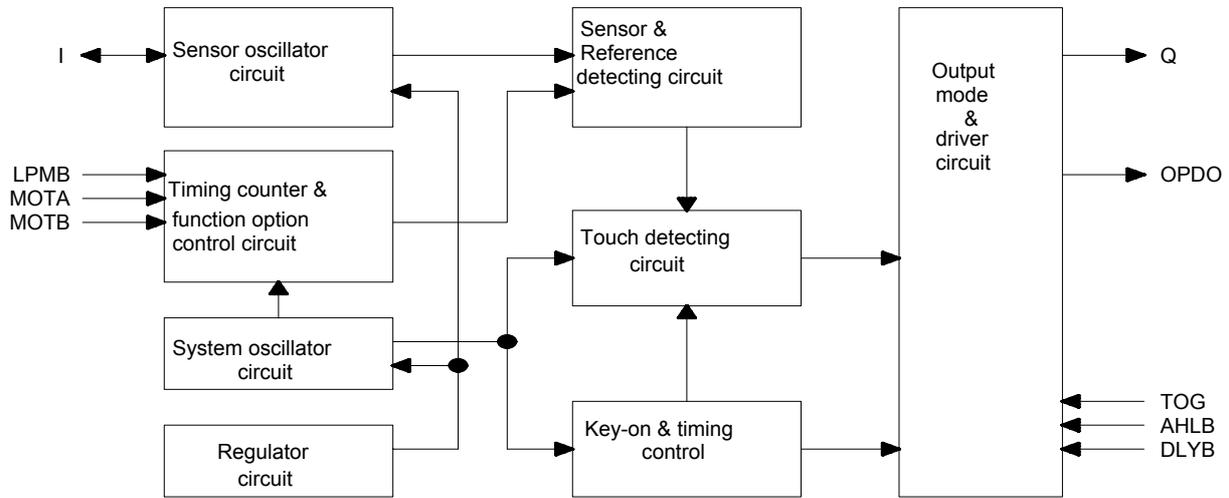
Characteristic

- Operating voltage 2.4V ~ 5.5V
- Built-in regulator for touch sensor
- Built-in low voltage reset (LVR) function
- Operating current, @VDD=3V no load
At low power mode typical 2.5uA, maximum 5uA
At fast mode typical 5uA, maximum 10uA
- The response time max about 60mS at fast mode, 220mS at low power mode @VDD=3V
- Sensitivity can adjust by the capacitance (1~50pF) outside
- Stable touching detection of human body for replacing traditional direct switch key
- Provides Fast mode and Low Power mode selection by pad option (LPMB pin)
- Provides normal mode and delay-off mode selection by pad option (DLYB pin)
- Provides output type selection by pad option (TOG pin)
Direct output or toggle output selection on normal mode
Delay-off mode-1 or mode-2 selection on delay-off mode
- Provides maximum on time and delay-off time selection by pad option (MOTA, MOTB pin)
- Q pin is CMOS output can be selected active high or active low by pad option (AHLB pin)
OPDO that has no diode protection, active low
- After power-on have about 0.5sec stable-time, during the time do not touch the key pad, and the function is disabled
- Auto calibration for life
The re-calibration period is about 1 sec within 8 sec after power-on. When key has been touched within 8 sec or key has not been touched more than 8 sec after power-on, then the re-calibration period change to 4 sec

Applications

- Wide consumer products
- Button key replacement

Block diagram



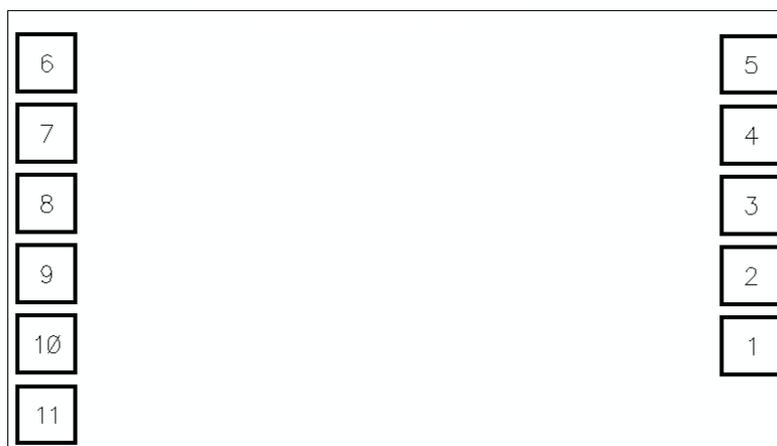
Pin Description

Pad NO	Pad Name	Type	Pad Description																				
1	Q	O	CMOS output pin																				
2	OPDO	OD	Open drain output pin active low(have no Diode protective circuit)																				
3	VSS	P	Negative power supply, ground																				
4	LPMB	I-PH	Low power mode selection, 1(Default)=>Fast mode; 0=>Low power mode																				
5	TOG	I-PL	Output type option pin, Normal mode: 0(Default)=>Direct output; 1=>Toggle output Delay-off mode:0(Default)=>delay-off mode-1; 1=>delay-off mode-2																				
6	VDD	P	Positive power supply																				
7	AHLB	I-PL	Output Q active high or low selection, 0(Default)=>Active high; 1=>Active low																				
8	DLYB	I-PH	Selecting delay-off option pin, 1(Default)=>normal mode; 0=>delay-off mode																				
9	MOTB	I-PH	Maximum on time or delay-off mode time selection, 11(Default)																				
10	MOTA	I-PH	<table border="1"> <thead> <tr> <th>MOTB</th> <th>MOTA</th> <th>Normal mode: Maximum on time</th> <th>Delay-off mode</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>1</td> <td>Infinity</td> <td>2sec</td> </tr> <tr> <td>0</td> <td>1</td> <td>16sec</td> <td>80sec</td> </tr> <tr> <td>1</td> <td>0</td> <td>64sec</td> <td>16sec</td> </tr> <tr> <td>0</td> <td>0</td> <td>8sec</td> <td>8sec</td> </tr> </tbody> </table>	MOTB	MOTA	Normal mode: Maximum on time	Delay-off mode	1	1	Infinity	2sec	0	1	16sec	80sec	1	0	64sec	16sec	0	0	8sec	8sec
			MOTB	MOTA	Normal mode: Maximum on time	Delay-off mode																	
			1	1	Infinity	2sec																	
			0	1	16sec	80sec																	
1	0	64sec	16sec																				
0	0	8sec	8sec																				
All time error is $\pm 50\%$																							
11	I	I/O	Input sensor port																				

Pin Type

- I CMOS input only
- O CMOS push-pull output
- I/O CMOS I/O
- P Power/Ground
- I-PH CMOS input and pull-high resistor
- I-PL CMOS input and pull-low resistor
- OD Open drain output, have no Diode protective circuit

Pad's Diagram



CHIP SIZE: 1236um x 740um
 Substrate floating (recommmend) or VSS

Pad's Coordinate

Pad NO.	Pad Name	X	Y
1	Q	520.500	-170.250
2	OPDO	520.500	-65.250
3	VSS	520.500	39.750
4	LPMB	520.500	144.750
5	TOG	520.500	249.750
6	VDD	-520.500	252.500
7	AHLB	-520.500	147.500
8	DLYB	-520.500	42.500
9	MOTB	-520.500	-62.500
10	MOTA	-520.500	-167.500
11	I	-520.500	-272.500

Electrical Characteristics

- Absolute maximum ratings**

Parameter	Symbol	Conditions	Rating	Unit
Operating Temperature	T _{OP}	—	-40~+85	°C
Storage Temperature	T _{STG}	—	-50~+125	°C
Supply Voltage	VDD	Ta=25°C	VSS-0.3~VSS+5.5	V
Input Voltage	V _{IN}	Ta=25°C	VSS-0.3~VDD+0.3	V
Human Body Mode	ESD	—	5	KV

Note : VSS symbolizes for system ground

- DC / AC characteristics : (Test condition at room temperature = 25 °C)**

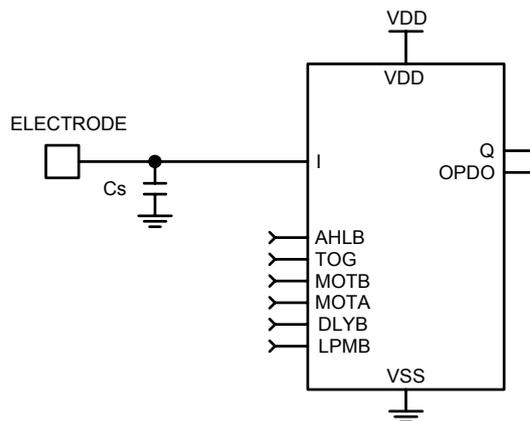
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating Voltage	VDD		2.4	3	5.5	V
Internal Regulator Output	VREG		2.2	2.3	2.4	V
Operating Current	I _{OPL}	VDD=3V, At low power mode		2.5	5	uA
	I _{OFF}	VDD=3V, At fast mode		5.0	10	uA
Input Ports	V _{IL}	Input Low Voltage	0		0.2	VDD
Input Ports	V _{IH}	Input High Voltage	0.8		1.0	VDD
Output Port Sink Current	I _{OL}	VDD=3V, V _{OL} =0.6V		8		mA
Output Port Source Current	I _{OH}	VDD=3V, V _{OH} =2.4V		-4		mA
Input Pin Pull-high Resistor	R _{PH}	VDD=3V (LPMB, MOTA, MOTB, DLYB)		30K		ohm
Input Pin Pull-low Resistor	R _{PL}	VDD=3V (TOG, AHLB)		25K		ohm
Output Response Time	T _R	VDD=3V、 At fast mode			60	mS
		VDD=3V、 At low power mode			220	

Function Description

I . Sensitivity adjustment

The total loading of electrode size and capacitance of connecting line on PCB can affect the sensitivity. So the sensitivity adjustment must according to the practical application on PCB. The TTP233D offers some methods for adjusting the sensitivity outside.

1. by the electrode size
Under other conditions are fixed. Using a larger electrode size can increase sensitivity. Otherwise it can decrease sensitivity. But the electrode size must use in the effective scope.
2. by the panel thickness
Under other conditions are fixed. Using a thinner panel can increase sensitivity. Otherwise it can decrease sensitivity. But the panel thickness must be below the maximum value.
3. by the value of Cs (please see the down figure)
Under other conditions are fixed. When do not use the Cs to VSS, the sensitivity is most sensitive. When adding the value of Cs will reduce sensitivity in the useful range ($1 \leq Cs \leq 50pF$) .

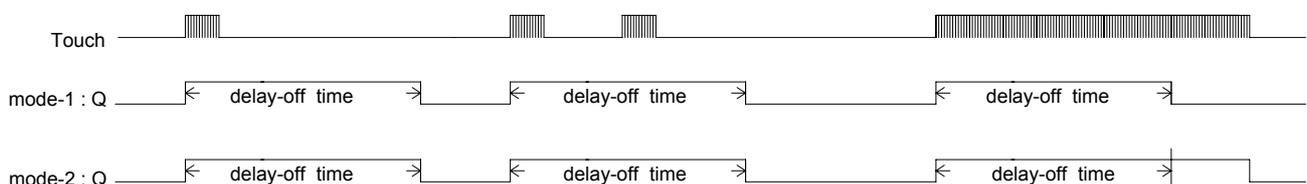


II . Output mode (By TOG 、 AHLB 、 DLYB pad option)

- TOG pad : Direct output or toggle output selection on normal mode.
Delay-off mode-1 or mode-2 selection on delay-off mode.
- AHLB pad : Output Q active high or active low selection.
- DLYB option pad : Normal mode or Delay-off mode selection.

Delay-off there are mode-1 and mode-2 :

- mode -1 : When key touch action be detected, no matter the key touch action time is more than or less than delay-off time, the output time is fixed to delay-off time.
- mode -2 : When key touch action be detected, if the key touch action time is less than delay-off time, then the output time is delay-off time, if the key touch action time is more than delay-off time, then the output time is the key touch action time.

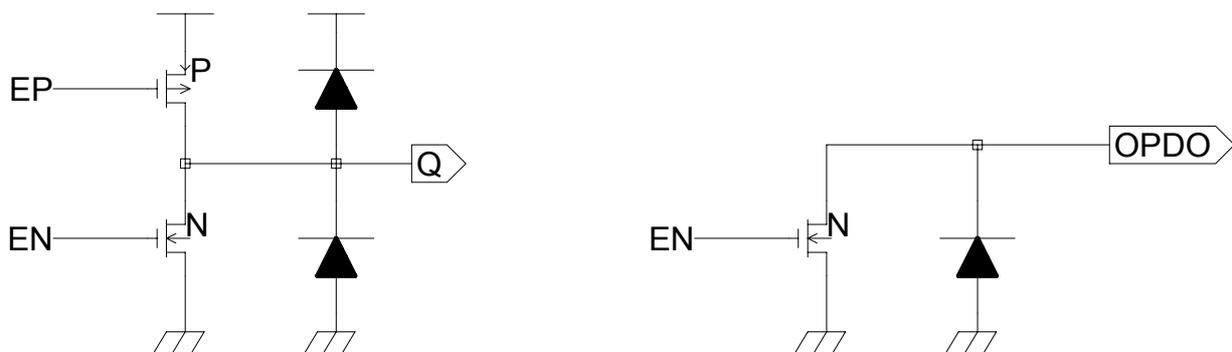


Pad Q (CMOS output) option features :

DLYB	TOG	AHLB	Pad Q option features
1	0	0	Normal mode, Direct output, CMOS active high
1	0	1	Normal mode, Direct output, CMOS active low
1	1	0	Normal mode, Toggle output, power on state = 0
1	1	1	Normal mode, Toggle output, power on state = 1
0	0	0	Delay off mode -1, active high
0	0	1	Delay off mode -1, active low
0	1	0	Delay off mode -2, active high
0	1	1	Delay off mode -2, active low

Pad OPDO (Open drain active low output, has no diode protective circuit) option features :

DLYB	TOG	Pad OPDO option features
1	0	Normal mode, Direct output, open drain active low, power on state high-Z
1	1	Normal mode, Toggle output, open drain active low, power on state high-Z
0	0	Delay off mode -1, open drain active low, power on state high -Z
0	1	Delay off mode -2, open drain active low, power on state high -Z



III. Maximum key on duration time or delay-off time (By MOTB 、 MOTA pad option)

1. On Normal mode, if some objects cover in the sense pad, and causing the change quantity enough to be detected. To prevent this, the TTP233D sets a timer to monitor the detection. The timer is the maximum on duration time. It is set by MOTB, MOTA pads, please to see below table. When the detection is over the timer, the system will return to the power-on initial state, and the output becomes inactive until the next detection.
2. On Delay-off mode, the MOTB, MOTA pads can select delay-off time, such as below table. All time error is $\pm 50\%$.

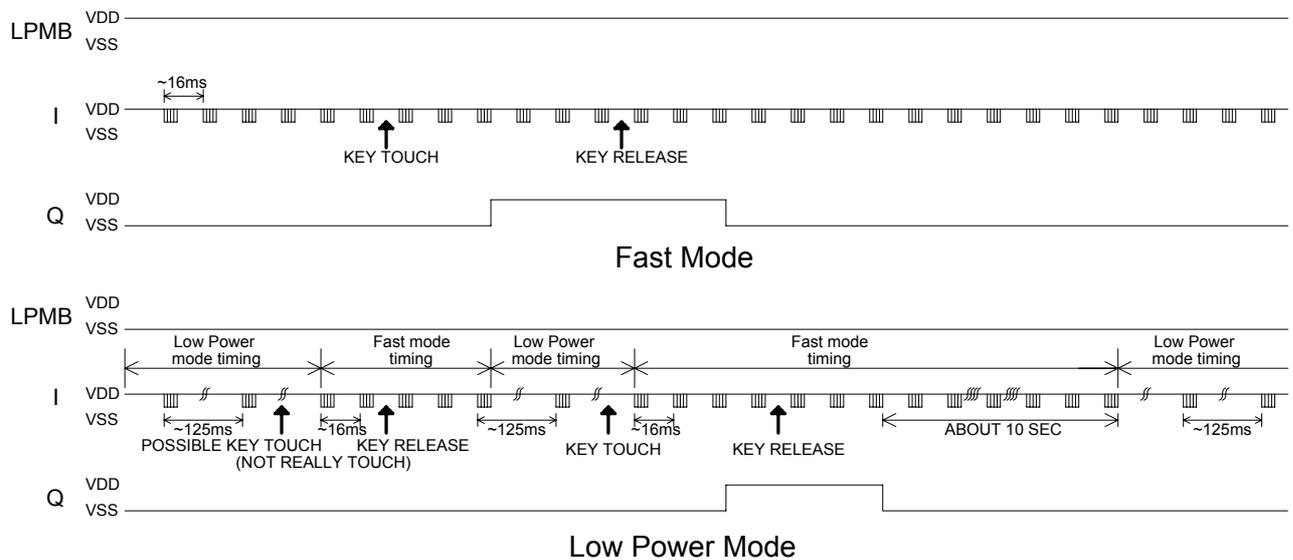
DLYB	MOTB	MOTA	Option features
DLYB=1 Normal mode	1	1	Infinite (Disable maximum on time)
	0	1	Maximum on time 16 sec
	1	0	Maximum on time 64 sec
	0	0	Maximum on time 8 sec
DLYB=0 Delay-off mode	1	1	Delay-off time : 2 sec
	0	1	Delay-off time : 80 sec
	1	0	Delay-off time : 16 sec
	0	0	Delay-off time : 8 sec

IV. Fast and Low power mode selection (By LPMB pad option)

The TTP233D has Fast mode and Low Power mode to be selected. It depends on the state of LPMB pad. When the LPMB pin is opened or connected to VDD, the TTP233D runs in Fast mode. When the LPMB pin is connected to VSS, the TTP233D runs in Low Power mode.

In the Fast mode response time is faster, but the current consumption will be increased. In the Low Power mode it will be saving power, but will be slowing response time for first touch. When it awaked in fast mode, the response time is the same the fast mode. In this mode when detecting key touch, it will switch to Fast mode. Until the key touch is released and will keep a time about 10 sec. Then it returns to Low Power mode.

The states and timing of two modes please see below figure.



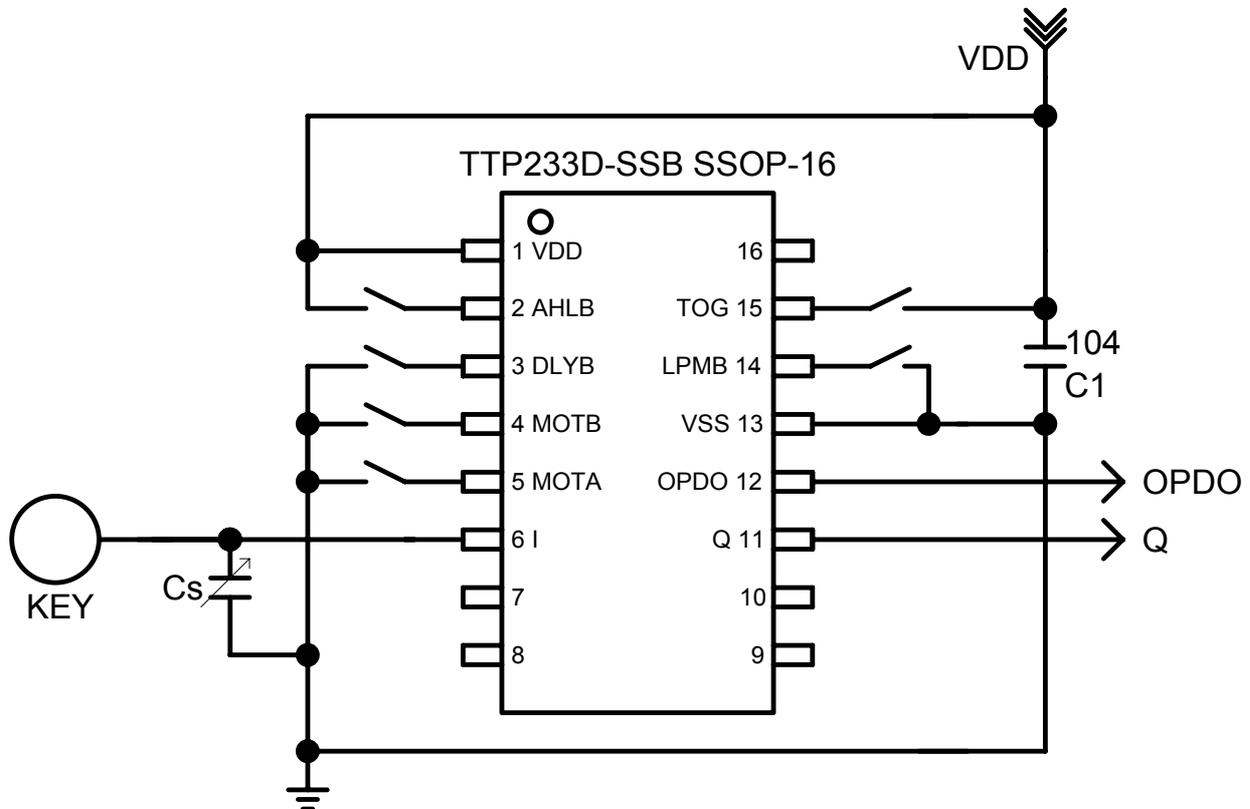
LPMB	Option features
1	Fast mode
0	Low Power mode

V. Option pin

For power saving concern and package bonding option consideration, all the feature option pins with latch type design and initial states are 0 or 1 as power on. If those pins are forced to VDD or VSS, the states will be changed to 1 or 0 without any current leakage to conflict the power saving issue.

Feature option pins	Initial state by Power on
AHLB	0
TOG	0
LPMB	1
MOTB	1
MOTA	1
DLYB	1

Application circuit

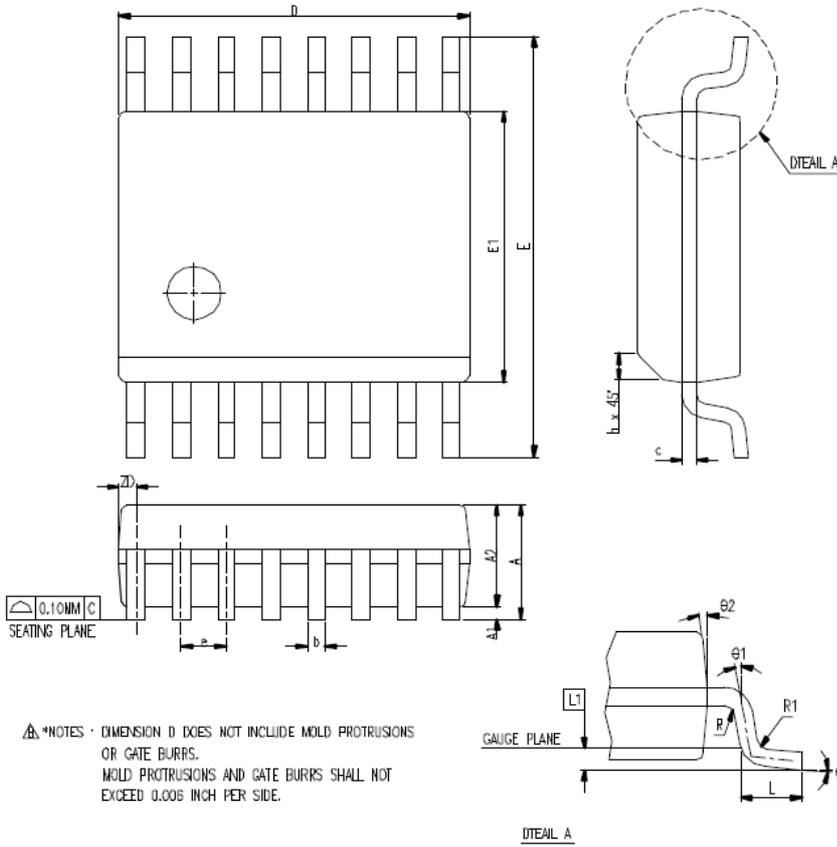


P.S. :

1. On PCB, the length of lines from touch pad to IC pin shorter is better. And the lines do not parallel and cross with other lines.
2. The power supply must be stable. If the supply voltage drift or shift quickly, maybe causing sensitivity anomalies or false detections.
3. The material of panel covering on the PCB can not include the metal or the electric element. The paints on the surfaces are the same.
4. The C1 capacitor must be used between VDD and VSS; and should be routed with very short tracks to the device's VDD and VSS pins (TTP233D).
5. The capacitance Cs can be used to adjust the sensitivity. The value of Cs use smaller, then the sensitivity will be better. The sensitivity adjustment must according to the practical application on PCB. The range of Cs value are 1~50pF.
6. The sensitivity adjustment capacitors (Cs) must use smaller temperature coefficient and more stable capacitors. Such are X7R, NPO for example. So for touch application, recommend to use NPO capacitor, for reducing that the temperature varies to affect sensitivity.

Package outline

Package Type: SSOP-16



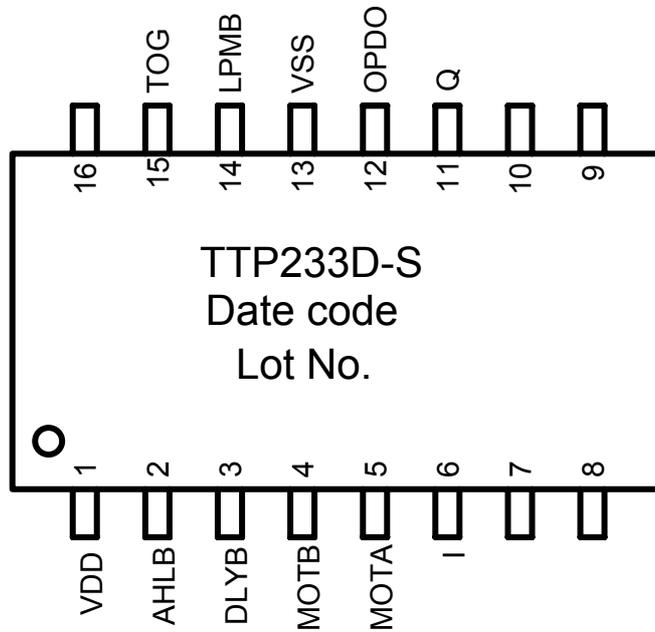
SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.35	1.63	1.75	0.053	0.064	0.069
A1	0.10	0.15	0.25	0.004	0.006	0.010
A2			1.50			0.059
b	0.20		0.30	0.008		0.012
c	0.18		0.25	0.007		0.010
e	0.635 BASIC			0.025 BASIC		
D	4.80	4.90	5.00	0.189	0.193	0.197
E	5.79	5.99	6.20	0.228	0.236	0.244
E1	3.81	3.91	3.99	0.150	0.154	0.157
L	0.41	0.635	1.27	0.016	0.025	0.050
h	0.25		0.50	0.010		0.020
L1	0.254 BASIC			0.010 BASIC		
ZD	0.229 REF			0.009 REF		
R1	0.20		0.33	0.008		0.013
R	0.20			0.008		
θ	0°		8°	0°		8°
θ1	0°			0°		
θ2	5°	10°	15°	5°	10°	15°
JEDEC	MO-137 (AB)					

△A: *NOTES - DIMENSION D DOES NOT INCLUDE MOLD PROTRUSIONS OR GATE BURRS. MOLD PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.005 INCH PER SIDE.

Package configuration

TTP233D-SSB

Package Type SSOP-16



Ordering Information

TTP233D

Package Type	Chip Type	Wafer Type
TTP233D-XXX	TCP233D	TDP233D