# ADD1021 Datasheet

Doc Rev 1.04 Datasheet — 25-May-2010

## Document information

| Info | Content |
|---|---|
| Author | J.G. |
| Keywords | 1021, Datasheet |
| Abstract | |

## Revision History

| Revision | Date | Description | Author |
|---|---|---|---|
| 1.02 | 2010-03-29 | --- | J.G. |
| 1.03 | 2010-04-08 | Updated example circuit | J.G. |
| 1.04 | 2010-05-25 | Max output current values updated | J.G. |
| | | | |
| | | | |
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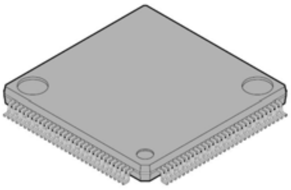
# Contents

# 1. General Description

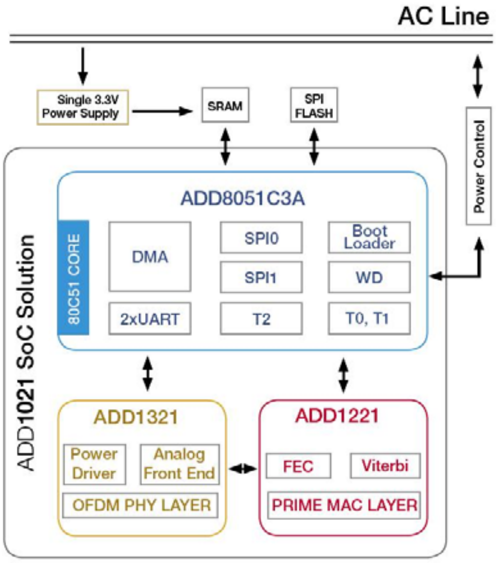
The ADD1021 is a Power Line Communications System on Chip, which implements a full PRIME compliant PLC modem. It includes an enhanced 8051 microcontroller (IP core ADD8051C3A), a Medium Access Controller (MAC) (IP core ADD1221) and a Modem circuit (IP core 1321) for power line medium using OFDM modulation compatible with PRIME specifications.

ADD1021 is oriented to high performance & robust AMR systems. The SoC is designed to be used by meter manufacturers to provide a low cost and compact solution for AMR & AMM systems using narrow band power line communications.

This device has been developed to reduce CPU computational load in PLC systems running PRIME protocols. ADD1021 includes all necessary resources to be used as main controller in metering applications, and allows an external device to comunicate according to PLC PRIME specifications.



120-pin plastic LQFP
(14 x 14mm)



**Features:**

- Power Line Carrier Modem for 50 and 60Hz mains
- 97-carriers OFDM PRIME compliant
- Baudrate: 21400 to 128600 bps
- Differential BPSK, QPSK, 8-PSK PRIME compliant modulations
- Viterbi decoding and CRC PRIME compliant
- Enhanced 8051 core, Average speedup of 5 times
- 32Kbytes On-Chip SRAM
- Up to 256Kbytes external SRAM
- AES encryption PRIME compliant
- Automatic Gain Control and signal amplitude tracking
- Embedded On-chip DMA’s
- Auto Boot-loading program from Serial Flash
- Code encryption in bootloading
- In-circuit Serial Flash Programming
- Programmable watchdog
- 2xUART
- Buffered SPI to external metering IC
- Power Supply 3.3v
- Pb-Free and RoHS compliant
- Ambient Temperature Range: -40ºC to +85ºC

**MARKING DIAGRAM**

***ADD*** =*Customer Logo*
***ADD1021AQF120*** =*Customer Part number*
***OOOOO*** =*Country of Origin*
***YYWW*** =*Year/week code*
***TTT*** =*Control Code*
***LL*** =*Lead Free Code*

***Ordering Code :*** ***ADD1021AQF120 Pb-Free***

## 1.1 Block Diagram

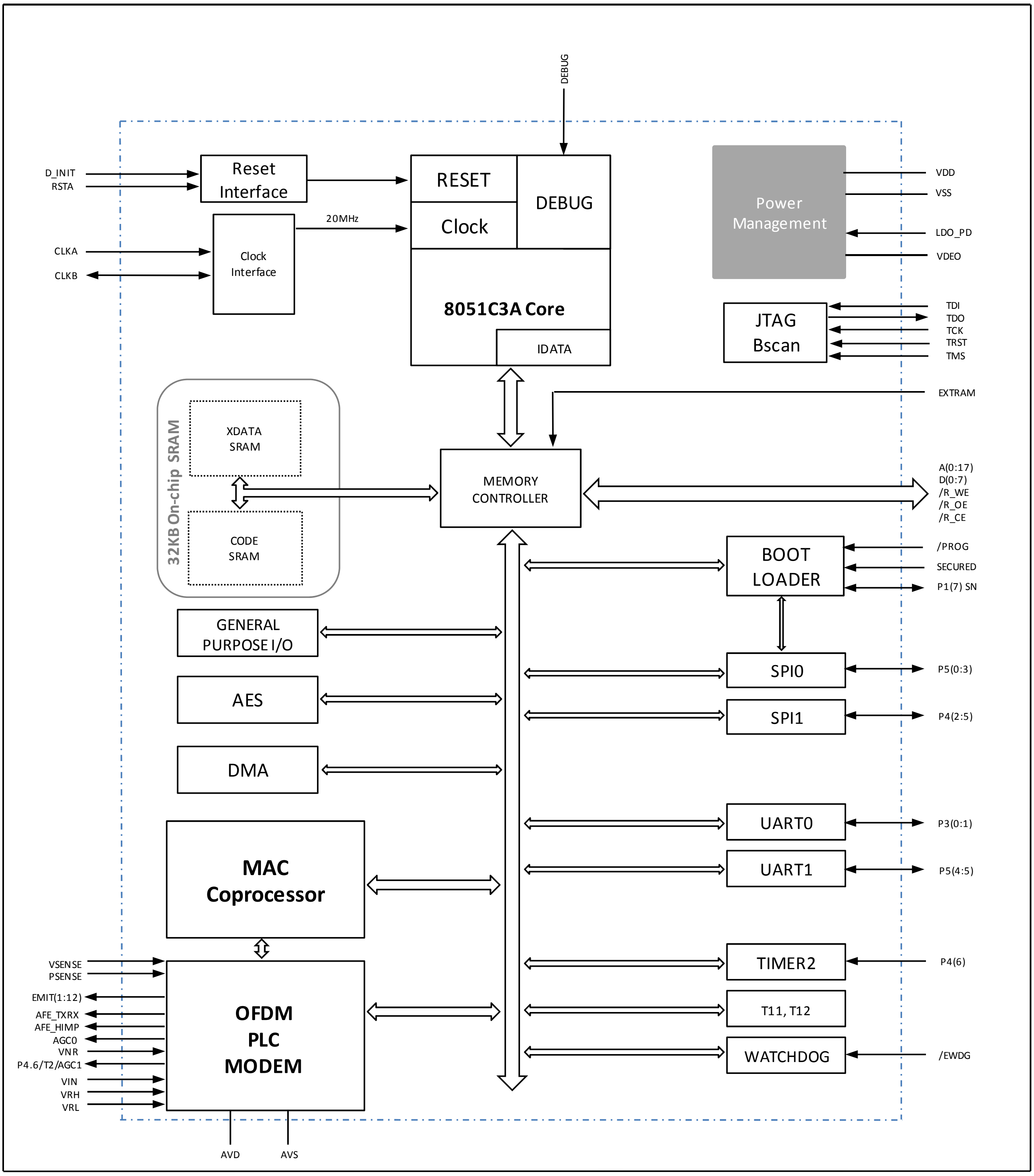


**Figure 1. ADD1021 Block Diagram**

## 1.2 Pin Assignment

The following figure illustrates the pinout of the ADD1021 LQFP120 package:

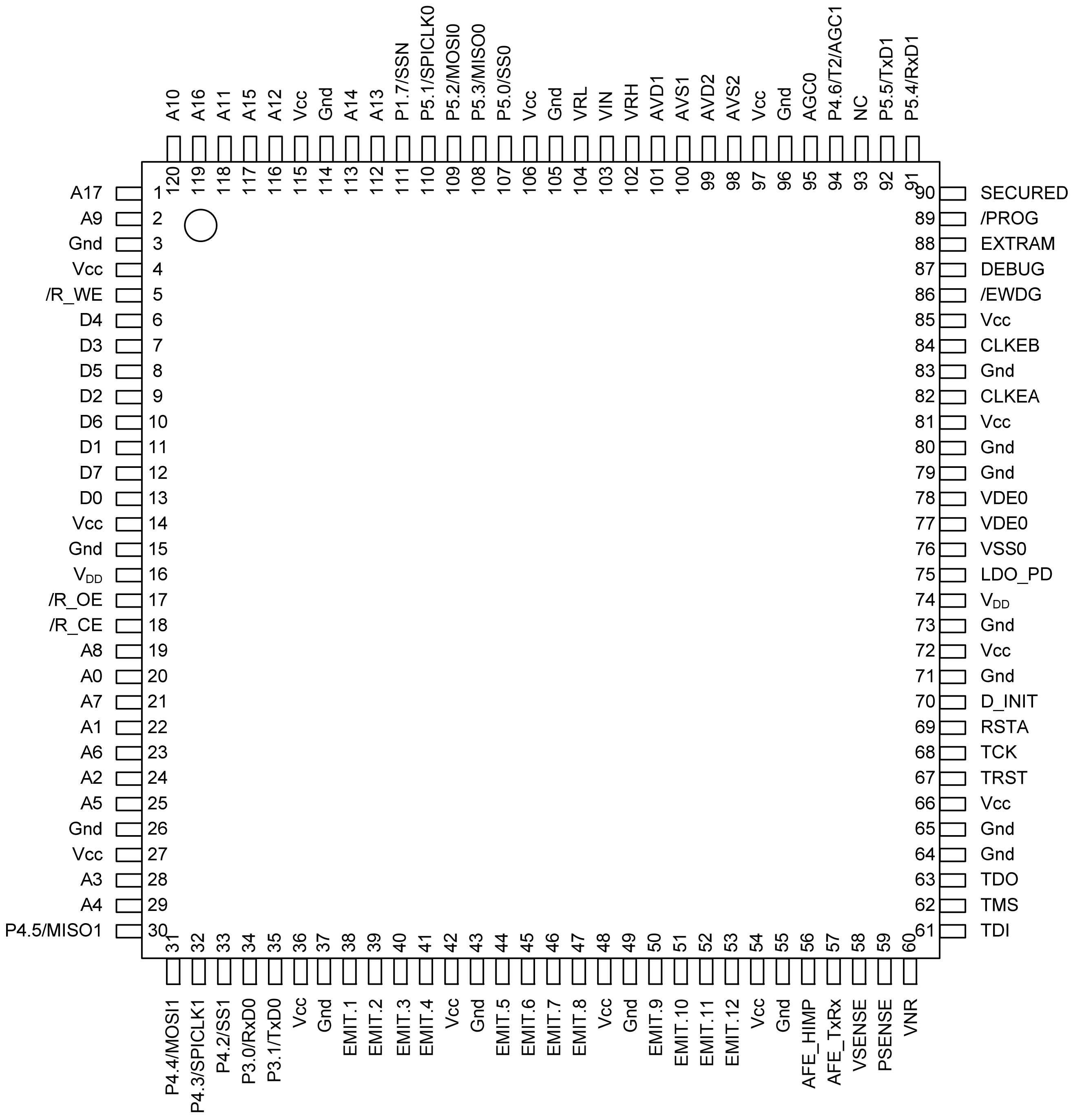


**Figure 2. LQFP pin assignment**

| PinNo | Pin Name | I/O | I(mA) | Res | HY | Pin Description |
|---|---|---|---|---|---|---|
| 1 | A17 | O | ±5 | - | - | Data/Prog. Address bus |
| 2 | A9 | O | ±5 | - | - | Data/Prog. Address bus |
| 3 | GND | P | - | - | - | Ground |
| 4 | VCC | P | - | - | - | 3.3v power Supply |
| 5 | /R_WE | O | ±5 | PU | - | External Memory Write Enable Signal |
| 6 | D4 | I/O | ±5 | - | - | External Memory Data bus |
| 7 | D3 | I/O | ±5 | - | - | External Memory Data bus |
| 8 | D5 | I/O | ±5 | - | - | External Memory Data bus |
| 9 | D2 | I/O | ±5 | - | - | External Memory Data bus |
| 10 | D6 | I/O | ±5 | - | - | External Memory Data bus |
| 11 | D1 | I/O | ±5 | - | - | External Memory Data bus |
| 12 | D7 | I/O | ±5 | - | - | External Memory Data bus |
| 13 | D0 | I/O | ±5 | - | - | External Memory Data bus |
| 14 | VCC | P | - | - | - | 3.3v Power Supply |
| 15 | GND | P | - | - | - | Ground |
| 16 | VDD | P | - | - | - | LDO power output. A capacitor in the range 0.1μF-10μF must be connected here |
| 17 | /R_OE | O | ±5 | - | - | External Memory Output Enable Signal |
| 18 | /R_CE | O | ±5 | - | - | External Memory Chip Enable Signal |
| 19 | A8 | O | ±5 | - | - | External Memory Data/Prog. Address bus |
| 20 | A0 | O | ±5 | - | - | External Memory Data/Prog. Address bus |
| 21 | A7 | O | ±5 | - | - | External Memory Data/Prog. Address bus |
| 22 | A1 | O | ±5 | - | - | External Memory Data/Prog. Address bus |
| 23 | A6 | O | ±5 | - | - | External Memory Data/Prog. Address bus |
| 24 | A2 | O | ±5 | - | - | External Memory Data/Prog. Address bus |
| 25 | A5 | O | ±5 | - | - | External Memory Data/Prog. Address bus |
| 26 | GND | P | - | - | - | Ground |
| 27 | VCC | P | - | - | - | 3.3v Power Supply |
| 28 | A3 | O | ±5 | - | - | External Memory Data/Prog. Address bus |
| 29 | A4 | O | ±5 | - | - | External Memory Data/Prog. Address bus |
| 30 | P4.5/MISO1 | I/O | ±5 | PU | - | P4.5 / MISO SPI1 Master In - Slave Out data |
| 31 | P4.4/MOSI1 | I/O | ±5 | PU | - | P4.4 / MOSI SPI1 Master Out - Slave In data |
| 32 | P4.3/SPICLK1 | I/O | ±5 | PU | - | P4.3 / SPICLK SPI1 Clock input/output |
| 33 | P4.2/SS1 | I/O | ±5 | PU | - | P4.2 / SS SPI1 Slave Select input |
| 34 | P3.0/RxD0 | I/O | ±5 | PU | - | P3.0 / RxD Serial Port 0 input |
| 35 | P3.1/TxD0 | I/O | ±5 | PU | - | P3.1 / TxD Serial Port 0 output |
| 36 | VCC | P | - | - | - | 3.3v Power Supply |
| 37 | GND | P | - | - | - | Ground |
| 38 | EMIT.1 | O | ±X | - | - | PLC Transmission port 1 |
| 39 | EMIT.2 | O | ±X | - | - | PLC Transmission port 2 |
| 40 | EMIT.3 | O | ±X | - | - | PLC Transmission port 3 |
| 41 | EMIT.4 | O | ±X | - | - | PLC Transmission port 4 |
| 42 | VCC | P | - | - | - | 3.3v Power Supply |
| 43 | GND | P | - | - | - | Ground |

| PinNo | Pin Name | I/O | I(mA) | Res | HY | Pin Description |
|---|---|---|---|---|---|---|
| 44 | EMIT.5 | O | ±X | - | - | PLC Transmission port 5 |
| 45 | EMIT.6 | O | ±X | - | - | PLC Transmission port 6 |
| 46 | EMIT.7 | O | ±X | - | - | PLC Transmission port 7 |
| 47 | EMIT.8 | O | ±X | - | - | PLC Transmission port 8 |
| 48 | VCC | P | - | - | - | 3.3v Power Supply |
| 49 | GND | P | - | - | - | Ground |
| 50 | EMIT.9 | O | ±X | - | - | PLC Transmission port 9 |
| 51 | EMIT.10 | O | ±X | - | - | PLC Transmission port 10 |
| 52 | EMIT.11 | O | ±X | - | - | PLC Transmission port 11 |
| 53 | EMIT.12 | O | ±X | - | - | PLC Transmission port 12 |
| 54 | VCC | P | - | - | - | 3.3v Power Supply |
| 55 | GND | P | - | - | - | Ground |
| 56 | AFE_HIMP | O | ±10 | - | - | Analog Front End impedance control signal |
| 57 | AFE_TXRX | O | ±10 | - | - | Analog Front End Transmission/Reception control signal |
| 58 | VSENSE | I | ±5 | - | Y | Voltage Amplitude Tracking to avoid power supply malfunction |
| 59 | PSENSE | I | ±5 | - | Y | Power Amplitude Tracking to avoid power supply malfunction |
| 60 | VNR | I | ±5 | - | Y | Zero Crossing Detection Signal |
| 61 | TDI | I | ±5 | PU | - | JTAG Test Data In |
| 62 | TMS | I | ±5 | PU | - | JTAG Test Mode Select |
| 63 | TDO | O | ±5 | - | - | JTAG Test Data Out |
| 64 | GND | P | - | - | - | Ground(*) |
| 65 | GND | P | - | - | - | Ground |
| 66 | VCC | P | - | - | - | 3.3v Power Supply |
| 67 | TRST | I | ±5 | PU | - | JTAG Test Reset |
| 68 | TCK | I | ±5 | - | - | JTAG Test Clock |
| 69 | RSTA | I | ±5 | PD | Y | Asynchronous Reset |
| 70 | D_INIT | I | ±5 | PD | Y | Initialization Signal |
| 71 | GND | P | - | - | - | Ground(*) |
| 72 | VCC | P | - | - | - | 3.3v Power Supply |
| 73 | GND | P | - | - | - | Ground |
| 74 | VDD | P | - | - | - | LDO power output. A capacitor in the range 0.1μF-10μF must be connected here |
| 75 | LDO_PD | I |  |  |  | LDO Power down |
| 76 | VSS0 | P | - | - | - | LDO ground |
| 77 | VDE0 | P | - | - | - | LDO power input |
| 78 | VDE0 | P | - | - | - | LDO power input |
| 79 | GND | P | - | - | - | Ground |
| 80 | GND | P | - | - | - | Ground |
| 81 | VCC | P | - | - | - | 3.3v Power Supply |
| 82 | CLKEA | I | - | - | - | External clock reference. The user may connect CLKEA to one terminal of a crystal oscillator or tie CLKEA to ground if a compatible oscillator is being used |
| 83 | GND | P | - | - | - | Ground |
| 84 | CLKEB | I/O | - | - | - | External clock reference. The user may connect CLKEB to a compatible oscillator or to one terminal of a crystal oscillator |

| PinNo | Pin Name | I/O | I(mA) | Res | HY | Pin Description |
|---|---|---|---|---|---|---|
| 85 | VCC | P | - | - | - | 3.3v Power Supply |
| 86 | /EWDG | I | ±5 | PD | Y | Watchdog enable. Active low |
| 87 | DEBUG | I | ±5 | PD | Y | Debug mode enable |
| 88 | EXTRAM | I | ±5 | - | Y | SRAM device selection |
| 89 | /PROG | I | ±5 | PU | Y | SPI Flash Programming pin |
| 90 | SECURED | I | ±5 | PD | Y | Encryption enable |
| 91 | P5.4/RxD1 | I/O | ±5 | PU | - | P5.4 / RxD Serial Port 1 input |
| 92 | P5.5/TxD1 | I/O | ±5 | PU | - | P5.5 / TxD Serial Port 1 output |
| 93 | NC | - | - | - | - | No Connect |
| 94 | P4.6/T2/AGC1 | I/O | ±10 | PU | - | P4.6 / Timer2 interrupt signal / Automatic Gain Control 1 |
| 95 | AGC0 | O | ±10 | - | - | Automatic Gain Control 0 |
| 96 | GND | P | - | - | - | Ground |
| 97 | VCC | P | - | - | - | 3.3v Power Supply |
| 98 | AVS2 | P | - | - | - | Analog Ground 2 |
| 99 | AVD2 | P | - | - | - | 3.3v Analog Power Supply 2 |
| 100 | AVS1 | P | - | - | - | Analog Ground 1 |
| 101 | AVD1 | P | - | - | - | 3.3v Analog Power Supply 1 |
| 102 | VRH | I | (**) | - | - | Analog input High Voltage Reference |
| 103 | VIN | I | (**) | - | - | Direct-Analog input Voltage |
| 104 | VRL | I | (**) | - | - | Analog input Low Voltage Reference |
| 105 | GND | P | - | - | - | Ground |
| 106 | VCC | P | - | - | - | 3.3v Power Supply |
| 107 | P5.0/SS0 | I/O | ±5 | PU | - | P5.0 / SS SPI0 Slave Select input |
| 108 | P5.3/MISO0 | I/O | ±5 | PU | - | P5.3 / MISO SPI0 Master In - Slave Out data |
| 109 | P5.2/MOSI0 | I/O | ±5 | PU | - | P5.2 / MOSI SPI0 Master Out - Slave In data |
| 110 | P5.1/SPICLK0 | I/O | ±5 | PU | - | P5.1 / SPICLK SPI0 Clock input/output |
| 111 | P1.7/SSN | I/O | ±5 | PU | - | Silicon Serial Number (P1.7 must not be used as generic control port since it searches for a Silicon Serial Number device at start-up and could put out undesirable transient values) |
| 112 | A13 | O | ±5 | - | - | External Memory Data/Prog. Address bus |
| 113 | A14 | O | ±5 | - | - | External Memory Data/Prog. Address bus |
| 114 | GND | P | - | - | - | Ground |
| 115 | VCC | P | - | - | - | 3.3v Power Supply |
| 116 | A12 | O | ±5 | - | - | External Memory Data/Prog. Address bus |
| 117 | A15 | O | ±5 | - | - | External Memory Data/Prog. Address bus |
| 118 | A11 | O | ±5 | - | - | External Memory Data/Prog. Address bus |
| 119 | A16 | O | ±5 | - | - | External Memory Data/Prog. Address bus |
| 120 | A10 | O | ±5 | - | - | External Memory Data/Prog. Address bus |

| | | |
|---|---|---|
| **I/O=pin direction:** | **I=input, O=Output, P=Power** | (*) Mandatory to be tied down |
| **I(mA)=nominal current:** | **+=source, -=sink, X=fixed by external resistor** | (**)See application circuit |

**RES=pin pullup/pulldown resistor: PU=pullup, PD=pulldown**

**HY=Input Hysteresis**

**Table 1. ADD1021 pin description**

# 2. Electrical Characteristics

## 2.1 Absolute Maximum Ratings

Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions given in the Recommended Operating Conditions section. Exposure to the Absolute Maximum Conditions for extended periods may affect device reliability.

(VSS = 0 V)

| Parameter | Symbol | Rating | Unit |
|---|---|---|---|
| Supply Voltage | VCC | -0.5 to 4.0 | V |
| Input Voltage | VI | -0.5 to VCC+0.5(≤4.0V) | V |
| Output Voltage | VO | -0.5 to VCC+0.5(<4.0V) | V |
| Storage Temperature | TST | -55 to 125 | ºC |
| Junction Temperature | TJ | -40 to 125 | ºC |
| Output Current(*)1 | IO | ±10(*)2 | mA |

Notes:

(*)1. DC current that continuously flows for 10ms or more, or average DC current.

(*)2. Applies to all the pins except EMIT pins. EMIT pins should be only used according to circuit configurations recommended by ADD.

**ATTENTION Observe ESD Precautions**

Precautions for handling electrostatic sensitive devices should be taken into account to avoid malfunction. Charged devices and circuit boards can discharge without detection.

## 2.2 Recommended Operating Conditions

| Parameter | Symbol | Rating | | | Unit |
|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | |
| Supply Voltage | VCC | 3.00 | 3.30 | 3.60 | V |
| | VDEO | 3.00 | 3.30 | 3.60 | |
| | VDA | 3.00 | 3.30 | 3.60 | |
| Junction Temperature | TJ | -40 | 25 | 125 | ºC |
| Ambient Temperature | TA | -40 | - | 85 | |

## 2.3 DC Characteristics

(VCC=3.3v ± 0.3v , VSS=0v , TJ=-40 to 125°C)

| Parameter | Condition | Symbol | Rating | | | Unit |
|---|---|---|---|---|---|---|
| | | | **Min.** | **Typ.** | **Max.** | |
| Supply Voltage | | VCC | 3.00 | 3.30 | 3.60 | V |
| H-level Input Voltage (3.3v CMOS) | | VIH | 2.0 | - | VCC+0.3 | |
| L-level Input Voltage (3.3v CMOS) | | VIL | -0.3 | - | 0.8 | |
| H-level Output Voltage | 3.3v I/O<br>IOH=-100µA | VOH | VCC-0.2 | - | VCC | |
| L-level Output Voltage | 3.3v I/O<br>IOL=100µA | VOL | 0 | - | 0.2 | |
| H-level Output V-I Characteristics | 3.3v I/O<br>VCC=3.3±0.3 | IOH | Refer to Annex 1 | | | mA |
| L-level Output V-I Characteristics | 3.3v I/O<br>VCC=3.3±0.3 | IOL | Refer to Annex 1 | | | |
| Internal Pull-up Resistor(*)1 | 3.3v I/O | Rpu | 10 | 33 | 80 | kΩ |
| Internal Pull-down Resistor(*)1 | 3.3v I/O | Rpd | 10 | 33 | 80 | kΩ |
| Junction Temperature | | TJ | -40 | - | 125 | °C |

Notes:

(*)1. Only applicable to pins with internal pulling. See related table.

## 2.4 Power Consumption

| Parameter | Condition | Symbol | Rating | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| Power Consumption | TA=25°C, VCC=3.3v | $P_{25}$ | -- | 265 | -- | mW |
| Power Consumption (worst case) | TA=85°C, VCC=3.6v | $P_{85}$ | -- | -- | 370 | -- |

## 2.5 Thermal data

| Parameter | Symbol | LQFP144 | Unit |
|---|---|---|---|
| Thermal resistance junction-ambient steady state | $R_{Theta\text{-}ja}$ | 60 *(1)<br>40 *(2) | ºC/W |

Notes:

1. Mounted on 2-layer PCB.
2. Mounted on 4-layer PCB.

Theta-ja is calculated based on a standard JEDEC defined environment and is not reliable indicator of a device's thermal performance in a non-JEDEC environment. The customer should always perform their own calculations/simulations to ensure that their system's thermal performance is sufficient.

## 2.6 Oscillator

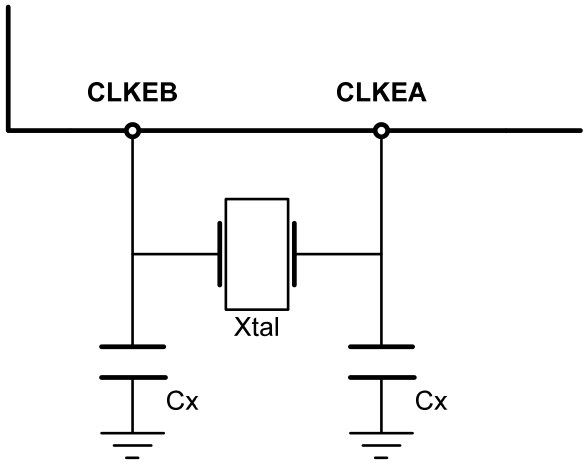


**Figure 3. External Crystal configuration**

| Parameter | Test Condition | Symbol | Rating | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| Crystal Oscillator frequency | fundamental | Xtal | 20 | | | MHz |
| External Oscillator Capacitance | See figure | Cx | 5 | 18 | 30 | pF |
| H-level Input Voltage | | XVIH | 2 | - | VCC+0.3 | V |
| L-level Input Voltage | | XVIL | -0.3 | - | 0.8 | |
| External Oscillator Parallel Resistance | | Rp | *not needed* | | | Ω |
| External Oscillator Series Resistance | | Rs | *not needed* | | | |

Notes:

1. The crystal should be located as close as possible to CLKEB and CLKEA pins.
2. Recommended value for Cx is 18pF. This value may depend on the specific crystal characteristics.
3. Crystal Stability/Tolerance/Ageing values must be selected according to standard PRIME requirements.

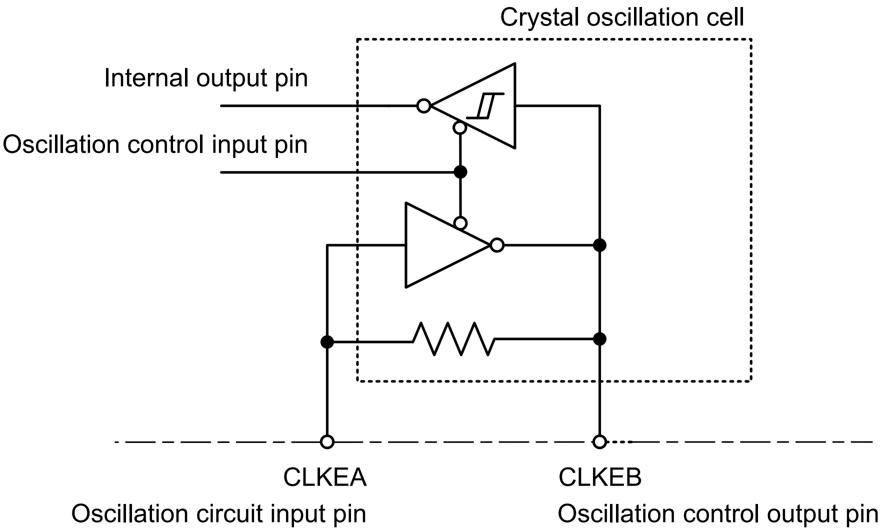
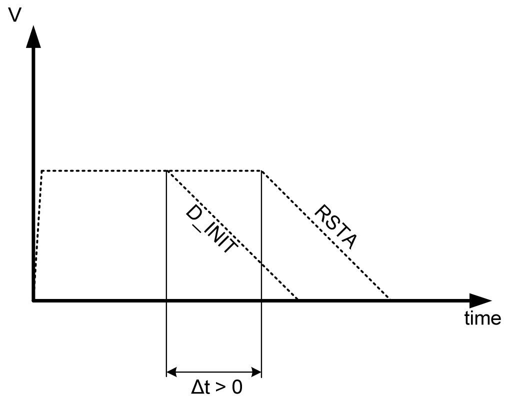


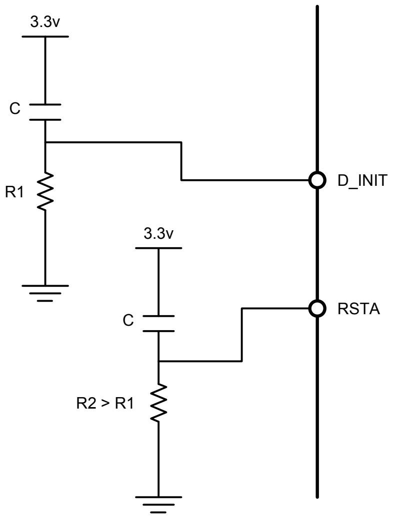
**Figure 4. Internal Oscillator Cell**

## 2.7 Power-on

In power-on, D_INIT should be released before asynchronous reset signal RSTA in order to ensure proper system start up.



Not minimum time is required between both releases, Δt > 0, so a simple RC circuit is enough to satisfy this requirement.

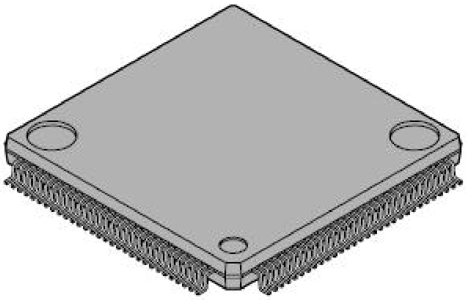


## 3. Mechanical data

120-pin plastic LQFP (14x14mm) Pb-free, RoHS compliant.

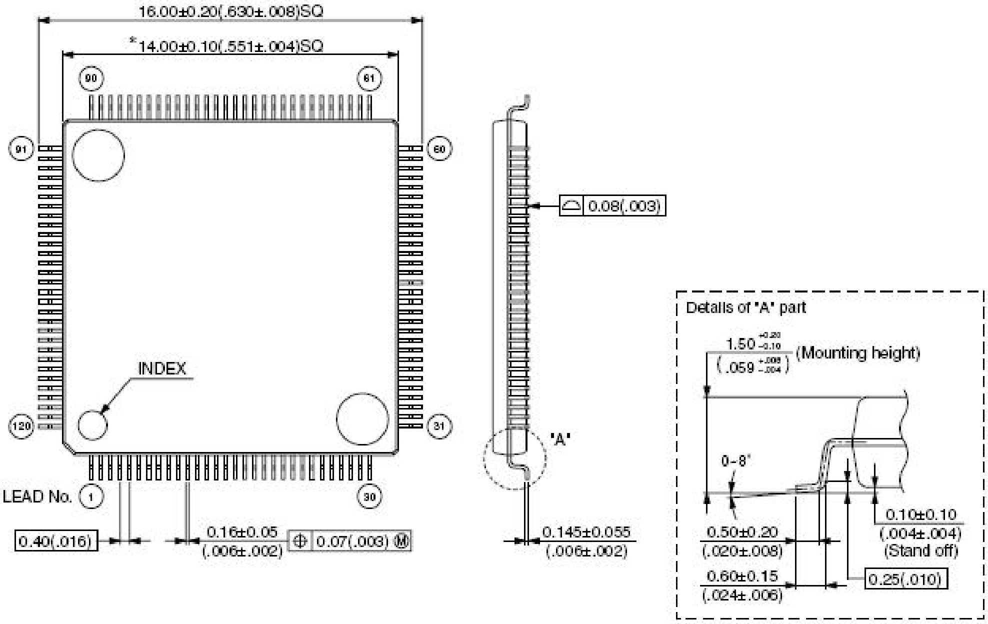
Ambient Temperature Range: -40ºC to +85ºC.

Ordering Code: **ADD1021AQF120**

| | | |
|---|---|---|
| 120-pin plastic LQFP | Lead pitch | 0.40 mm |
|  | Package width × package length | 14.0 mm × 14.0 mm |
| | Lead shape | Gullwing |
| | Sealing method | Plastic mold |
| | Mounting height | 1.70 mm MAX |
| | Code (Reference) | P-LFQFP120-14×14-0.40 |
| (FPT-120P-M24) | | |

120-pin plastic LQFP

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



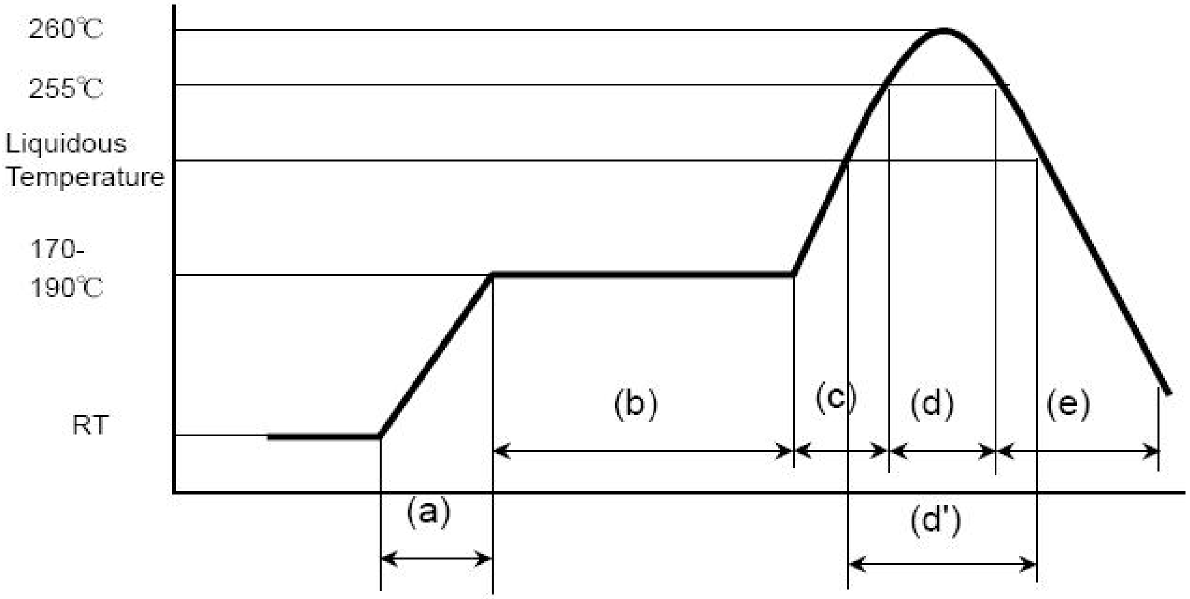
Dimensions in mm (inches).
Note: The values in parentheses are reference values.

## 3.1 Recommended mounting conditions

### 3.1.1 Conditions of Standard Reflow

| Items | Contents | |
|---|---|---|
| Method | IR(Infrared Reflow) / Convection | |
| Times | 2 | |
| Floor life | Before unpacking | Please use within 2 years after production |
| | From unpacking to second reflow | Within 8 days |
| | In case over period of floor life | Baking with 125°C +/- 3°C for 24hrs +2hrs/-0hrs is required. Then please use within 8 days. (please remember baking is up to 2 times) |
| Floor life condition | Between 5°C and 30°C and also below 70%RH required. (it is preferred lower humidity in the required temp range.) | |

**Temperature Profile**



**H rank: 260°C Max**

**(a) Average ramp-up rate: 1°C/s to 4°C/s**

**(b) Preheat & Soak: 170°C to 190°C, 60s to 180s**

**(c) Average ramp-un rate: 1°C/s to 4°C/s**

**(d) Peak temperature: 260°C Max, Up to 255°C within 10s**

**(d') Liquidous temperature: Up to 230°C within 40s or**
**Up to 225°C within 60s or**
**Up to 220°C within 80s**

**(e) Cooling: Natural cooling or forced cooling**

***Temperature on the top of the package is measured***

### 3.1.2 Manual Soldering

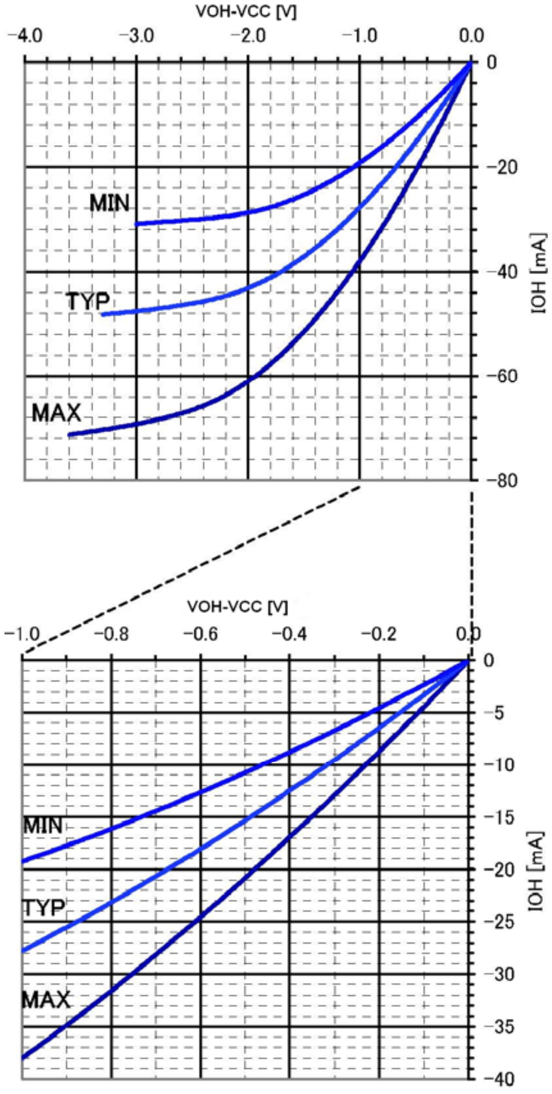
| **Items** | **Contents** | |
|---|---|---|
| Floor life | Before unpacking | Please use within 2 years after production |
| | From unpacking to Manual Soldering | Within 2 years after production (No control required for moisture adsorption because it is partial heating) |
| Floor life condition | Between 5°C and 30°C and also below 70%RH required. (It is preferred lower humidity in the required temp range.) | |
| Solder Condition | Temperature of soldering iron: Max 400°C, Time: Within 5 seconds/pin<br>*Be careful for touching package body with iron | |

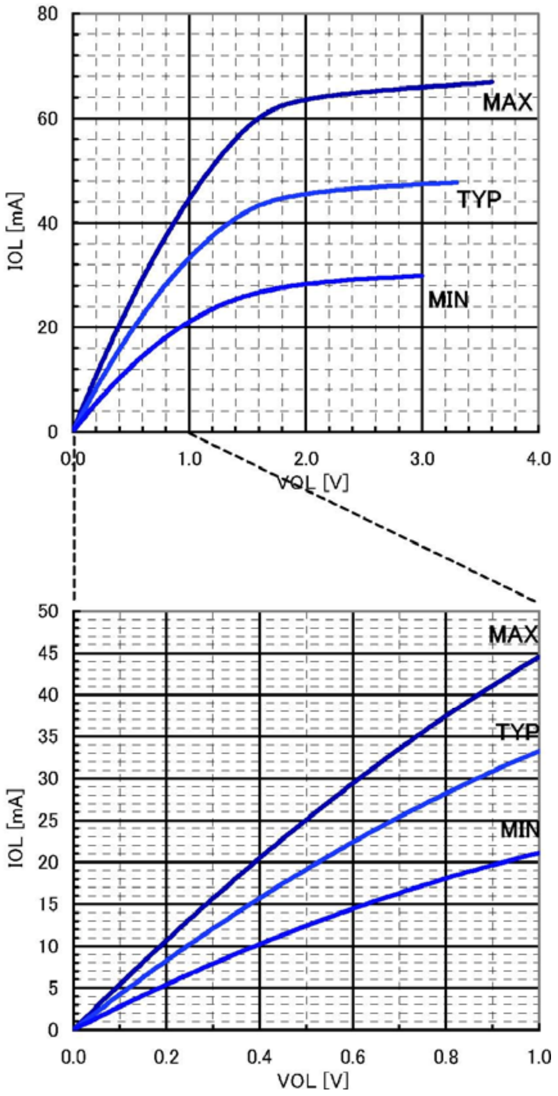
# 4. Annex 1

**V-I Characteristics 3.3 Vstandard CMOS IO L, M type**

**Pins marked in section 1.2 - pinout table with Nominal Current I(mA)=±5**

| | | | | | | |
|---|---|---|---|---|---|---|
| Condition: | MIN | Process=Slow | Tj= | 125°C | VCC= | 3.0 V |
| | TYP | Process=Typical | Tj= | 25°C | VCC= | 3.3 V |
| | MAX | Process=Fast | Tj= | -40°C | VCC= | 3.6 V |

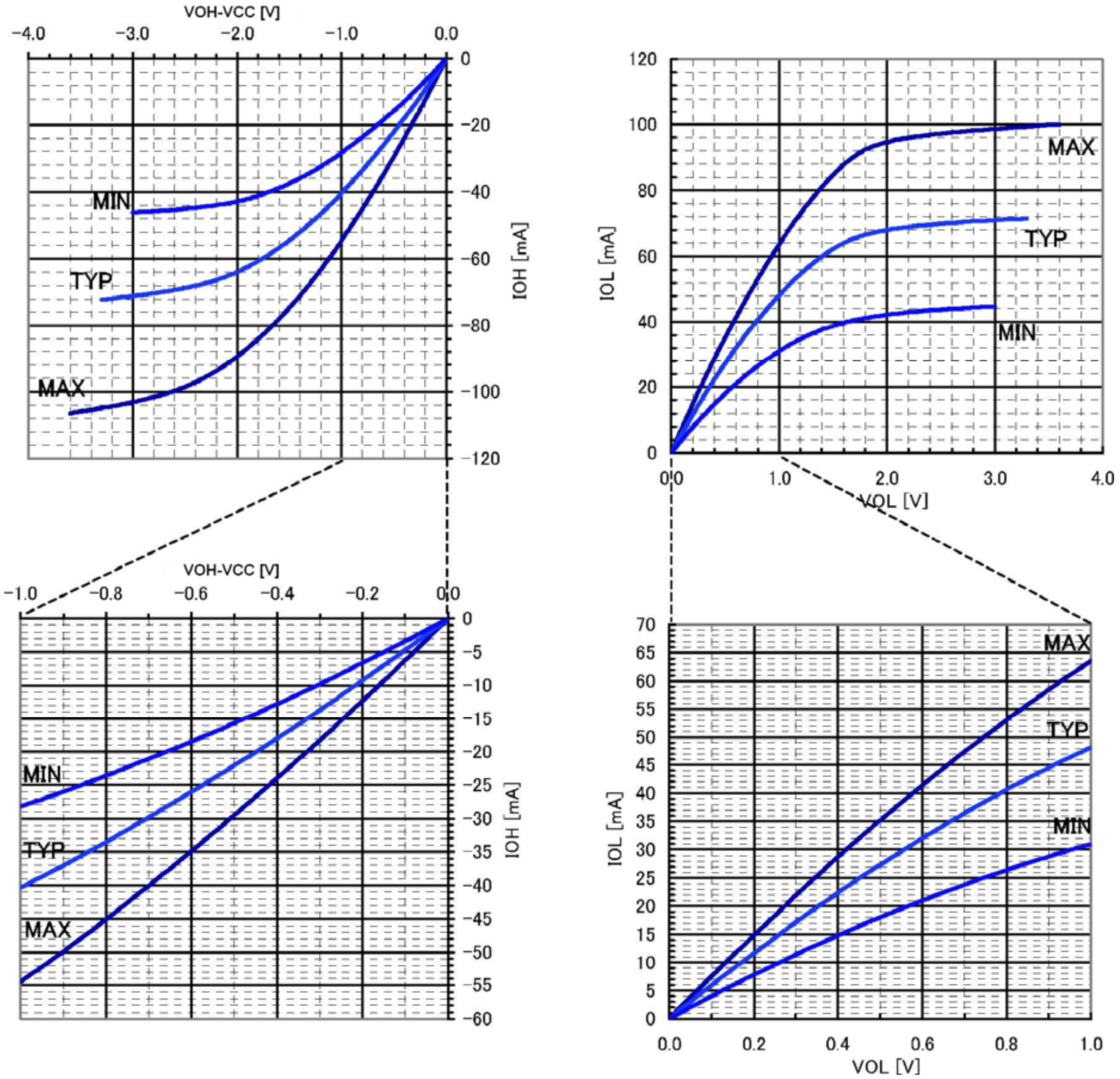




**V-I Characteristics 3.3 Vstandard CMOS IO H, V type**

**Pins marked in section 1.2 - pinout table with Nominal Current I(mA)=±10**

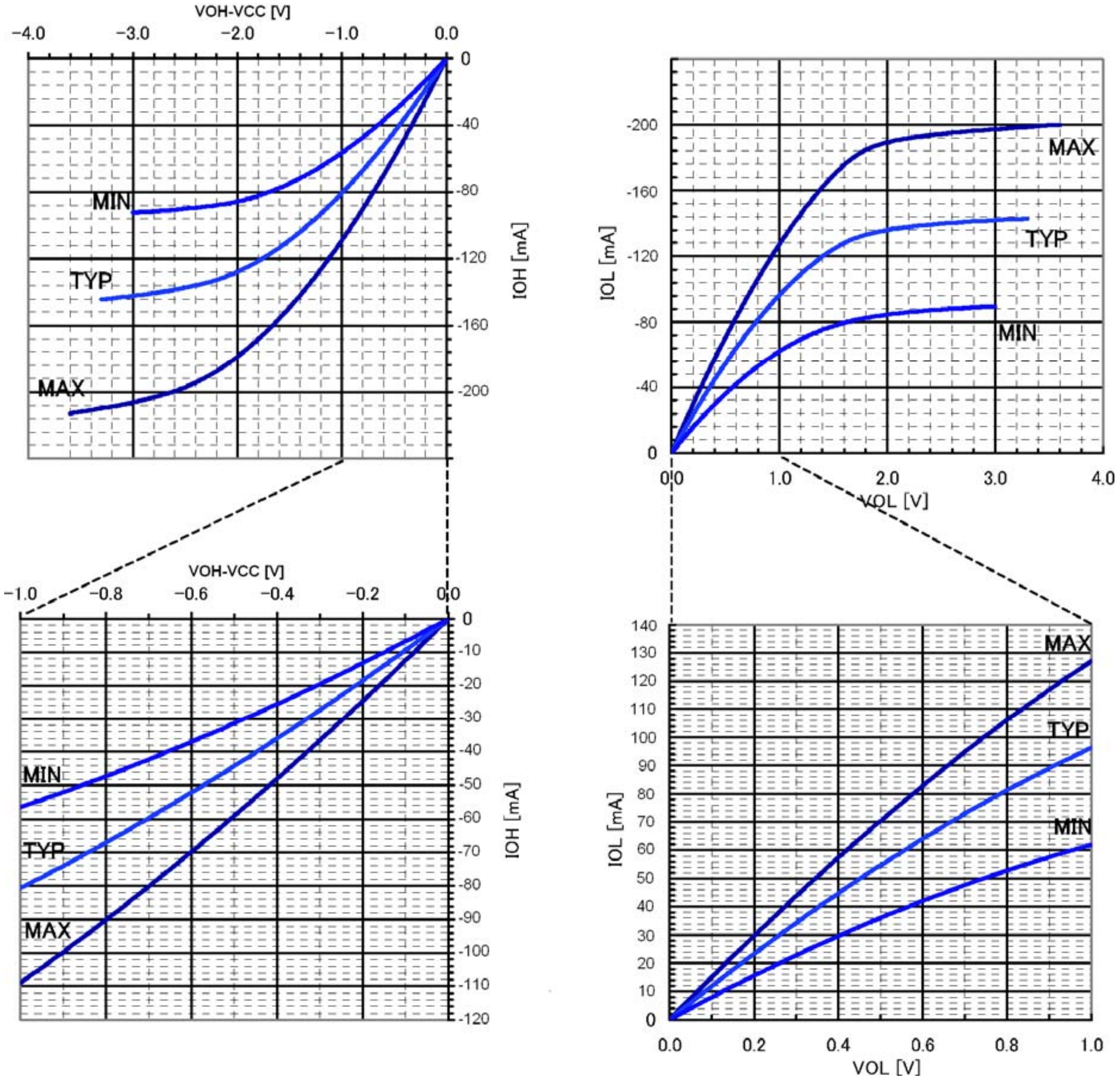
| | | | | | | |
|---|---|---|---|---|---|---|
| Condition: | MIN | Process=Slow | Tj= | 125°C | VCC= | 3.0 V |
| | TYP | Process=Typical | Tj= | 25°C | VCC= | 3.3 V |
| | MAX | Process=Fast | Tj= | -40°C | VCC= | 3.6 V |



**V-I Characteristics 3.3 Vstandard CMOS IO H, V type**

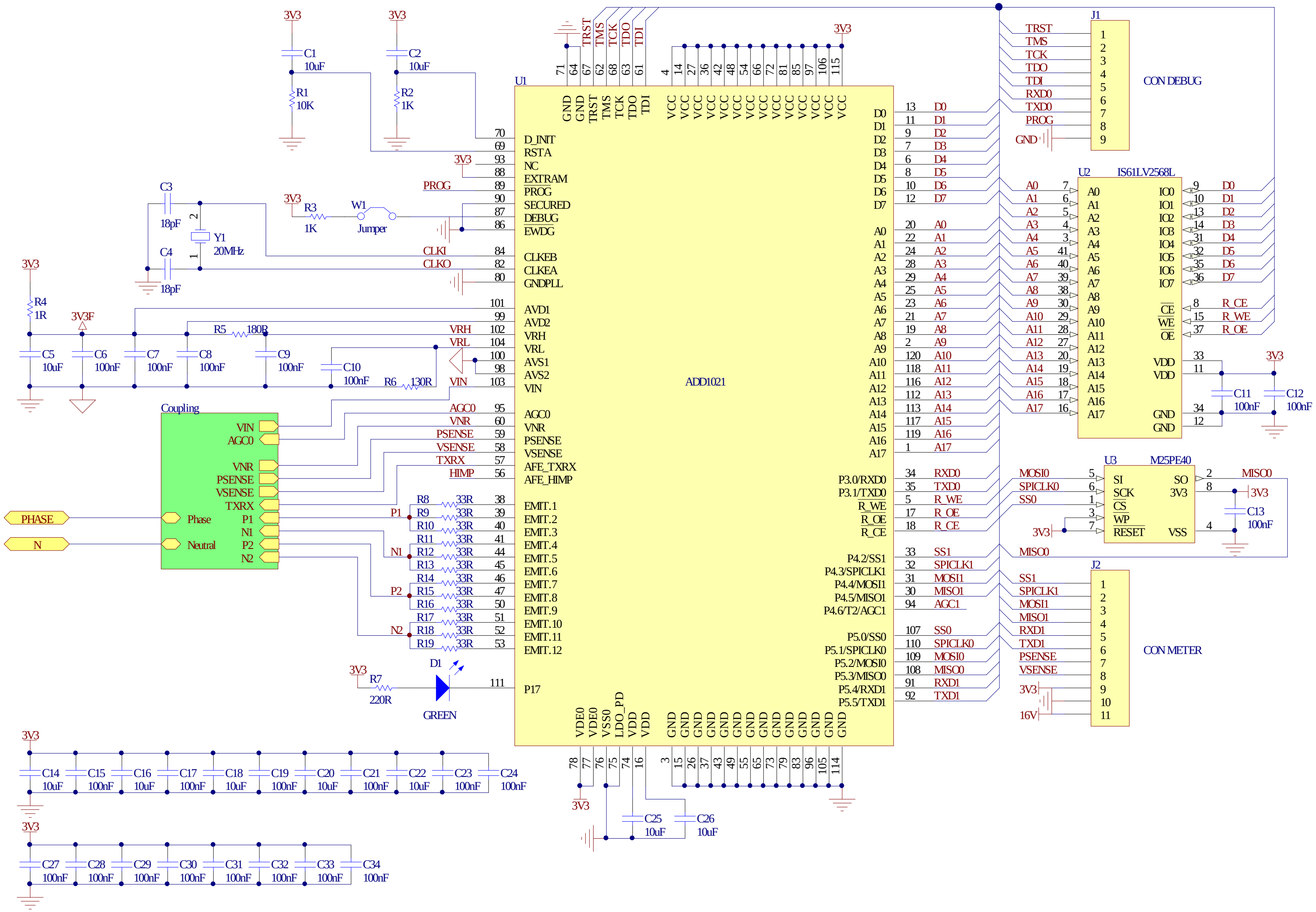
**Pins marked in section 1.2 - pinout table with Nominal Current I(mA)=±X**

| | | | | | | |
|---|---|---|---|---|---|---|
| Condition: | MIN | Process=Slow | Tj= | 125°C | VCC= | 3.0 V |
| | TYP | Process=Typical | Tj= | 25°C | VCC= | 3.3 V |
| | MAX | Process=Fast | Tj= | -40°C | VCC= | 3.6 V |



# 5. Annex 2

## 5.1 ADD1021 Application Circuit Example



## 5.2 Analog Front End example