AAT2789

SystemPower™

Low Noise, High Frequency Dual Step-Down Converter

General Description

The AAT2789 is a 2-channel synchronous step-down converter operating from an input voltage range of 2.7V to 5.5V, making it the ideal choice for single-cell Lithium-ion/polymer battery powered systems or low voltage 3.3V and 5V based consumer equipment.

Channel 1 delivers up to 1700mA output current while Channel 2 delivers up to 800mA. Both converters incorporate a unique low noise architecture which reduces output ripple and spectral noise.

The AAT2789 uses a high switching frequency to minimize external filter sizing. Peak current mode control eliminates external compensation while optimizing transient performance and stability.

The AAT2789 requires a minimum of external components to realize a high efficiency dual-output step-down converter while minimizing solution size and footprint.

Each of the step-down regulators has an independent input and enable pin. Externally adjustable output voltage is provided. Light load operating mode provides high efficiency over the entire load range. Low quiescent current enables excellent life for battery powered systems.

The AAT2789 is available in a 3x4mm Pb-free 16-pin TDFN package and is rated over the -40°C to 85°C operating temperature range.

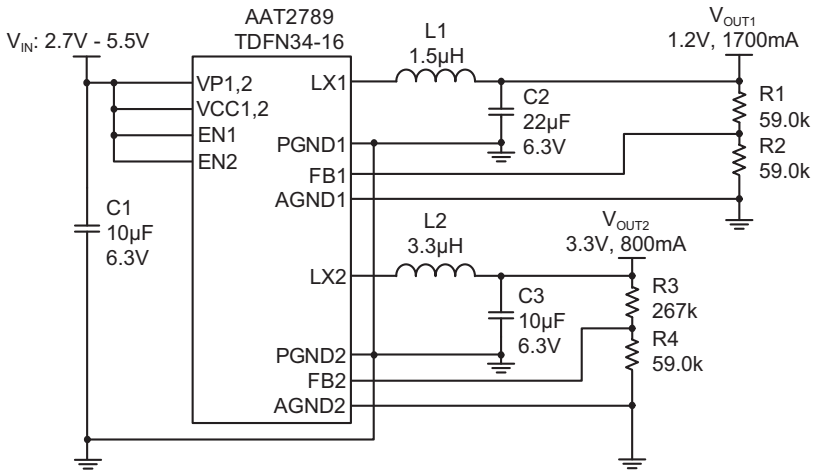
Features

- V_{IN} Range: 2.7V to 5.5V
- Output Voltage Range: 0.6V to V_{IN}
- Low Noise Light Load Mode
- Low Ripple PWM Mode
- Output Current:
  - Channel 1: 1700mA
  - Channel 2: 800mA
- Highly Efficient Step-Down Converters
- Low $R_{DS(ON)}$ Integrated Power Switches
- 100% Duty Cycle
- High Switching Frequency
- Peak Current Mode Control
- Internal Compensation
- Excellent Transient Response
- Internal Soft Start
- Fast Turn-On Time
- Over-Temperature Protection
- Current Limit Protection
- Low Profile TDFN34-16 Package
- -40°C to 85°C Temperature Range

Applications

- Cellular and Smart Phones
- Digital Cameras
- Handheld Instruments
- Mass Storage Systems
- Microprocessor / DSP Core / IO Power
- PDAs and Handheld Computers
- Portable Media Players
- USB Devices
- Wireless Data Systems

Typical Application

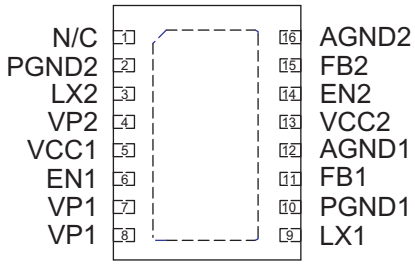


Pin Descriptions

Pin #	Symbol	Function
1	N/C	No connect.
2	PGND2	Power ground pin for Channel 2 step-down converter. Connect return of Channel 2 input and output capacitors close to this pin for best noise performance.
3	LX2	Channel 2 step-down converter switching pin. Connect output inductor to this pin. Inductor value is determined by output voltage.
4	VP2	Input supply voltage pin for Channel 2 step-down converter. Connect a 10µF ceramic input capacitor close to this pin or connect to VP1. Operating input voltage range is 2.7V to 5.5V.
5	VCC1	Input supply pin for Channel 1. Must be closely decoupled.
6	EN1	Enable Channel 1 input pin. Active high.
7,8	VP1	Input supply voltage pin for Channel 1 step-down converter. Connect a 10µF ceramic input capacitor close to this pin. Operating input voltage range is 2.7V to 5.5V.
9	LX1	Channel 1 step-down converter switching pin. Connect output inductor to this pin. Inductor value is determined by output voltage.
10	PGND1	Power ground pin for Channel 1 step-down converter. Connect return of Channel 1 input and output capacitors close to this pin for best noise performance.
11	FB1	Feedback pin for Channel 1. Connect an external resistor divider to this pin to program the output voltage to the desired value.
12	AGND1	Signal ground for Channel 1.
13	VCC2	Input supply pin for Channel 2. Must be closely decoupled.
14	EN2	Enable Channel 2 input pin. Active high.
15	FB2	Feedback pin for Channel 2. Connect an external resistor divider to this pin to program the output voltage to the desired value.
16	AGND2	Signal Ground for Channel 2.
EP	EP	Exposed paddle. Connect to PGND1 and PGND2 as close as possible to the device. Use properly sized vias for thermal coupling to the ground plane. See PCB layout guidelines.

Pin Configuration

TDFN34-16
(Top View)



Absolute Maximum Ratings[1]

Symbol	Description	Value	Units
V_{IN}	VP1, VP2, VCC1, VCC2 voltages to PGND, AGND	6.0	V
V_{LX}	V_{LX1}, V_{LX2} to PGND, AGND	-0.3 to V_{IN} + 0.3	V
V_{FB}	V_{FB1}, V_{FB2} to PGND, AGND	-0.3 to V_{IN} + 0.3	V
V_{EN}	V_{EN1}, V_{EN2} to PGND, AGND	-0.3 to 6.0	V
T_J	Operating Junction Temperature Range	-40 to 150	°C
T_{LEAD}	Maximum Soldering Temperature (at leads, 10 sec)	300	°C

Thermal Information

Symbol	Description	Value	Units
P_D	Maximum Power Dissipation[2]	2.0	W
Θ_{JA}	Thermal Resistance[1]	50	°C/W

1. Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum Rating should be applied at any one time.
2. Mounted on a FR4 board.
3. Derate 20mW/°C above 25°C ambient temperature.

Electrical Characteristics[1]

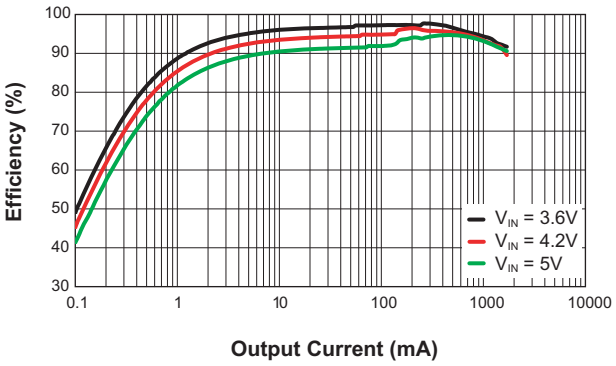
V_{IN} = 3.6V, T_A = -40°C to 85°C, unless noted otherwise. Typical values are at T_A = 25°C.

Symbol	Description	Conditions	Min	Typ	Max	Units
Channel 1: 1700mA Step-Down Converter						
V_{P1}, V_{CC1}	Input Voltage		2.7		5.5	V
V_{UVLO1}	UVLO Threshold	V_{P1} Rising			2.4	V
		V_{P1} Hysteresis		250		mV
		V_{P1} Falling	1.7			V
V_{OUT1}	Output Voltage Range		0.6		V_{P1}	V
$V_{OUT1(TOL)}$	Output Voltage Tolerance	I_{OUT1} = 0A to 1.7A; V_{P1} = 2.7V to 5.5V	-3.0		3.0	%
I_{Q1}	Quiescent Current	No load, V_{EN1} = V_{P1}, V_{EN2} = AGND		42	90	µA
I_{SHDN1}	Shutdown Current	V_{EN1} = GND			1.0	µA
I_{LIM1}	Current Limit		1800			mA
$R_{DSON(H)1}$	High Side On-Resistance			120		mΩ
$R_{DSON(L)1}$	Low Side On-Resistance			85		mΩ
$\Delta V_{LOADREG1}$	Load Regulation	I_{OUT1} = 0A to 1.7A		0.5		%
$\Delta V_{LINEREG1} / \Delta V_{P1}$	Line Regulation	V_{P1} = 2.7V to 5.5V		0.2		%/V
F_{OSC1}	Oscillator Frequency		1.12	1.40	1.68	MHz
T_{S1}	Start-Up Time	From Enable-1 to Output-1 Regulation		150		µs
Channel 2: 800mA Step-Down Converter						
V_{P2}, V_{CC2}	Input Voltage		2.7		5.5	V
V_{UVLO2}	UVLO Threshold	V_{P2} Rising			2.7	V
		V_{P2} Hysteresis		100		mV
		V_{P2} Falling	1.7			V
V_{OUT2}	Output Voltage Range		0.6		V_{P2}	V
$V_{OUT2(TOL)}$	Output Voltage Tolerance	I_{OUT2} = 0A to 800mA, V_{P2} = 2.7V to 5.5V	-3.0		3.0	%
I_{Q2}	Quiescent Current	No load, V_{EN2} = V_{P2}, V_{EN1} = AGND		37	70	µA
I_{SHDN2}	Shutdown Current	V_{EN2} = GND			1.0	µA
I_{LIM2}	Current Limit		900			mA
$R_{DSON(H)2}$	High Side On-Resistance			330		mΩ
$R_{DSON(L)2}$	Low Side On-Resistance			275		mΩ
$\Delta V_{LOADREG2}$	Load Regulation	I_{OUT2}= 0mA to 800mA		0.5		%
$\Delta V_{LINEREG2} / \Delta V_{P2}$	Line Regulation	V_{P2} = 2.7V to 5.5V		0.1		%/V
F_{OSC2}	Oscillator Frequency		0.9	2.0	2.6	MHz
T_{S2}	Start-Up Time	From Enable-2 to Output-2 Regulation		150		µs
Over-Temperature, EN Logic						
$T_{SD1,2}$	Over-Temperature Shutdown Threshold			140		°C
	Over-Temperature Shutdown Hysteresis			15		°C
$V_{EN1,2(L)}$	Enable Threshold Low				0.6	V
$V_{EN1,2(H)}$	Enable Threshold High		1.4			V
$I_{EN(1,2}$	Input Low Current		-1.0		1.0	µA

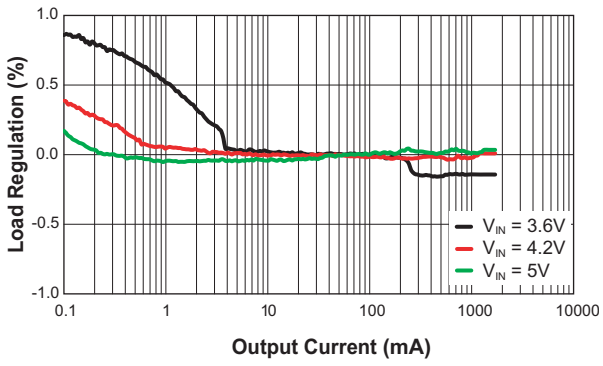
1. The AAT2789 is guaranteed to meet performance specifications over the –40°C to +85°C operating temperature range, and is assured by design, characterization and correlation with statistical process controls.

Typical Characteristics – Channel 1

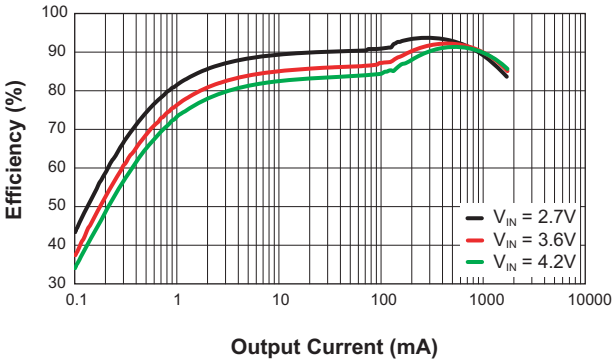
Efficiency vs. Output Current
(V_{OUT} = 3.3V)



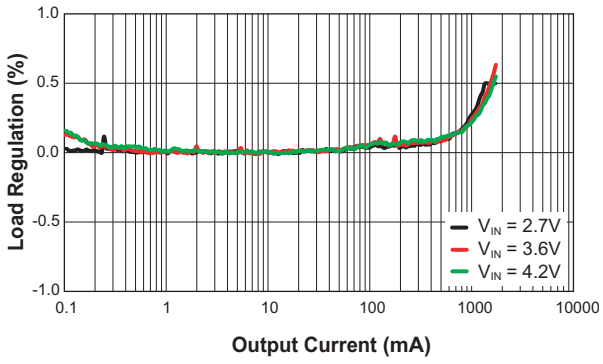
Load Regulation vs. Output Current
(V_{OUT} = 3.3V)



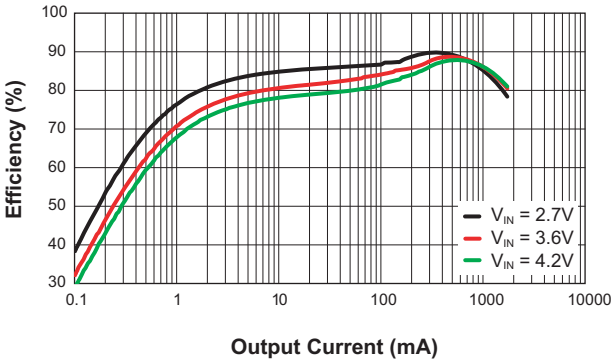
Efficiency vs. Output Current
(V_{OUT} = 1.8V)



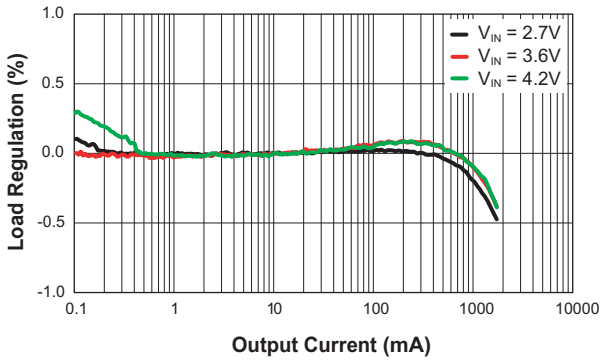
Load Regulation vs. Output Current
(V_{OUT} = 1.8V)



Efficiency vs. Output Current
(V_{OUT} = 1.2V)

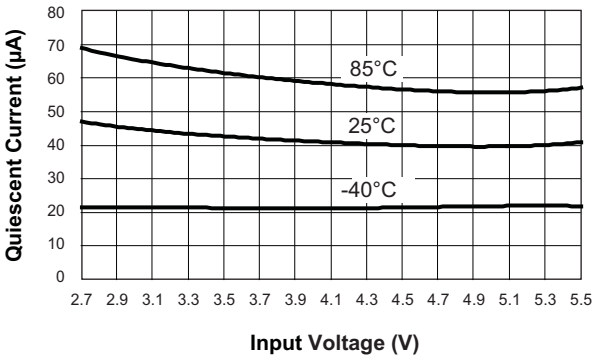


Load Regulation vs. Output Current
(V_{OUT} = 1.2V)

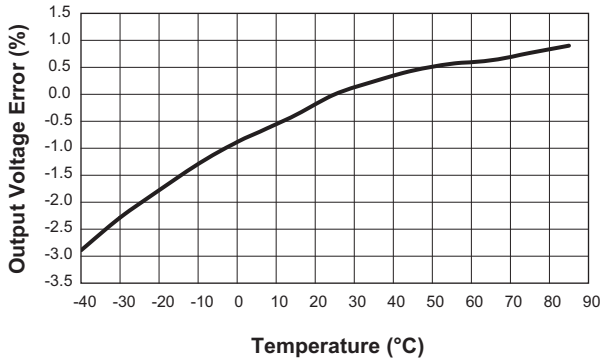


Typical Characteristics – Channel 1

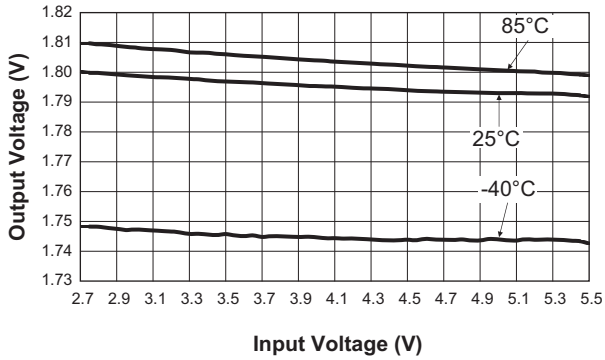
Quiescent Current vs. Input Voltage
(V_{OUT} = 1.8V; No Load)



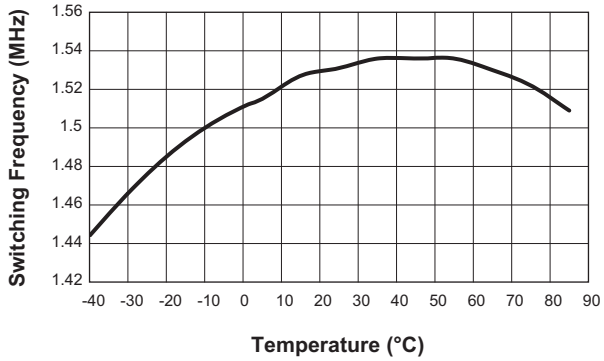
Output Voltage Error vs. Temperature
(V_{OUT} = 1.8V; I_{OUT} = 1A)



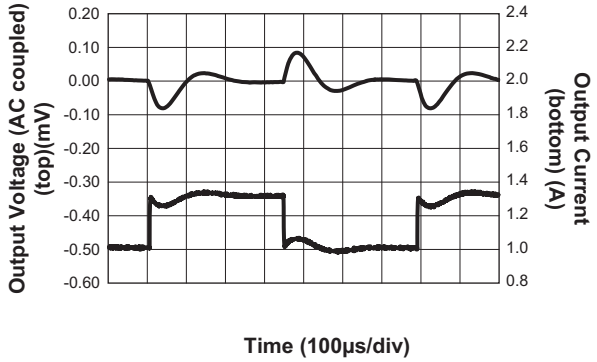
Output Voltage vs. Input Voltage
(V_{OUT} = 1.8V; I_{OUT} = 1A)



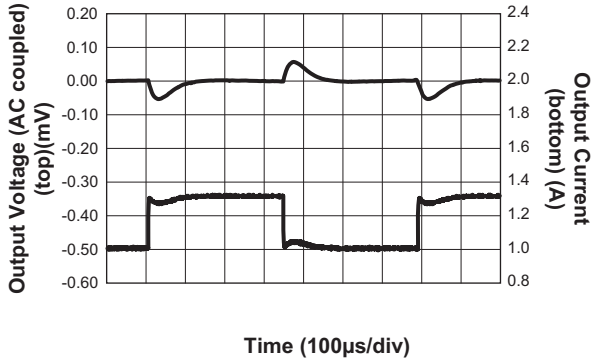
Switching Frequency vs. Temperature
(V_{OUT} = 1.8V; I_{OUT} = 1A)



Load Transient Response
(V_{OUT} = 1.8V)

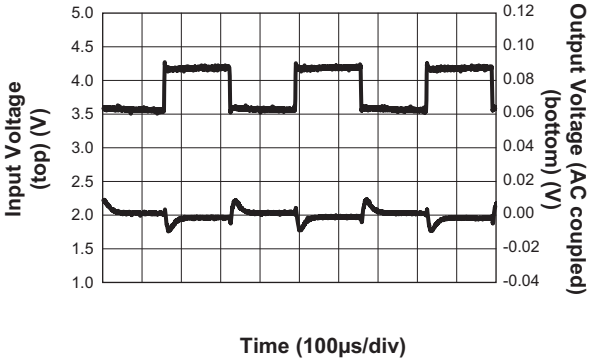


Load Transient Response
(V_{OUT} = 1.8V; C_{FF} = 100pF)

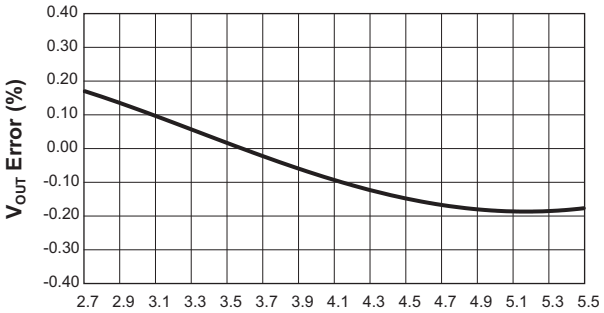


Typical Characteristics – Channel 1

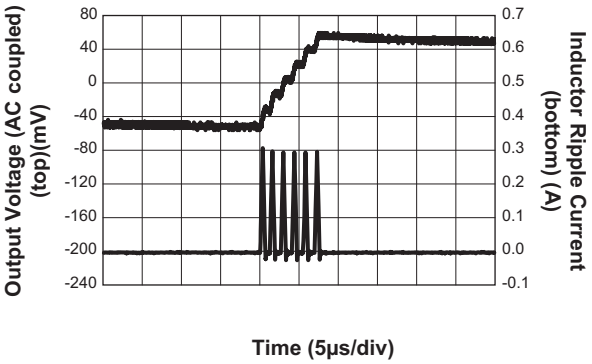
Line Transient Response
(V_{OUT} = 1.8V; I_{OUT} = 1.5A; C_{FF} = 100pF)



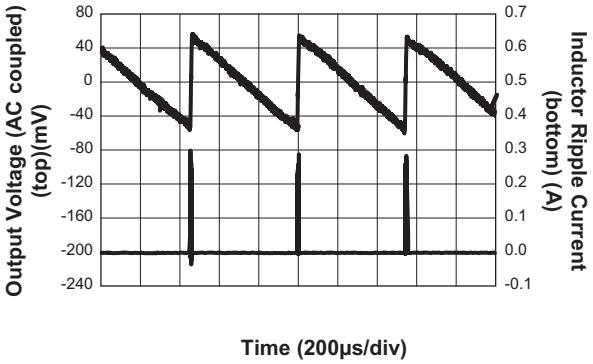
Line Regulation
(V_{OUT} = 1.8V; I_{OUT} = 1A)



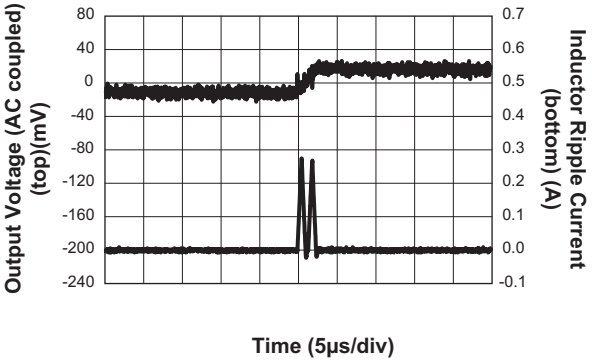
Light Load Switching Waveform
(V_{IN} = 3.6V; V_{OUT} = 1.8V; I_{OUT} = 1mA; C_{FF} = 0pF)



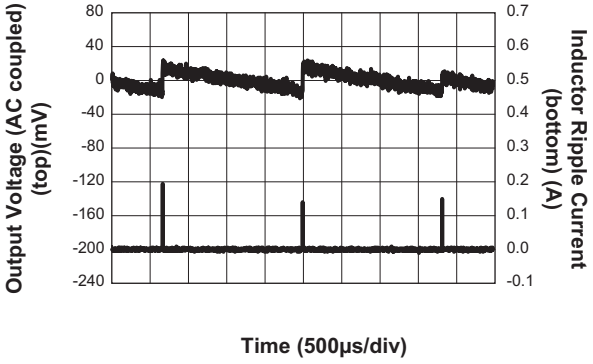
Light Load Switching Waveform
(V_{IN} = 3.6V; V_{OUT} = 1.8V; I_{OUT} = 1mA; C_{FF} = 0pF)



Light Load Switching Waveform
(V_{IN} = 3.6V; V_{OUT} = 1.8V; I_{OUT} = 1mA; C_{FF} = 100pF)

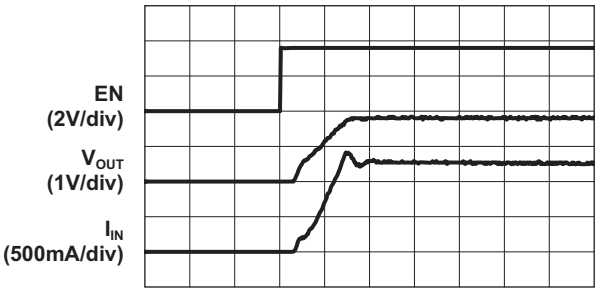


Light Load Switching Waveform
(V_{IN} = 3.6V; V_{OUT} = 1.8V; I_{OUT} = 1mA; C_{FF} = 100pF)

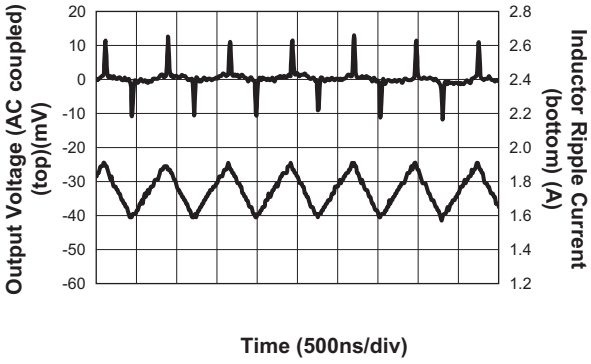


Typical Characteristics – Channel 1

Enable Soft Start
(V_{IN} = 3.6V; V_{OUT} = 1.8V; I_{OUT} = 1.7A)

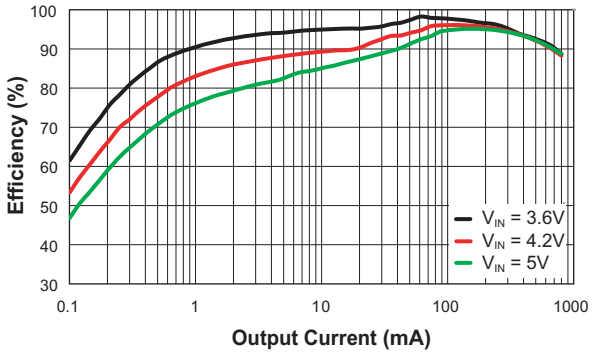


Heavy Load Switching Waveform
(V_{IN} = 3.6V; V_{OUT} = 1.8V; I_{OUT} = 1.7mA)

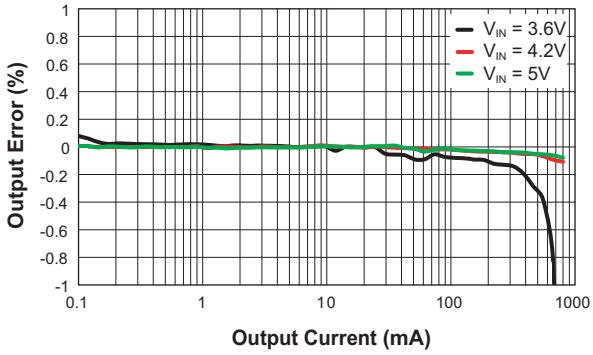


Typical Characteristics – Channel 2

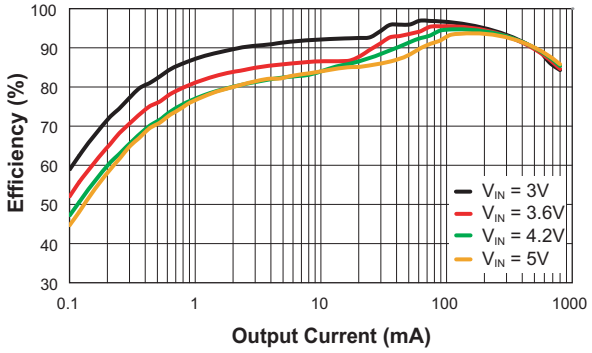
Efficiency vs. Output Current
(V_{OUT} = 3.3V)



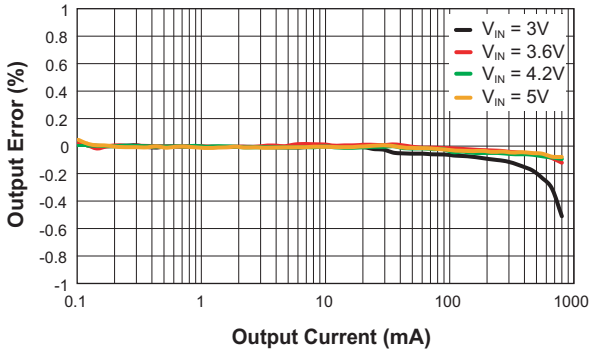
Load Regulation
(V_{OUT} = 3.3V)



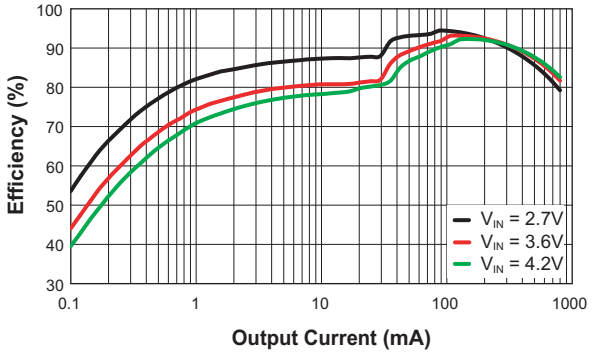
Efficiency vs. Output Current
(V_{OUT} = 2.5V)



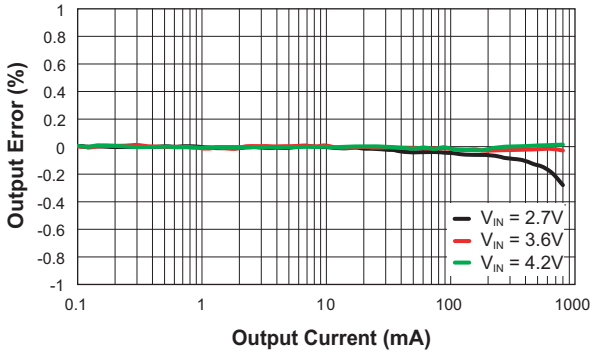
Load Regulation
(V_{OUT} = 2.5V)



Efficiency vs. Output Current
(V_{OUT} = 1.8V)

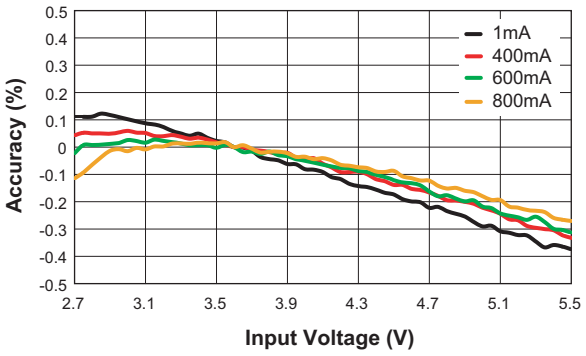


Load Regulation
(V_{OUT} = 1.8V)

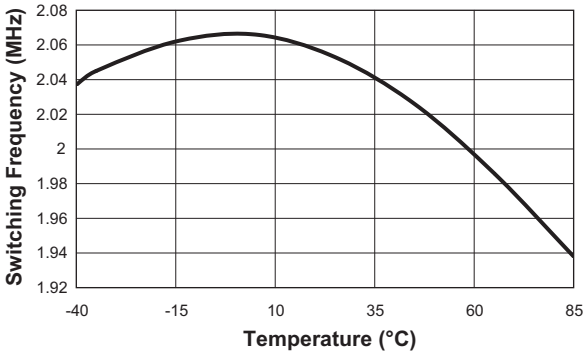


Typical Characteristics – Channel 2

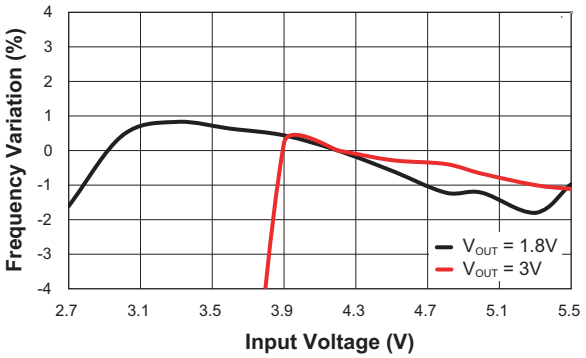
Line Regulation
(V_{OUT} = 1.8V)



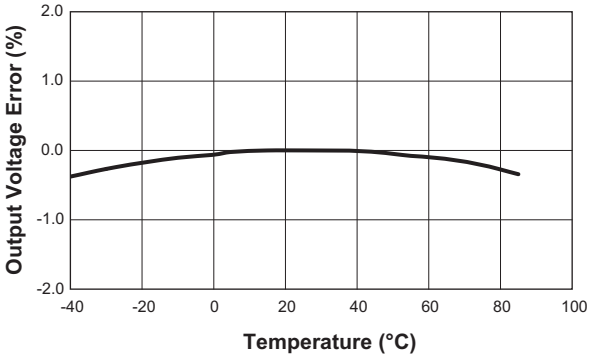
Switching Frequency vs. Temperature
(V_{OUT} = 1.8V; I_{OUT} = 800mA)



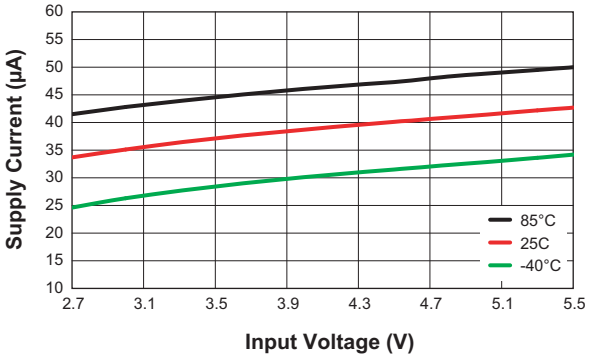
Frequency Variation vs. Input Voltage



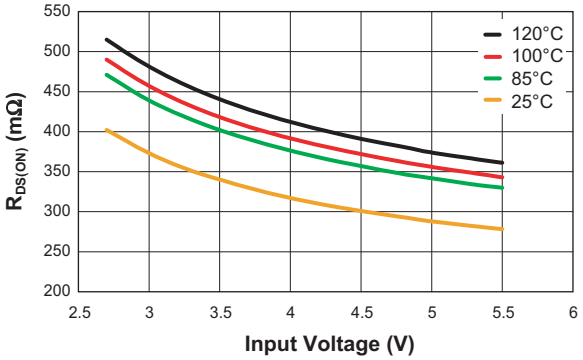
Output Voltage Error vs. Temperature
(V_{IN} = 3.6V; V_O = 1.8V, I_{OUT} = 400mA)



No Load Quiescent Current vs. Input Voltage

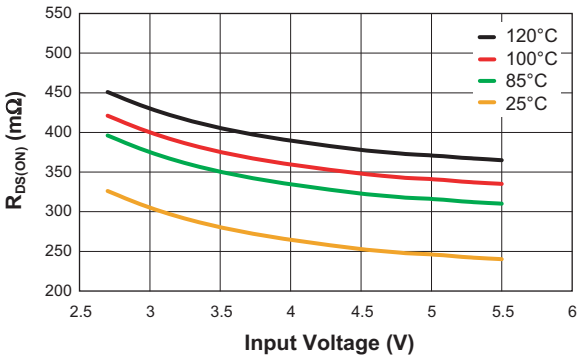


P-Channel $R_{DS(ON)}$ vs. Input Voltage

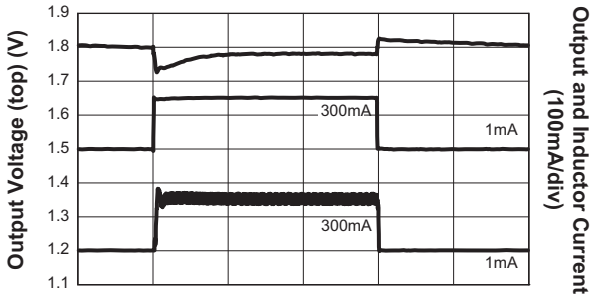


Typical Characteristics – Channel 2

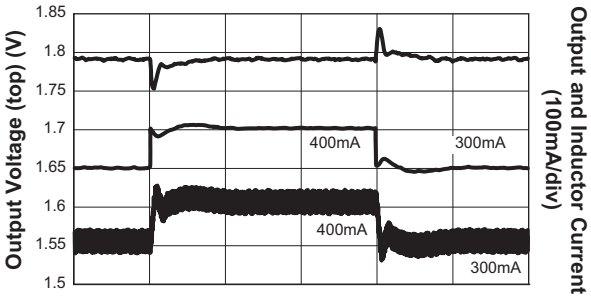
N-Channel $R_{DS(ON)}$ vs. Input Voltage



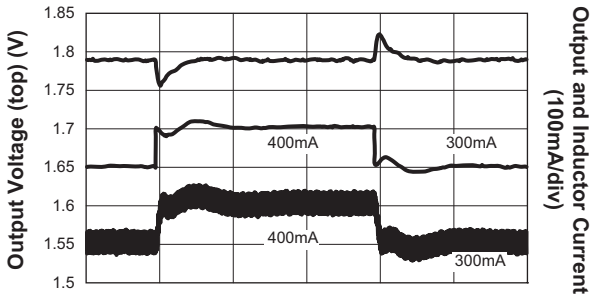
Load Transient
(V_{IN} = 3.6V; V_{OUT} = 1.8V; C_{OUT} = 10µF; C_{FF} = 100pF)



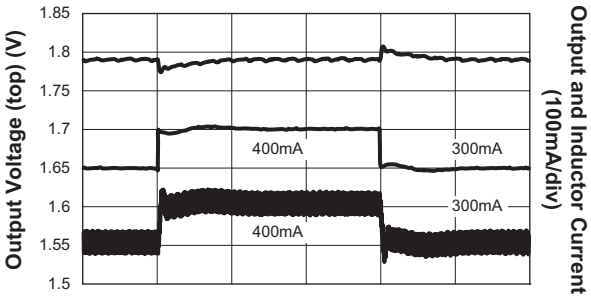
Load Transient
(V_{IN} = 3.6V; V_{OUT} = 1.8V; C_{OUT} = 4.7µF; C_{FF} = 0pF)



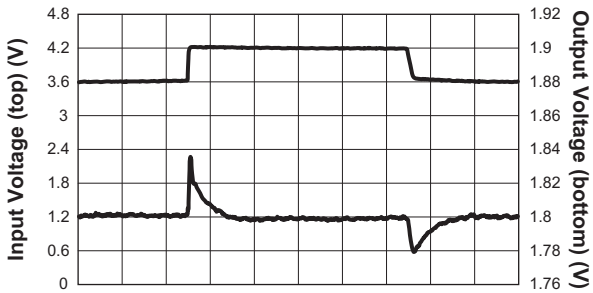
Load Transient
(V_{IN} = 3.6V; V_{OUT} = 1.8V; C_{OUT} = 10µF; C_{FF} = 0pF)



Load Transient
(V_{IN} = 3.6V; V_{OUT} = 1.8V; C_{OUT} = 10µF; C_{FF} = 100pF)

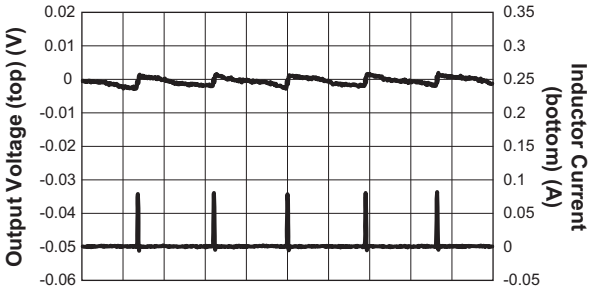


Line Transient
(V_{OUT} = 1.8V; V_{IN} = 3.6V to 4.2V; I_{OUT} = 400mA; C_{FF} = 0pF)

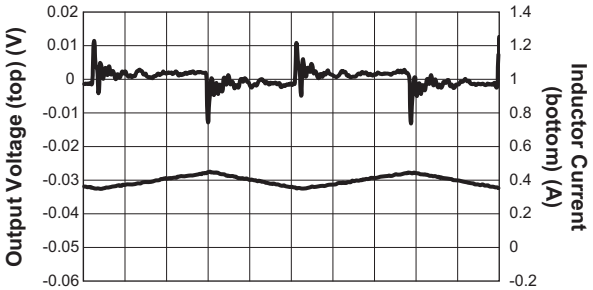


Typical Characteristics – Channel 2

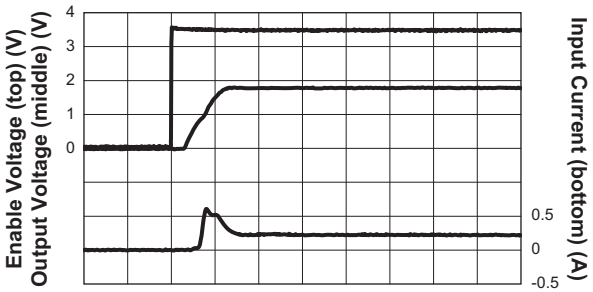
Output Ripple
(V_{OUT} = 1.8V; V_{IN} = 3.6V; I_{OUT} = 1mA; C_{FF} = 0pF)



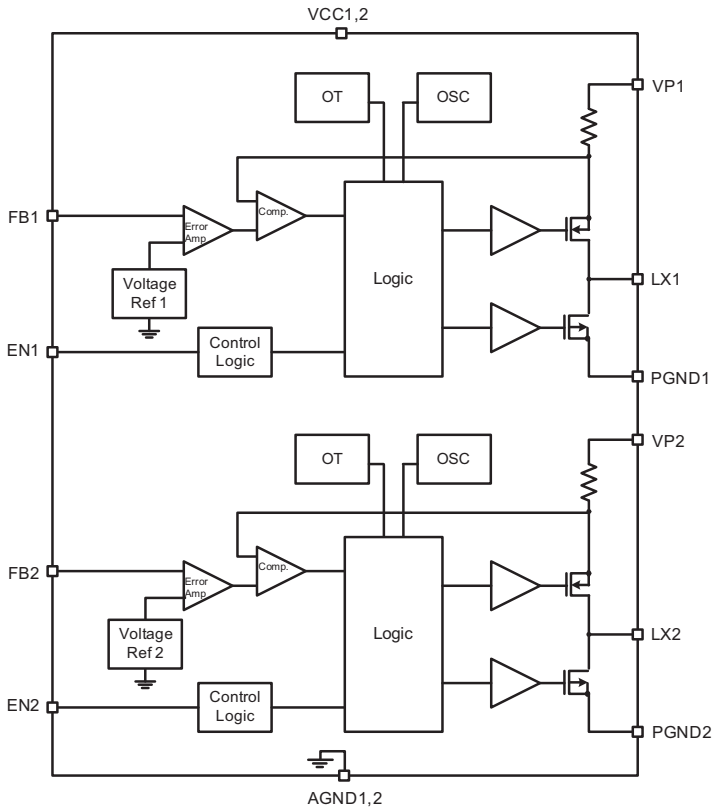
Output Ripple
(V_{OUT} = 1.8V; V_{IN} = 3.6V; I_{OUT} = 400mA; C_{FF} = 0pF)



Soft Start
(V_{IN} = 3.6V; V_{OUT} = 1.8V; I_{OUT} = 400mA)



Functional Block Diagram



Functional Description

The AAT2789 is a 2-channel synchronous step-down (Buck) converter operating from an input voltage range of 2.7V to 5.5V; making it the ideal choice for single-cell Lithium-ion/polymer battery powered systems or low voltage 3.3V and 5V based consumer equipment.

Channel 1 delivers up to 1700mA output current while Channel 2 delivers up to 800mA. Both converters incorporate a unique low noise architecture which reduces output ripple and spectral noise.

The device utilizes a high switching frequency to minimize external filter sizing. Peak current mode control eliminates external compensation while optimizing transient performance and stability.

The device requires a minimum of external components to realize a high efficiency dual-output step-down converter while minimizing solution size and footprint.

Each of the step-down regulators has an independent input and enable pin. Adjustable output voltage is provided. Light load operating mode provides high efficiency over the entire load range. The enable inputs, when pulled low, force the respective converter into a low power non-switching state consuming less than 1µA of current. Low quiescent current enables excellent life for battery powered systems.

Additional features include integrated soft start to limit inrush current. Soft start limits the current surge seen at the input and eliminates output voltage overshoot.

For overload conditions, the peak input current is limited. Also, over-temperature protection safeguards the device from damage due to high operating temperature or fault conditions. The junction over-temperature threshold is 140°C with 15°C of hysteresis. Under voltage lockout (UVLO) guarantees sufficient input voltage bias prior to turn-on.

The AAT2789 is available in the 3x4mm Pb-free 16-pin TDFN package and is rated over the -40°C to 85°C operating temperature range.

Applications Information

Inductor Selection

Both step-down converters use peak current mode control with slope compensation to maintain stability for duty cycles greater than 50%. When the duty cycle exceeds 50%, the inductor value must be selected to maintain the prescribed down-slope in accordance with the internal slope compensation requirements.

Channel 1

The internal slope compensation for the adjustable and low voltage fixed versions of Channel 1 is 0.75A/µs. This equates to a slope compensation that is 75% of the inductor current down slope for a 1.8V output and 1.8µH inductor.

$$m = \frac{0.75 \cdot V_O}{L} = \frac{0.75 \cdot 1.8V}{1.8\mu H} = 0.75\frac{A}{\mu s}$$

$$L = \frac{0.75 \cdot V_O}{m} = \frac{0.75 \cdot 1.2V}{0.75\frac{A}{\mu s}} = 1.2\mu H$$

The inductor should be set equal to the output voltage numeric value in microhenries (µH). This guarantees sufficient internal slope compensation. Manufacturer's specifications list both the inductor DC current rating, which is a thermal limitation, and the peak current rating, which is determined by the saturation characteristics. The inductor should not show any appreciable saturation under normal load conditions. Some inductors may meet the peak and average current ratings yet result in excessive losses due to a high DCR. Always consider the losses associated with the DCR and its effect on the total converter efficiency when selecting an inductor.

Channel 2

The slope compensation for Channel 2 output is set at 0.75A/us. This equates to a slope compensation that is 75% of the inductor current down slope for a 1.8V output and 1.8µH inductor:

$$m = \frac{0.75 \cdot V_O}{L} = \frac{0.75 \cdot 1.8V}{1.8\mu H} = 0.75\frac{A}{\mu s}$$

$$L = \frac{0.75 \cdot V_O}{m} = \frac{0.75 \cdot 3.3V}{0.75\frac{A}{\mu s}} = 3.3\mu H$$

Input Capacitor

Select a 10µF to 22µF X7R or X5R ceramic capacitor for the input. To estimate the required input capacitor size, determine the acceptable input ripple level (V_{PP}) and solve for C_{IN}. The calculated value varies with input voltage and is a maximum when V_{IN} is double the output voltage.

$$C_{IN} = \frac{\frac{V_O}{V_{IN}} \cdot \left(1 - \frac{V_O}{V_{IN}}\right)}{\left(\frac{V_{PP}}{I_O} - ESR\right) \cdot F_S}$$

$$\frac{V_O}{V_{IN}} \cdot \left(1 - \frac{V_O}{V_{IN}}\right) = \frac{1}{4} \text{ for } V_{IN} = 2 \cdot V_O$$

$$C_{IN(MIN)} = \frac{1}{\left(\frac{V_{PP}}{I_O} - ESR\right) \cdot 4 \cdot F_S}$$

Always examine the ceramic capacitor DC voltage coefficient characteristics when selecting the proper value. For example, the capacitance of a 10µF, 6.3V, X5R ceramic capacitor with 5.0V DC applied is actually about 6µF.

The maximum input capacitor RMS current is:

$$I_{RMS} = I_O \cdot \sqrt{\frac{V_O}{V_{IN}} \cdot \left(1 - \frac{V_O}{V_{IN}}\right)}$$

The input capacitor RMS ripple current varies with the input and output voltage and will always be less than or equal to half of the total DC load current.

$$\sqrt{\frac{V_O}{V_{IN}} \cdot \left(1 - \frac{V_O}{V_{IN}}\right)} = \sqrt{D \cdot (1 - D)} = \sqrt{0.5^2} = \frac{1}{2}$$

For $V_{IN} = 2 \cdot V_O$

$$I_{RMS(MAX)} = \frac{I_O}{2}$$

The term $\frac{V_O}{V_{IN}} \cdot \left(1 - \frac{V_O}{V_{IN}}\right)$ appears in both the input voltage ripple and input capacitor RMS current equations and is a maximum when V_O is twice V_{IN}. This is why the input voltage ripple and the input capacitor RMS current ripple are a maximum at 50% duty cycle.

The input capacitor provides a low impedance loop for the edges of pulsed current drawn by the AAT2789. Low ESR/ESL X7R and X5R ceramic capacitors are ideal for this function. To minimize stray inductance, the capacitor should be placed as closely as possible to the IC. This keeps the high frequency content of the input current localized, minimizing EMI and input voltage ripple. The proper placement of the input capacitor (C1) can be seen in the evaluation board layout in the Layout section of this datasheet (see Figures 1 and 2).

A laboratory test set-up typically consists of two long wires running from the bench power supply to the evaluation board input voltage pins. The inductance of these wires, along with the low-ESR ceramic input capacitor, can create a high Q network that may affect converter performance. This problem often becomes apparent in the form of excessive ringing in the output voltage during load transients. Errors in the loop phase and gain measurements can also result. Since the inductance of a short PCB trace feeding the input voltage is significantly lower than the power leads from the bench power supply, most applications do not exhibit this problem.

In applications where the input power source lead inductance cannot be reduced to a level that does not affect the converter performance, a high ESR tantalum or aluminum electrolytic should be placed in parallel with the low ESR/ESL bypass ceramic capacitor. This dampens the high Q network and stabilizes the system.

Output Capacitor

Channel 1

The output capacitor limits the output ripple and provides holdup during large load transitions. A 10µF to 22µF X5R or X7R ceramic capacitor typically provides sufficient bulk capacitance to stabilize the output during large load transitions and has the ESR and ESL characteristics necessary for low output ripple.

The output voltage droop due to a load transient is dominated by the capacitance of the ceramic output capacitor. During a step increase in load current, the ceramic output capacitor alone supplies the load current until the loop responds. Within two or three switching cycles, the loop responds and the inductor current increases to match the load current demand. The relationship of the output voltage droop during the three switching cycles to the output capacitance can be estimated by:

$$C_{OUT} = \frac{3 \cdot \Delta I_{LOAD}}{V_{DROOP} \cdot F_S}$$

Once the average inductor current increases to the DC load level, the output voltage recovers. The above equation establishes a limit on the minimum value for the output capacitor with respect to load transients.

The internal voltage loop compensation also limits the minimum output capacitor value to 10µF. This is due to its effect on the loop crossover frequency (bandwidth), phase margin, and gain margin. Increased output capacitance will reduce the crossover frequency with greater phase margin.

The maximum output capacitor RMS ripple current is given by:

$$I_{RMS(MAX)} = \frac{1}{2 \cdot \sqrt{3}} \cdot \frac{V_{OUT} \cdot (V_{IN(MAX)} - V_{OUT})}{L \cdot F_S \cdot V_{IN(MAX)}}$$

Dissipation due to the RMS current in the ceramic output capacitor ESR is typically minimal, resulting in less than a few degrees rise in hot-spot temperature.

Channel 2

The output capacitor limits the output ripple and provides holdup during large load transitions. A 4.7µF to 10µF X5R or X7R ceramic capacitor typically provides sufficient bulk capacitance to stabilize the output during large load transitions and has the ESR and ESL characteristics necessary for low output ripple.

Output Voltage

The AAT2789 output voltages are programmed with external resistors R1, R2 (Channel 1) and R3, R4 (Channel 2). To limit the bias current required for the external feedback resistor string while maintaining good noise immunity, the minimum suggested value for R2 and R4 are 59kΩ. Although a larger value will further reduce quiescent current, it will also increase the impedance of the feedback node, making it more sensitive to external noise and interference. Table 1 summarizes the resistor values for various output voltages with R2 and R4 set to either 59kΩ for good noise immunity or 221kΩ for reduced no load input current.

V_{OUT}(V)	$R_{2,4}$ = 59kΩ $R_{1,3}$(kΩ)	$R_{2,4}$ = 221kΩ $R_{1,3}$(kΩ)
0.6	0	0
0.8	19.6	75.0
0.9	29.4	113
1.0	39.2	150
1.1	49.9	187
1.2	59.0	221
1.3	68.1	261
1.4	78.7	301
1.5	88.7	332
1.8	118	442
1.85	124	464
2.0	137	523
2.5	187	715
3.0	237	887
3.3	267	1000

Table 1: AAT2789 Resistor Values for Various Output Voltages.

Thermal Calculations

There are three types of losses associated with the AAT2789 step-down converter: switching losses, conduction losses, and quiescent current losses. Conduction losses are associated with the $R_{DS(ON)}$ characteristics of the power output switching devices. Switching losses are dominated by the gate charge of the power output switching devices. At full load, assuming continuous conduction mode (CCM), a simplified form of both step-down converters is given by:

$$P_{TOTAL} = \frac{I_{O1}^2 \cdot (R_{DSON(HS)} \cdot V_{O1} + R_{DSON(L)} \cdot [V_{IN} - V_{O1}])}{V_{IN1}} + (t_{sw} \cdot F_S \cdot I_{O1} + I_{Q1}) \cdot V_{IN1}$$

$$+ \frac{I_{O2}^2 \cdot (R_{DSON(HS)} \cdot V_{O2} + R_{DSON(L)} \cdot [V_{IN} - V_{O2}])}{V_{IN2}} + (t_{sw} \cdot F_S \cdot I_{O2} + I_{Q2}) \cdot V_{IN2}$$

I_{Q1} and I_{Q2} are the step-down converter quiescent currents for Channel 1 and Channel 2 respectively. The term t_{SW} is used to estimate the full load step-down converter switching losses.

For the condition where the step-down converter is in dropout at 100% duty cycle, the total device dissipation reduces to:

$$P_{TOTAL} = I_{O1}^2 \cdot R_{DS(ON)H1} + I_{Q1} \cdot V_{IN1} + I_{O2}^2 \cdot R_{DS(ON)H2} + I_{Q2} \cdot V_{IN2}$$

Since $R_{DS(ON)}$, quiescent current, and switching losses all vary with input voltage, the total losses should be investigated over the complete input voltage range.

Given the total losses, the maximum junction temperature can be derived from the θ_{JA} for the TDFN34-16 package, which is 50°C/W.

$$T_{J(MAX)} = P_{TOTAL} \cdot \Theta_{JA} + T_{AMB}$$

PCB Layout

The suggested PCB layout for the AAT2789 is shown in Figures 1 and 2. The following guidelines should be used to help ensure a proper layout.

1. The input and output capacitors C1, C2, C3, and C4 should be connected as closely as possible to the input and output pins.
2. Output capacitors and inductors (C2, C3 and L1; C4 and L2) should connect as closely as possible. The connection of the inductor (L1, L2) to the LX1 and LX2 pins should be as short as possible.
3. The feedback traces or FB pins should be separated from any power traces and connect as closely as possible to the load point. Sensing along a high-current load trace will degrade DC load regulation.
4. The resistance of the trace from the load return to PGND should be kept to a minimum. This will help to minimize any error in DC regulation due to differences in the potential of the internal signal ground and the power ground.
5. The lower R2 (FB1) and R4 (FB2) resistor's grounds should be connected to the AGND1 and AGND2 pins.
6. C5, C6 are optional feed forward capacitors for both channels to stabilize the output voltage during large load transitions.
7. For good thermal coupling, PCB vias are required from the pad for the TDFN paddle to the bottom ground plane.

Printed Circuit Board Layout Recommendations

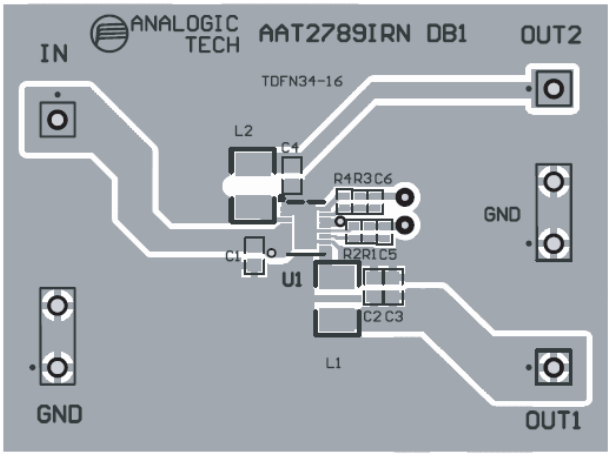


Figure 1: AAT2789 Evaluation Board Component Side Layout.

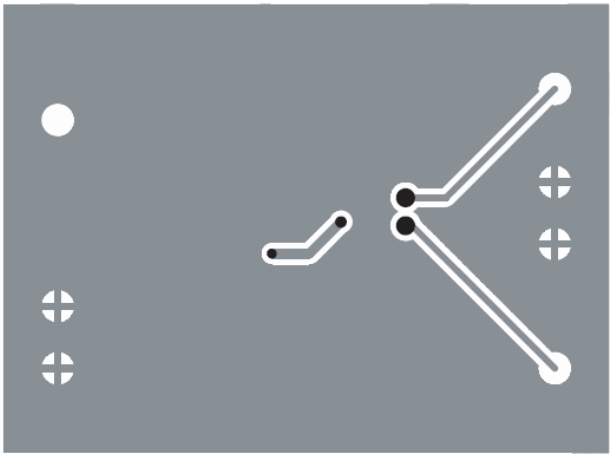


Figure 2: AAT2789 Evaluation Board Solder Side Layout.

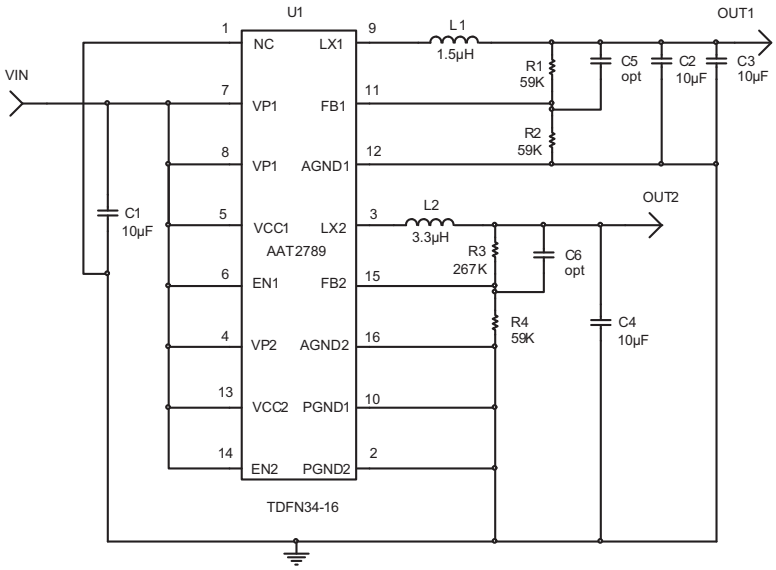


Figure 3: AAT2789 Evaluation Board Schematic.

Symbol	Part Number	Description	Qty
U1	AAT2789	AnalogicTech 2-Output Buck TDFN34-16	1
C1, C2, C3, C4	GRM188R60J106ME47D	Cap, MLC, 10uF/6.3V, 0603 (H_{MAX}=0.9mm), Murata	4
C5	Generic	Cap,10nF/6.3V,0402	1
C6	Generic	Cap,100pF/6.3V,0402	1
L1	LQM2HPN1R5MG0	1.5uH, I_{SAT}=3A, 2x2.5x0.9mm (H_{MAX}=0.95mm), shielded chip inductor, Murata	1
L2	TFC252008MBT	3.3uH, I_{SAT}=0.52A, 2x2.5x1mm (H_{MAX}=1.0mm), non-shielded chip inductor, TDK	1
R1-R4	Generic	Carbon Film resistor, 0402	1

Table 1: AAT2789 Bill of Materials.

Design Example

Specifications

V_{O1} = 1.2V @ 1.5A (adjustable using 0.6V version), Pulsed Load ΔI_{LOAD} = 1.5A
V_{O2} = 3.3V @ 500mA (adjustable using 0.6V version), Pulsed Load ΔI_{LOAD} = 0.5A
V_{IN} = 2.7V to 4.2V (3.6V nominal)
F_{S1} = 1.8MHz, F_{S2} = 2MHz
m = 0.75A/µs
T_{AMB} = 85°C in TDFN34-16 Package

Channel 1 Inductor

$$L = \frac{0.75 \cdot V_O}{m} = \frac{0.75 \cdot 1.2V}{0.75\frac{A}{\mu s}} = 1.2\mu H; \text{ use } 1.5\mu H$$

For TDK inductor LQM2PHN1R5MG0, 1.5µH, DCR = 70mΩ max.

$$\Delta I = \frac{V_{O1}}{L_1 \cdot F_S} \cdot \left(1 - \frac{V_{O1}}{V_{IN}}\right) = \frac{1.2V}{1.5\mu H \cdot 1.8MHz} \cdot \left(1 - \frac{1.2V}{4.2V}\right) = 317mA$$

$$I_{PK1} = I_{O1} + \frac{\Delta I}{2} = 1.5A + 0.317A = 1.817A$$

$$P_{L1} = I_{OUTBUCK}^2 \cdot DCR = 1.5A^2 \cdot 70m\Omega = 158mW$$

Channel 2 Inductor

$$L = \frac{0.75 \cdot V_O}{m} = \frac{0.75 \cdot 3.3V}{0.75\frac{A}{\mu s}} = 3.3\mu H$$

For TDK inductor TFC252008MBT, 3.3µH, DCR = 100mΩ max.

$$\Delta I = \frac{V_{O1}}{L_1 \cdot F_S} \cdot \left(1 - \frac{V_{O2}}{V_{IN}}\right) = \frac{3.3V}{3.3\mu H \cdot 1.8MHz} \cdot \left(1 - \frac{3.3V}{4.2V}\right) = 107mA$$

$$I_{PK1} = I_{O1} + \frac{\Delta I}{2} = 0.5A + 0.054A = 0.55A$$

$$P_{L1} = I_{OUTBUCK}^2 \cdot DCR = 0.55A^2 \cdot 100m\Omega = 30.1mW$$

Channel 1 Output Capacitor

V_{DROOP}= 0.12V

$$C_{OUT3} = \frac{3 \cdot \Delta I_{LOAD}}{V_{DROOP} \cdot F_S} = \frac{3 \cdot 1.5A}{0.12V \cdot 1.8MHz} = 20.8\mu F; \text{ use } 22\mu F$$

$$I_{RMS(MAX)} = \frac{1}{2 \cdot \sqrt{3}} \cdot \frac{V_{OUT} \cdot (V_{IN(MAX)} - V_{OUT})}{L \cdot F_S \cdot V_{IN(MAX)}} = \frac{1}{2 \cdot \sqrt{3}} \cdot \frac{1.2V \cdot (4.2V - 1.2V)}{1.5\mu H \cdot 1.8MHz \cdot 4.2V} = 92mA$$

$P_{ESR} = ESR \cdot I_{RMS}^2 = 5m\Omega \cdot 24mA^2 = 3\mu W$

Channel 2 Output Capacitor

V_{DROOP}= 0.1V

$$C_{OUT3} = \frac{3 \cdot \Delta I_{LOAD}}{V_{DROOP} \cdot F_S} = \frac{3 \cdot 0.5A}{0.1V \cdot 2MHz} = 7.5\mu F; \text{ use } 10\mu F$$

$$I_{RMS(MAX)} = \frac{1}{2 \cdot \sqrt{3}} \cdot \frac{V_{OUT} \cdot (V_{IN(MAX)} - V_{OUT})}{L \cdot F_S \cdot V_{IN(MAX)}} = \frac{1}{2 \cdot \sqrt{3}} \cdot \frac{3.3V \cdot (4.2V - 3.3V)}{3.3\mu H \cdot 2MHz \cdot 4.2V} = 30mA$$

$P_{ESR} = ESR \cdot I_{RMS}^2 = 5m\Omega \cdot 30mA^2 = 4.5\mu W$

Input Capacitor

Input Ripple V_{PP1} = 50mV, V_{PP2} = 25mV

$$C_{IN1} = \frac{1}{\left(\frac{V_{PP1}}{I_{O1}} - ESR\right) \cdot 4 \cdot F_S} = \frac{1}{\left(\frac{50mV}{1.5A} - 5m\Omega\right) \cdot 4 \cdot 1.8MHz} = 4.9\mu F$$

$$C_{IN2} = \frac{1}{\left(\frac{V_{PP2}}{I_{O2}} - ESR\right) \cdot 4 \cdot F_S} = \frac{1}{\left(\frac{25mV}{0.5A} - 5m\Omega\right) \cdot 4 \cdot 2MHz} = 3\mu F$$

$C_{IN} = C_{IN1} + C_{IN2}$ = 4.9µF+3µF= 7.9µF; use 10µF

$$I_{RMS(MAX)} = \frac{I_{O1} + I_{O2}}{2} = 1A$$

$P = ESR \cdot I_{RMS}^2 = ESR \cdot (1A)^2 = 5mW$

AAT2789 Losses

Total loss can be estimated by calculating the dropout ($V_{IN} = V_O$) losses where the power MOSFETs $R_{DS\ (ON)}$ will be at the maximum value. All values assume an 85°C ambient temperature and a 120°C junction temperature with the TDFN 50°C/W package.

$$P_{TOTAL} = I_{O1}^2 \cdot R_{DS(ON)H1} + I_{Q1} \cdot V_{IN1} + I_{O2}^2 \cdot R_{DS(ON)H2} + I_{Q2} \cdot V_{IN2}$$

$$P_{TOTAL} = 1.5A^2 \cdot 120m\Omega + 70\mu A \cdot 4.2 + 0.5^2 \cdot R_{DS(ON)H2} + 70\mu A \cdot 4.2V = 270mW$$

$$T_{J(MAX)} = T_{AMB} + \Theta_{JA} \cdot P_{LOSS} = 85°C + (50°C/W) \cdot 270mW = 99°C$$

Ordering Information

Package	Output Voltage		Marking[1]	Part Number (Tape and Reel)[2]
	Channel 1	Channel 2		
TDFN34-16	Adjustable (0.6)	Adjustable (0.6)	3JXYY	**AAT2789IRN-AA-T1**

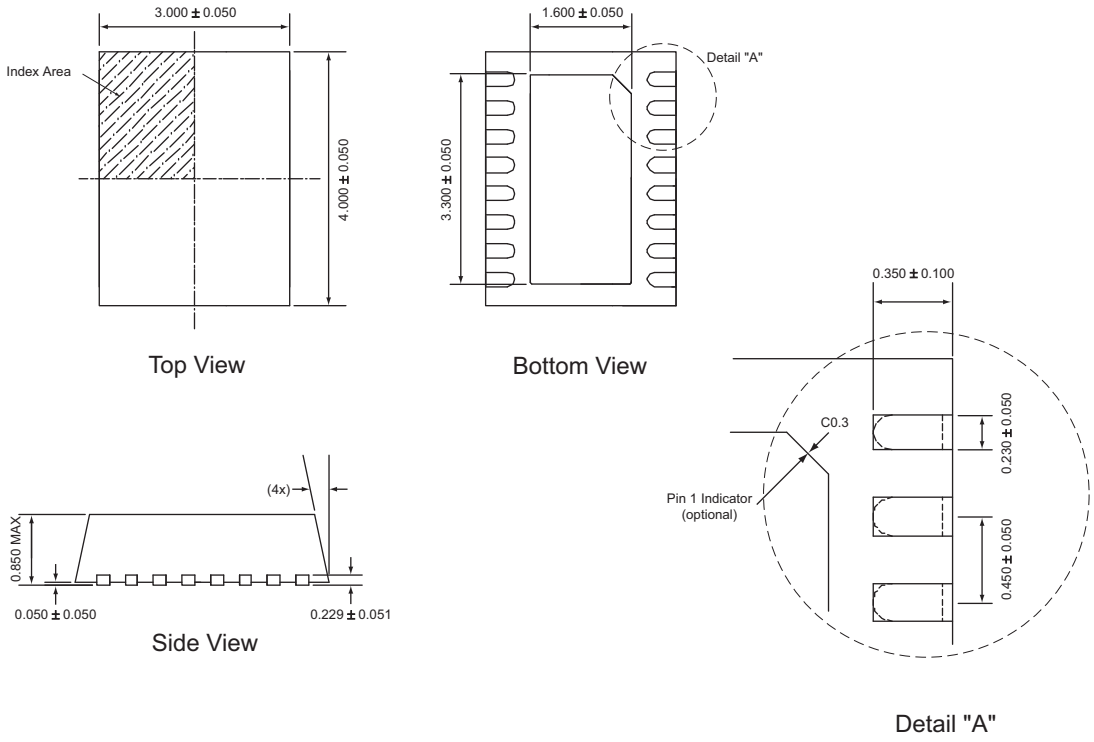
All AnalogicTech products are offered in Pb-free packaging. The term "Pb-free" means semiconductor products that are in compliance with current RoHS standards, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. For more information, please visit our website at http://www.analogictech.com/about/quality.aspx.

Legend	
Output Voltage	Code
Adjustable (0.6)	A

1. XYY = assembly and date code.
2. Sample stock is generally held on part numbers listed in BOLD.

Package Information[1]

TDFN34-16



All dimensions in millimeters.

1. The leadless package family, which includes QFN, TQFN, DFN, TDFN and STDFN, has exposed copper (unplated) at the end of the lead terminals due to the manufacturing process. A solder fillet at the exposed copper edge cannot be guaranteed and is not required to ensure a proper bottom solder connection.

Advanced Analogic Technologies, Inc.
3230 Scott Boulevard, Santa Clara, CA 95054
Phone (408) 737-4600
Fax (408) 737-4611