AAT2786

SystemPower™

1.5A Step-Down Converter and 150mA LDO

General Description

The AAT2786 is a dual output power solution. It includes a 1.5A, 1.4MHz, high-efficiency step-down converter and a high performance 150mA LDO regulator. The step-down regulator output voltage is adjustable from 0.6V to V_{IN}. The LDO regulator has a factory preset fixed output voltage from 1.2V to 3.3V.

The step-down converter consumes only 42µA of no-load quiescent current and is designed to maintain high efficiency throughout the load range. The step-down converter has ultra-low $R_{DS(ON)}$ integrated MOSFETs and can operate up to 100% duty cycle to enable high output voltage, high current applications which require a low dropout threshold. The AAT2786 provides excellent transient response and high output accuracy across the operating range. Pulling the MODE/SYNC pin high enables "PWM Only" mode, maintaining constant frequency and low output ripple across the operating range. Alternatively, the converter may be synchronized to an external clock input via the MODE/SYNC pin.

The MicroPower low dropout linear regulator in the AAT2786 has been specifically designed for high-speed turn-on and turn-off performance, fast transient response, and good noise and power supply ripple rejection (PSRR), making it ideal for powering sensitive circuits with fast switching requirements.

Over-temperature and short-circuit protection safeguard the AAT2786 and system components from damage.

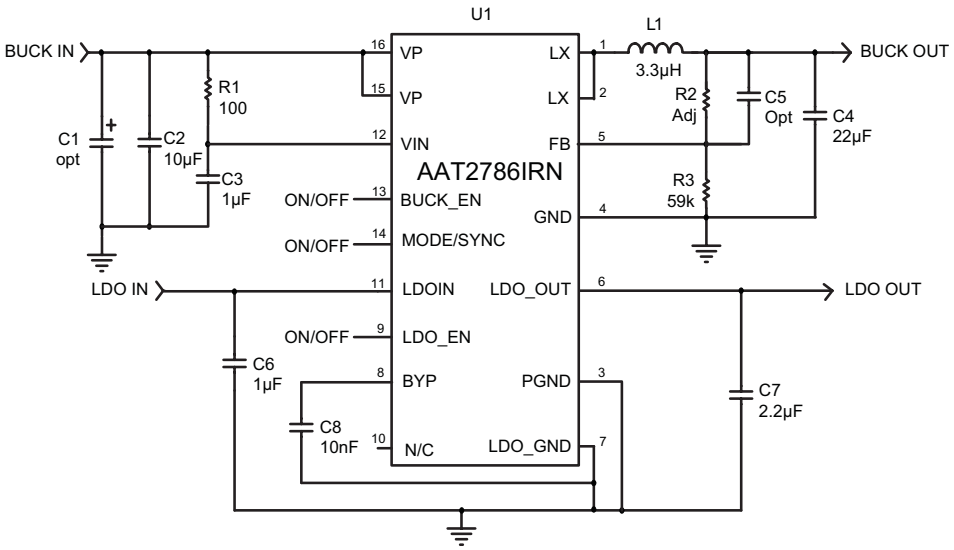
Features

- V_{IN} Range : 2.5V to 5.5V
- 1.5A Step-Down Converter
  - V_{OUT} Range: 0.6V to V_{IN}
  - 95% Peak Efficiency
  - High Efficiency across load range
  - 42µA No Load Quiescent Current
  - Optional "PWM Only" Low Noise Mode
  - Current limit and soft start
- 150mA LDO Regulator
  - V_{OUT} Range: 1.2V to 3.3V (Fixed)
  - High Power Supply Rejection Ratio
  - Low Output Noise
- Independent Enable Pins
- Integrated Power MOSFETs
- Over-Temperature Protection
- TDFN34-16 Package
- -40°C to +85°C Temperature Range

Applications

- Cellular and Smart Phones
- PDAs, Palmtops
- Digital Still and Video Cameras
- Portable Instruments
- Battery-Powered Applications

Typical Application

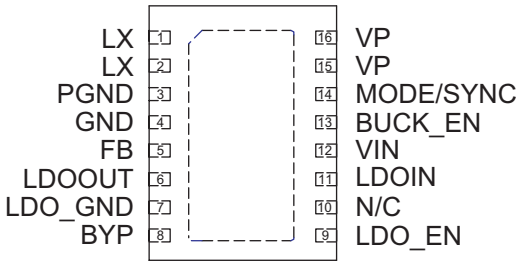


Pin Descriptions

Pin #	Symbol	Description
1, 2	LX	Step-down converter switching node. Connect the output inductor to this pin. The switching node is internally connected to the drain of both high- and low-side MOSFETs.
3	PGND	Step-down converter main power ground return pin. Connect to the output and input capacitor return.
4	GND	Non-power signal ground pin.
5	FB	Step-down converter feedback input pin. This pin is connected either directly to the converter output or to an external resistive divider for an adjustable output.
6	LDOOUT	LDO output pin; should be decoupled with 2.2µF ceramic capacitor.
7	LDO_GND	LDO ground connection pin.
8	BYP	LDO bypass capacitor connection; to improve AC ripple rejection, connect a 10nF capacitor to GND. This will also provide a soft start function.
9	LDO_EN	LDO enable pin; this pin should not be left floating. When pulled low, the LDO PMOS pass transistor turns off and all internal circuitry enters low-power mode, consuming less than 1µA.
10	N/C	Open
11	LDOIN	LDO input voltage pin; should be decoupled with 1µF or greater capacitor.
12	VIN	Step-down converter power supply. Supplies power for the internal circuitry.
13	BUCK_EN	Step-down converter enable pin. A logic low disables the step-down converter and it consumes less than 1µA of current. When connected high, it resumes normal operation.
14	MODE/SYNC	Connect to ground for Light-Load/PWM mode and optimized efficiency throughout the load range. Connect high for low noise PWM operation under all operating conditions. Connect to an external clock for synchronization (PWM only).
15,16	VP	Step-down converter input voltage for the power switches.

Pin Configuration

TDFN34-16
(Top View)



Absolute Maximum Ratings

T_A = 25°C unless otherwise noted.

Symbol	Description	Value	Units
V_{IN}	VIN, VP to GND	6.0	V
V_{LX}	LX Pin to GND	-0.3 to V_{IN} + 0.3	
V_{FB}	FB Pin to GND	-0.3 to V_{IN} + 0.3	
V_N	MODE/SYNC, BUCK_EN to GND	-0.3 to 6.0	
V_{LDOIN}	VLDOIN to LDO_GND	6.0	
$V_{ENIN(MAX)}$	LDO_EN to LDO_GND	-0.3 to V_{IN} + 0.3	
T_J	Maximum Junction Operating Temperature	-40 to +150	°C
T_{LEAD}	Maximum Soldering Temperature (at leads, 10 sec)	300	

Thermal Information

Symbol	Description	Value	Units
P_D	Maximum Power Dissipation[1]	2.0	W
θ_{JA}	Thermal Resistance	50	°C/W
V_{LDOIN}	LDO Input Voltage	(V_{LDOUT} + V_{DO}) to 5.5	V

1. Derate 20mW/ºC above 25°C ambient temperature. Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation at conditions other than the operating conditions specified is not implied.
2. Mounted on an FR4 board.
3. To calculate minimum input voltage, use the following equation: $V_{IN(MIN)} = V_{OUT(MAX)} + V_{DO(MAX)}$ as long as $V_{IN} \geq 2.5V$.

Electrical Characteristics[1]

V_{IN}=3.6V; T_A = -40°C to 85°C unless otherwise noted. Typical values are at T_A = 25°C.

Symbol	Description	Conditions	Min	Typ	Max	Units
Step-Down Converter						
V_{IN}	Input Voltage		2.5		5.5	V
V_{OUT}	Output Voltage Range		0.6		V_{IN}	V
V_{UVLO}	UVLO Threshold	V_{IN} Rising			2.5	V
		Hysteresis		150		mV
		V_{IN} Falling	1.7			V
V_{OUT}	Output Voltage Tolerance	I_{OUT} = 0A to 1.5A, V_{IN} = 2.4V to 5.5V	-3.0		3.0	%
I_Q	Quiescent Current	No Load		42	90	µA
I_{SHDN}	Shutdown Current	V_{EN} = GND			1.0	µA
I_{LIM}	Current Limit		1.8			A
$R_{DS(ON)H}$	High Side Switch On-Resistance			0.120		Ω
$R_{DS(ON)L}$	Low Side Switch On-Resistance			0.085		Ω
I_{LXLEAK}	LX Leakage Current	V_{IN} = 5.5V, V_{LX} = 0 to VIN			1.0	µA
$\Delta V_{LOADREG}$	Load Regulation	I_{LOAD} = 0A to 1.5A		0.5		%
$\Delta V_{LINEREG}/\Delta V_{IN}$	Line Regulation	V_{IN} = 2.4V to 5.5V		0.2		%/V
V_{FB}	Feedback Threshold Voltage Accuracy (Adjustable Version)	No Load, T_A = 25°C	0.591	0.60	0.609	V
I_{FB}	FB Leakage Current	V_{OUT} = 1.0V			0.2	µA
F_{OSC}	Internal Oscillator Frequency	T_A = 25°C	1.12	1.4	1.68	MHz
	Synchronous Clock		0.60		3.0	
T_S	Start-Up Time	From Enable to Output Regulation		150		µs
T_{SD}	Over-Temperature Shutdown Threshold			140		°C
T_{HYS}	Over-Temperature Shutdown Hysteresis			15		°C
MODE/SYNC						
$V_{MODE/SYNC(L)}$	Enable Threshold Low				0.6	V
$V_{MODE/SYNC(H)}$	Enable Threshold High		1.4			V
$I_{MODE/SYNC}$	Enable Leakage Current	V_{IN} = V_{EN} = 5.5V			1.0	µA

1. The AAT2786 is guaranteed to meet performance specifications over the -40°C to +85°C operating temperature range and is assured by design, characterization, and correlation with statistical process controls.

Electrical Characteristics (continued)

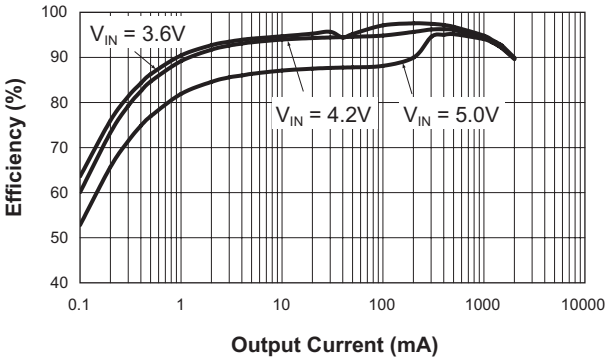
V_{LDOIN} = $V_{OUT(NOM)}$ + 1V for V_{OUT} options greater than 1.5V. V_{IN} = 2.5 for V_{OUT} ≤1.5V. I_{OUT} = 1mA, C_{OUT} = 2.2µF, C_{IN} = 1µF, T_A = -40°C to +85°C, unless otherwise noted. Typical values are T_A = 25°C.

Symbol	Description	Conditions		Min	Typ	Max	Units
LDO Regulator							
V_{LDOOUT}	Output Voltage Tolerance	I_{LDOOUT} = 1mA to 150mA	T_A = 25°C	-1.5		1.5	%
			T_A = -40°C to 85°C	-2.5		2.5	
I_{LDOOUT}	Output Current	V_{LDOOUT} > 1.2V		150			mA
V_{DO}	Dropout Voltage[2, 3]	I_{LDOOUT} = 150mA			200	300	mV
I_{SC}	Short-Circuit Current	V_{LDOOUT} < 0.4V			600		mA
I_Q	Ground Current	V_{IN} = 5V, No Load, EN = V_{IN}			70	125	µA
I_{SD}	Shutdown Current	V_{IN} = 5V, EN = 0V				1	µA
$\Delta V_{OUT}/V_{OUT}*\Delta V_{IN}$	Line Regulation	V_{IN} = V_{OUT} + 1 to 5.0V				0.09	%/V
$\Delta V_{OUT(line)}$	Dynamic Line Regulation	V_{IN} = V_{LDOOUT} + 1V to V_{LDOOUT} + 2V, I_{LDOOUT} = 150mA, T_R/T_F = 2µs			2.5		mV
$\Delta V_{OUT(load)}$	Dynamic Load Regulation	I_{LDOOUT} = 1mA to 150mA, T_R < 5µs			30		mV
PSRR	Power Supply Rejection Ratio	I_{LDOOUT} = 10mA, C_{BYP} = 10nF	1 kHz		67		dB
			10kHz		47		
			1MHz		45		
e_N	Output Noise	Noise Power BW = 300Hz - 50kHz			50		µVrms
T_{SD}	Over-Temperature Shutdown Threshold				145		°C
T_{HYS}	Over-Temperature Shutdown Hysteresis				12		°C
T_C	Output Voltage Temperature Coefficient				22		ppm/°C
Enable							
V_{IL}	Enable Threshold Low					0.6	V
V_{IH}	Enable Threshold High			1.4			V
I_{EN_BUCK}	Enable Leakage Current	V_{EN_BUCK} = 5V				1	µA
I_{EN_LDO}	Enable Leakage Current	V_{EN_LDO} = 5V				1.0	µA
t_{ENDLY}	Enable Delay Time	BYP = Open			15		µs

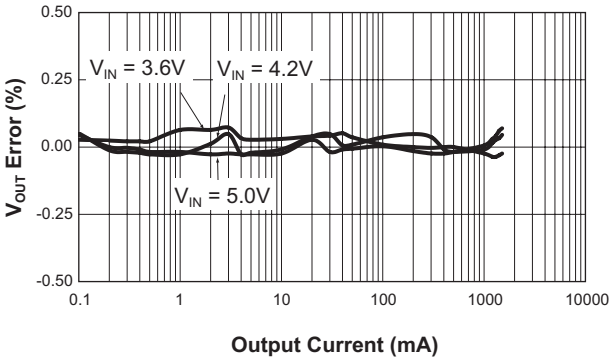
1. V_{DO} is defined as V_{LDOIN} - V_{LDOOUT} when V_{LDOOUT} is 98% of nominal.
2. For V_{LDOOUT} < 2.3V, V_{DO} = 2.5V - V_{LDOOUT}.

Typical Characteristics–Step-Down Converter

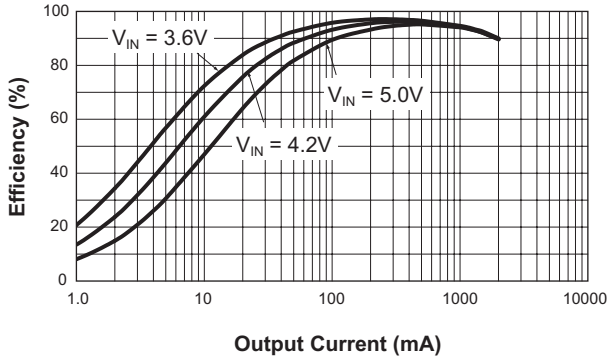
Efficiency vs. Output Current
(Light-Load Mode; V_{OUT} = 3.3V)



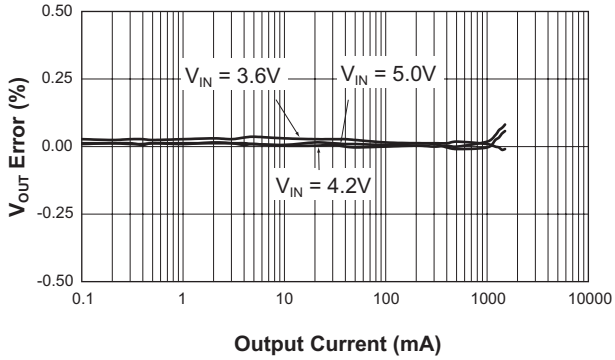
Load Regulation
(Light-Load Mode; V_{OUT} = 3.3V)



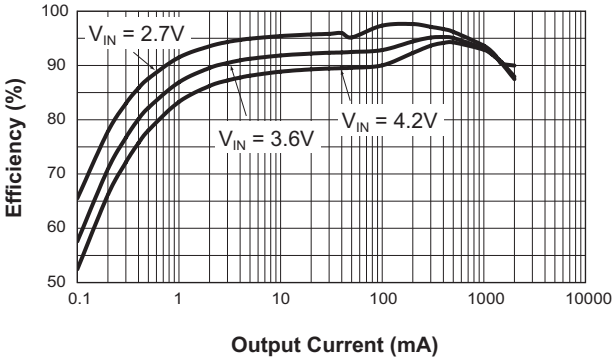
Efficiency vs. Output Current
(PWM Mode; V_{OUT} = 3.3V)



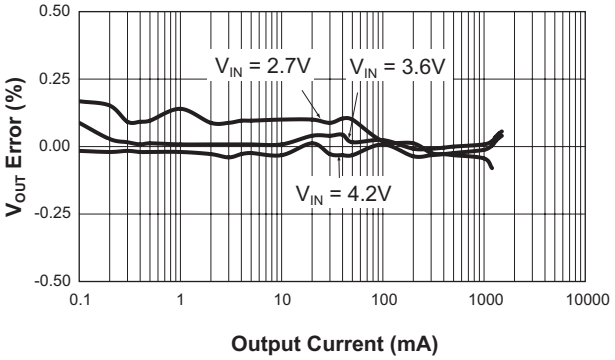
Load Regulation
(PWM Mode; V_{OUT} = 3.3V)



Efficiency vs. Output Current
(Light-Load Mode; V_{OUT} = 2.5V)

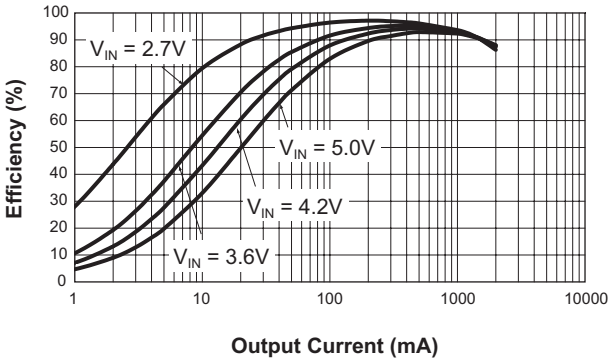


Load Regulation
(Light-Load Mode; V_{OUT} = 2.5V)

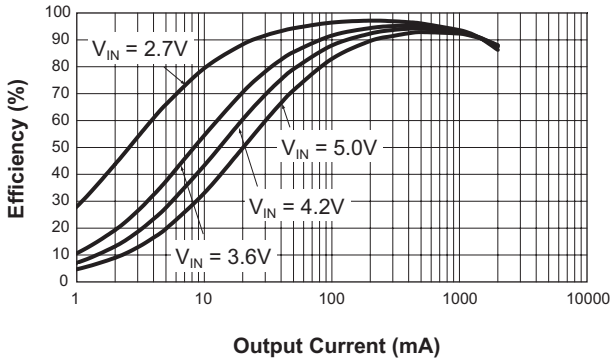


Typical Characteristics–Step-Down Converter

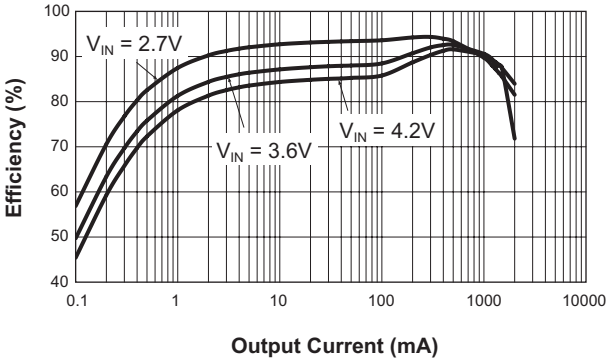
Efficiency vs. Output Current
(PWM Mode; V_{OUT} = 2.5V)



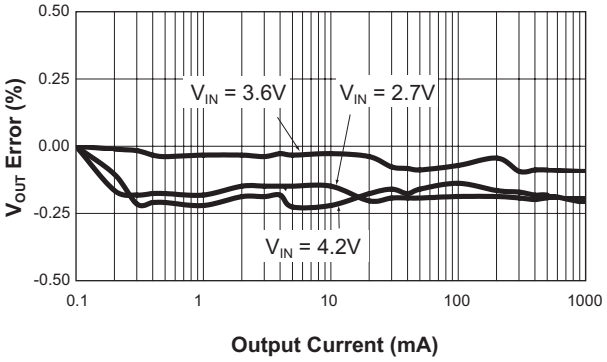
Efficiency vs. Output Current
(PWM Mode; V_{OUT} = 2.5V)



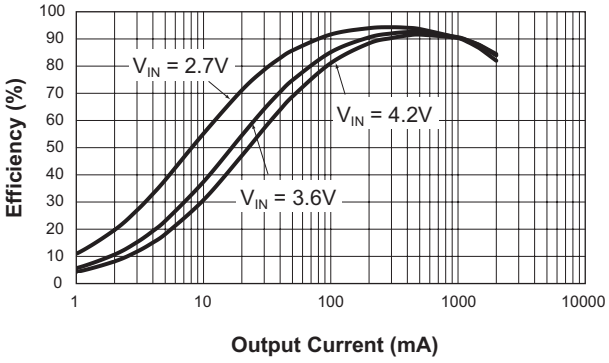
Efficiency vs. Output Current
(Light-Load Mode; V_{OUT} = 1.8V)



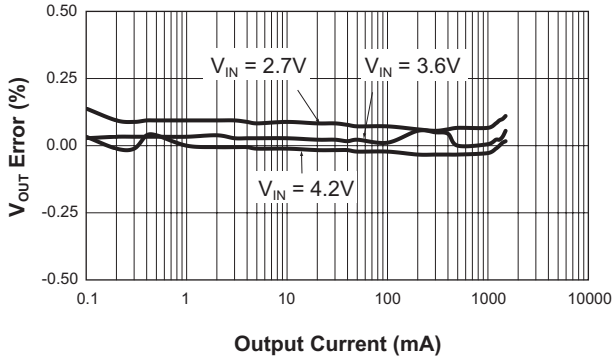
Load Regulation
(Light-Load Mode; V_{OUT} = 1.8V)



Efficiency vs. Output Current
(PWM Mode; V_{OUT} = 1.8V)

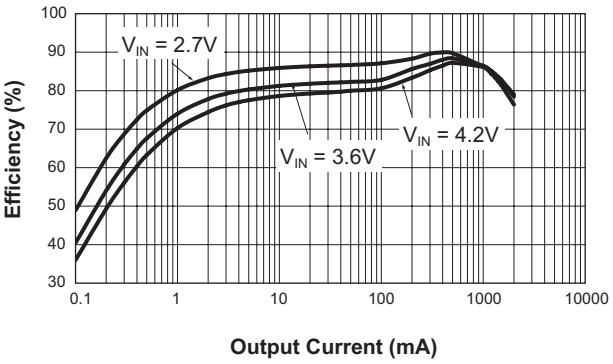


Load Regulation
(PWM Mode; V_{OUT} = 1.8V)

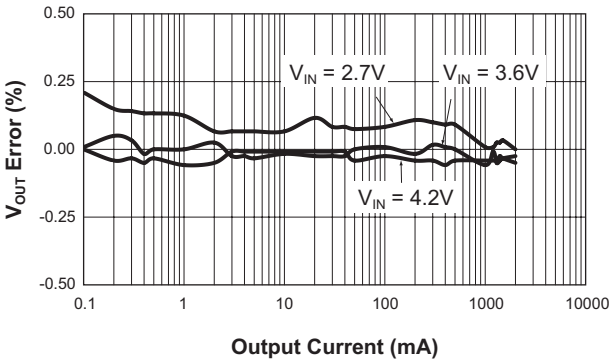


Typical Characteristics–Step-Down Converter

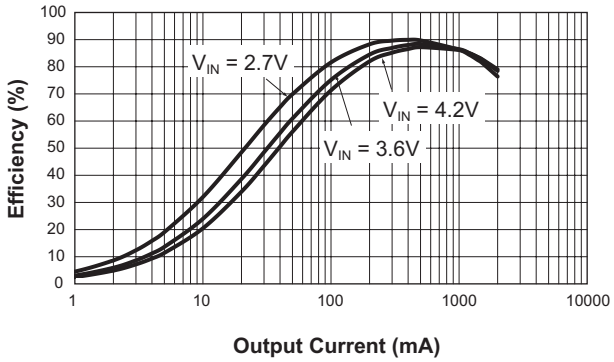
Efficiency vs. Output Current
(Light-Load Mode; V_{OUT} = 1.2V)



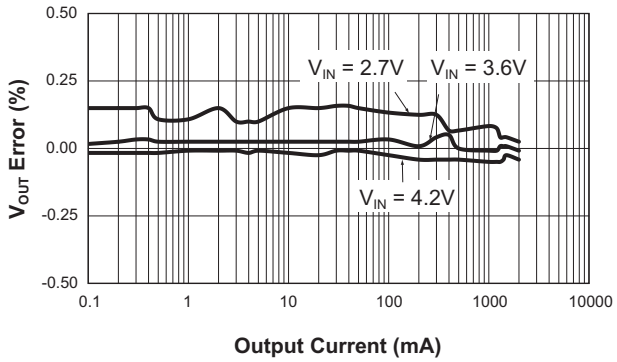
Load Regulation
(Light-Load Mode; V_{OUT} = 1.2V)



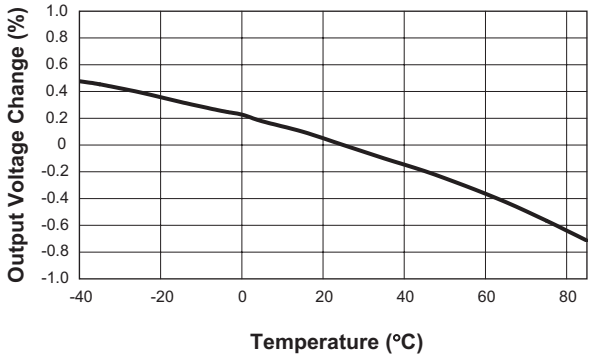
Efficiency vs. Output Current
(PWM Mode; V_{OUT} = 1.2V)



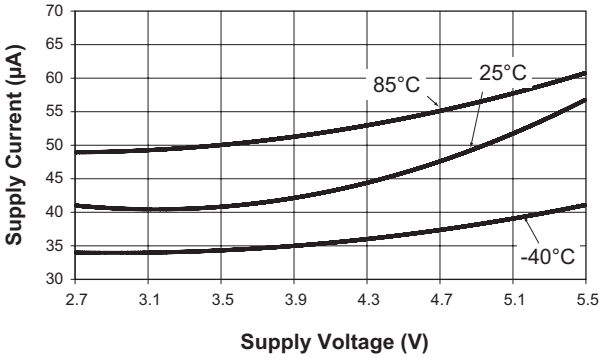
Load Regulation
(PWM Mode; V_{OUT} = 1.2V)



Output Voltage vs. Temperature
(V_{IN} = 3.6V; V_{OUT} = 1.8V; I_{OUT} = 1A)

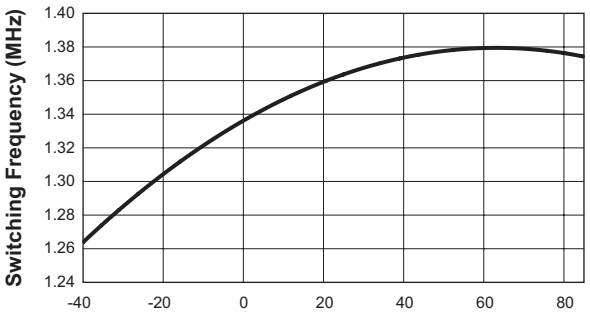


Supply Current vs. Supply Voltage
(V_{OUT} = 1.8V; No Load; Light-Load Mode)

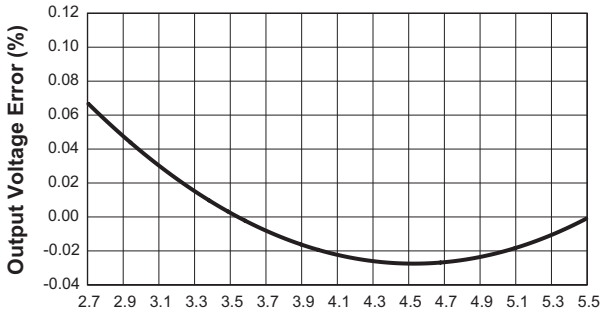


Typical Characteristics–Step-Down Converter

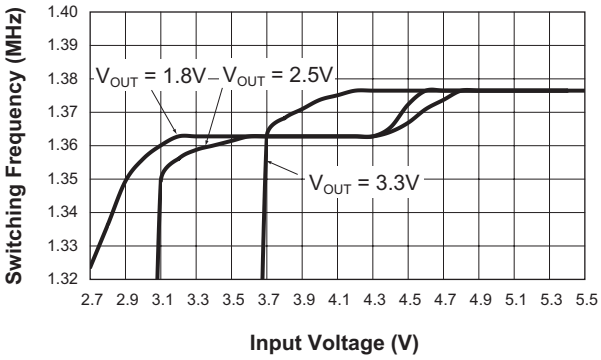
Switching Frequency vs. Temperature
(V_{IN} = 3.6V; V_{OUT} = 1.8V; I_{OUT} = 1A)



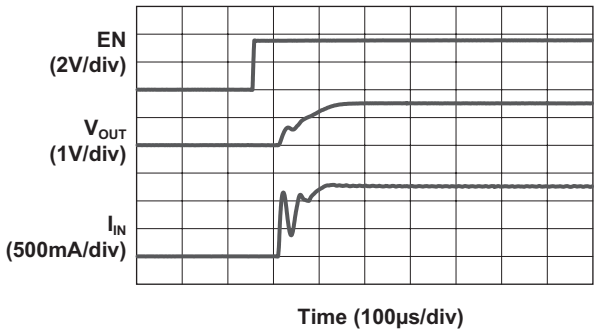
Line Regulation
(V_{OUT} = 1.8V; I_{OUT} = 1A)



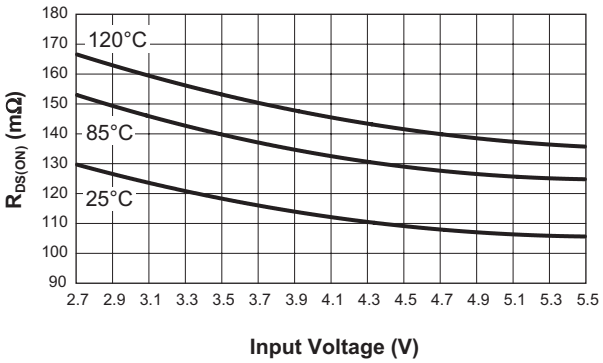
Switching Frequency vs. Input Voltage
(I_{OUT} = 1A)



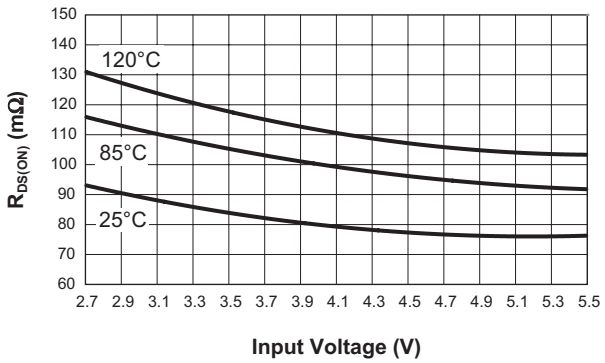
Enable Soft Start
(V_{OUT} = 3.6V; I_{OUT} = 1.5A)



P-Channel $R_{DS(ON)}$ vs. Input Voltage

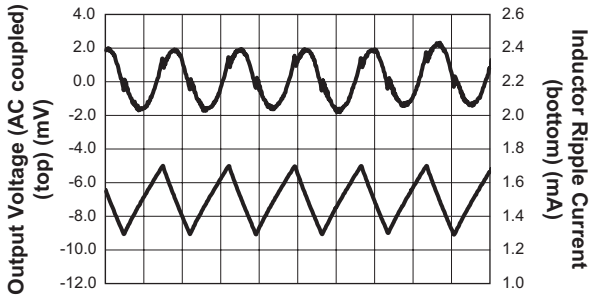


N-Channel $R_{DS(ON)}$ vs. Input Voltage

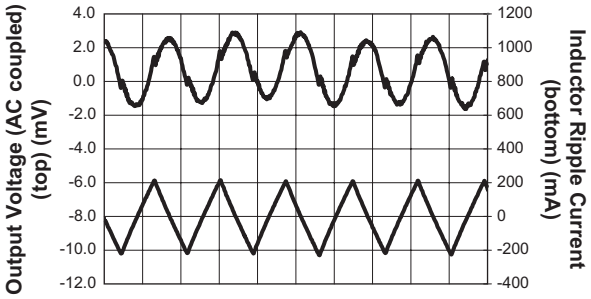


Typical Characteristics–Step-Down Converter

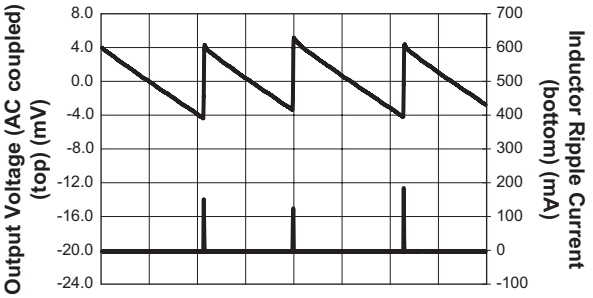
Heavy Load Switching Waveform
(V_{IN} = 3.6V; V_{OUT} = 1.8V; 1.5A Load)



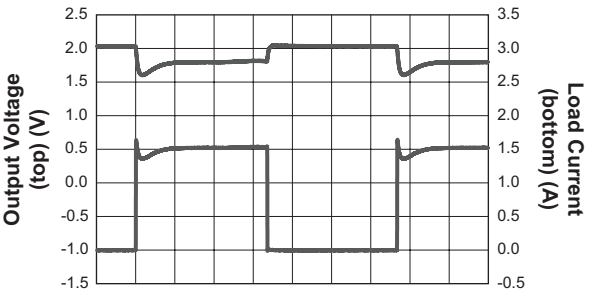
Light Load Switching Waveform
(V_{IN} = 3.6V; V_{OUT} = 1.8V; 1mA Load)



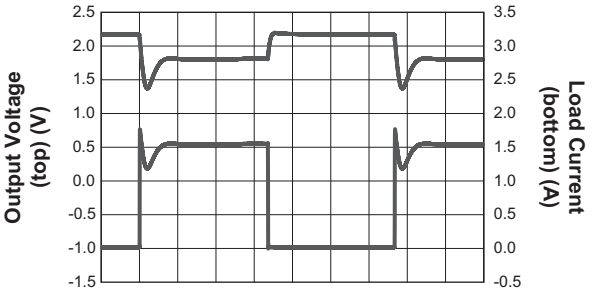
Light Load Switching Waveform
(Light-Load Mode; V_{IN} = 3.6V; V_{OUT} = 1.8V; 1mA Load)



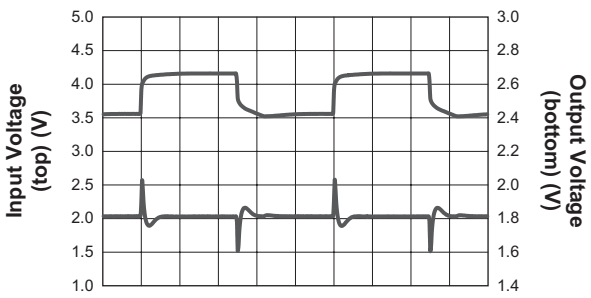
Load Transient Response
(V_{IN} = 3.6V; V_{OUT} = 1.8V; C_{FF} = 100pF)



Load Transient Response
(V_{IN} = 3.6V; V_{OUT} = 1.8V; No C_{FF})

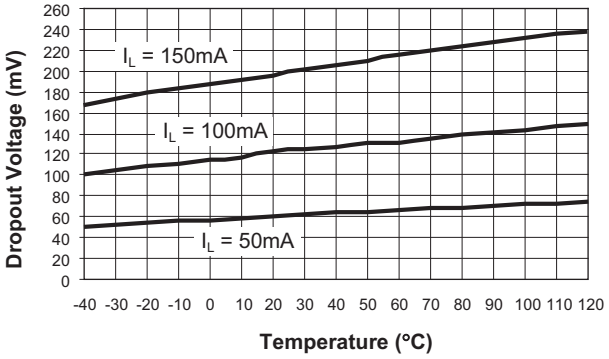


Line Transient Response
(V_{OUT} = 1.8V; 1.5A Load)

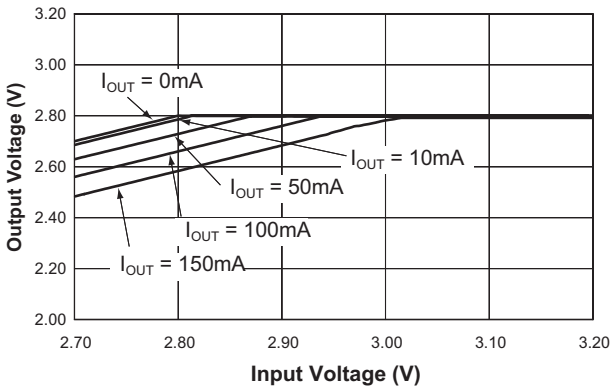


Typical Characteristics–LDO

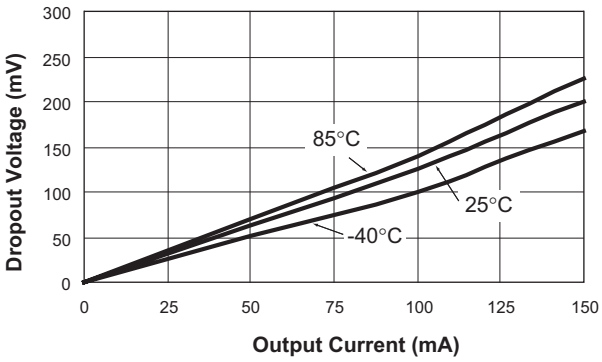
Dropout Voltage vs. Temperature



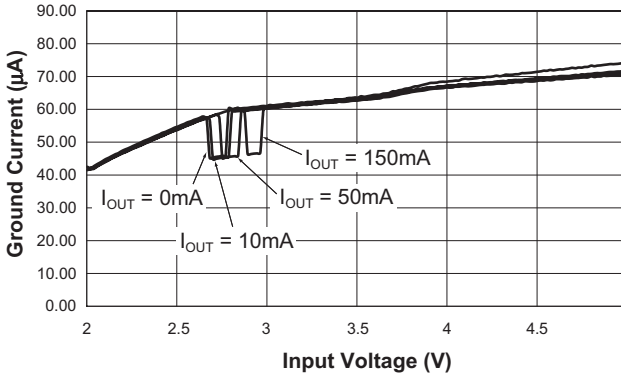
Dropout Characteristics



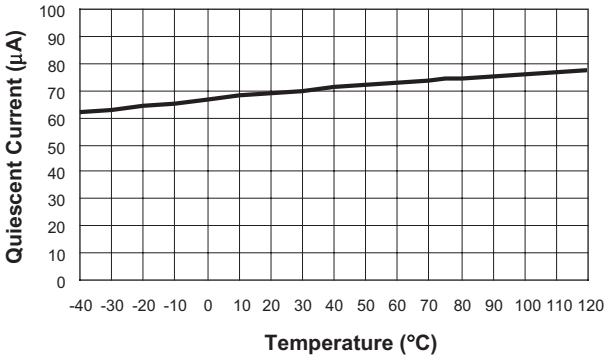
Dropout Voltage vs. Output Current



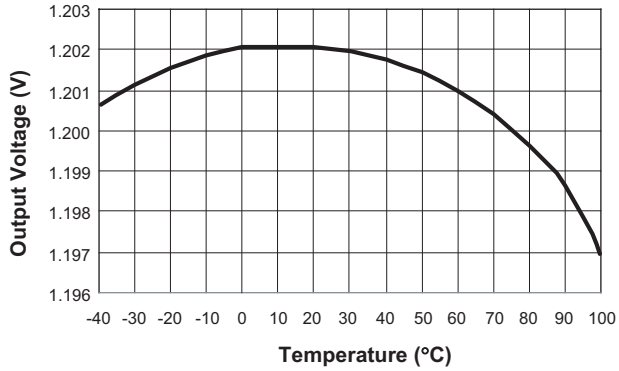
Ground Current vs. Input Voltage



Quiescent Current vs. Temperature

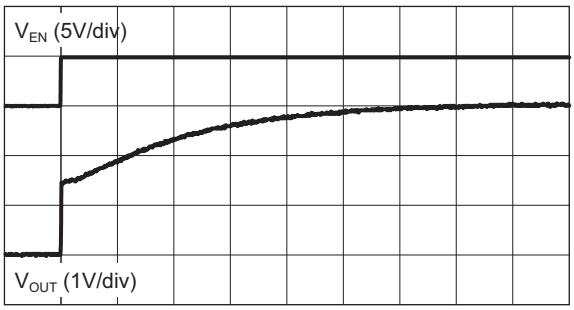


Output Voltage vs. Temperature



Typical Characteristics–LDO

Initial Power-Up Response Time
(C_{BYP} = 10nF)

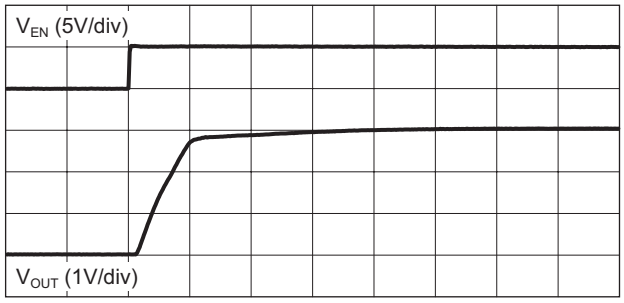


Time (400µs/div)

Turn-Off Response Time
(C_{BYP} = 10nF)

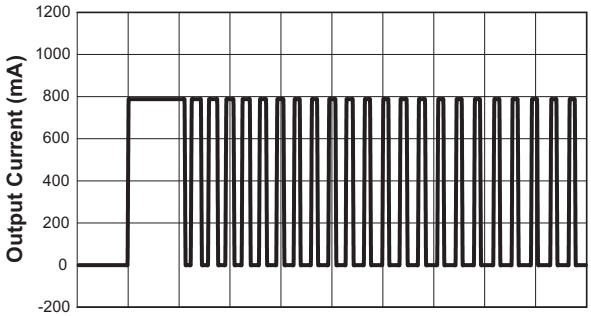
Time (50µs/div)

Turn-On Time From Enable (V_{IN} present)
(C_{BYP} = 10nF)



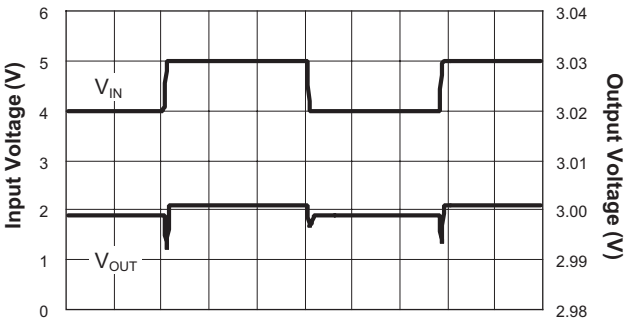
Time (5µs/div)

Over-Current Protection



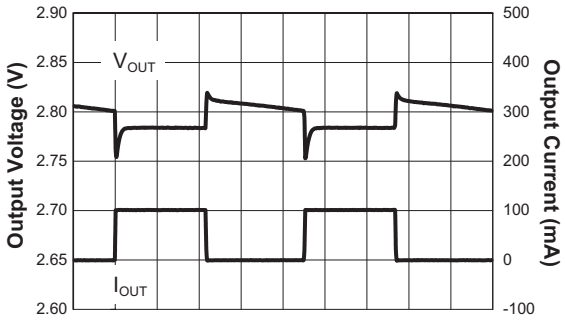
Time (20ms/div)

Line Transient Response



Time (100µs/div)

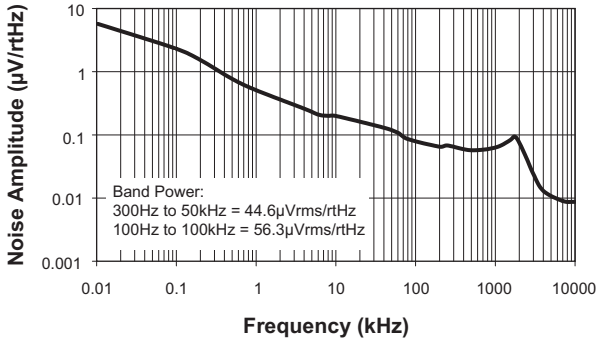
Load Transient Response



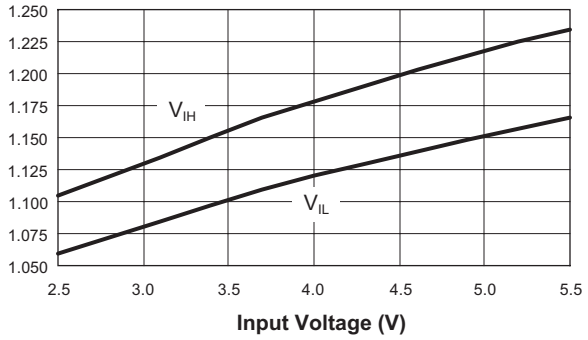
Time (100µs/div)

Typical Characteristics–LDO

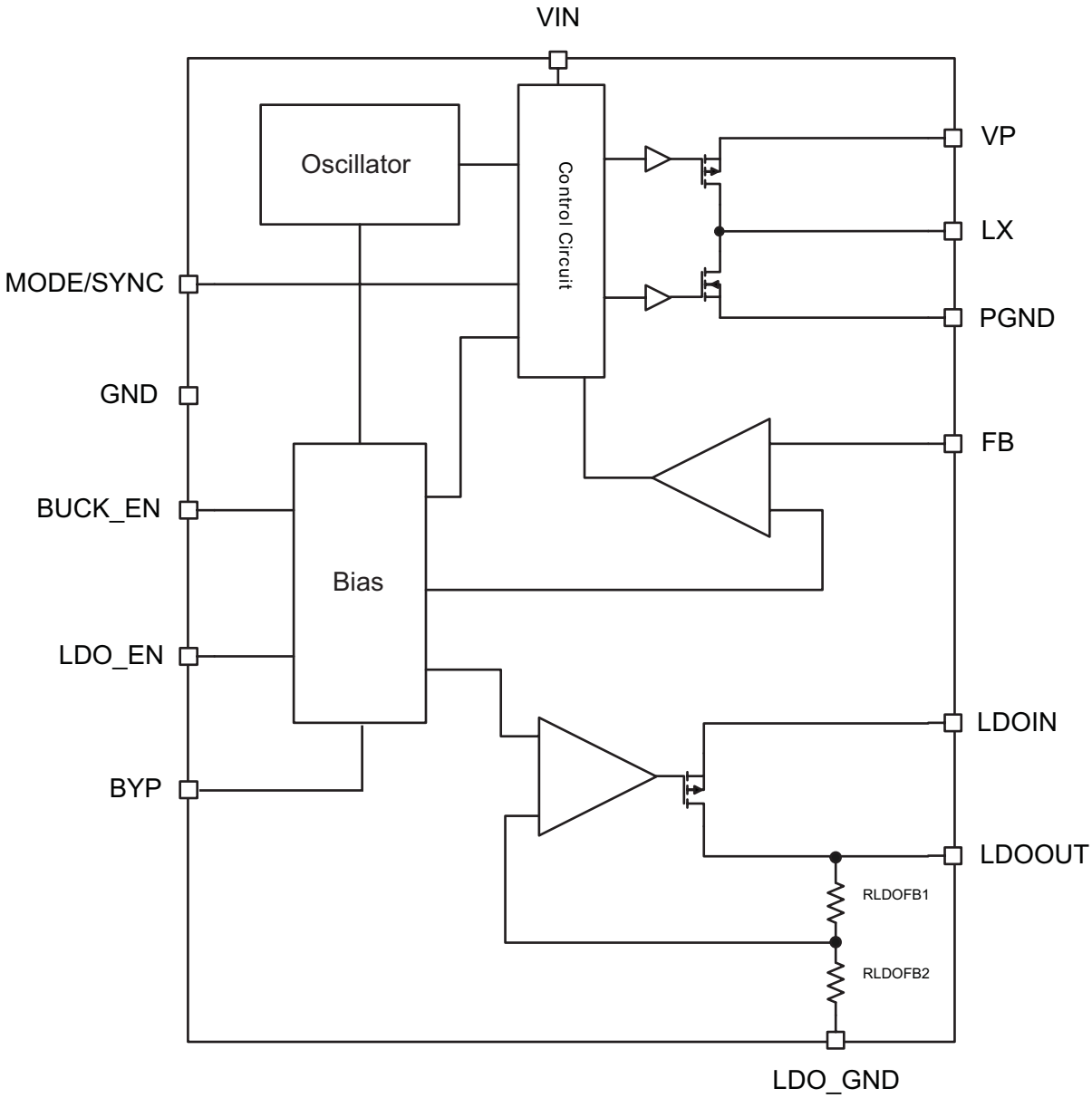
AAT2786 Self Noise
(C_{OUT} = 10µF, ceramic)



V_{IH} and V_{IL} vs. V_{IN}



Functional Block Diagram



Functional Description

The AAT2786 is a dual output power solution. It includes a 1.5A, 1.4MHz, high-efficiency step-down converter and a high performance 150mA LDO regulator. The step-down regulator output voltage is adjustable from 0.6V to V_{IN}. The LDO regulator has a factory preset fixed output voltage from 1.2V to 3.3V. The on and off states of the step-down converter and the LDO regulator are independently controlled by separate enable pins.

Step-Down Converter

The step-down converter in the AAT2786 is a high performance 1.5A monolithic step-down converter operating at 1.4MHz switching frequency. It minimizes external component size and optimizes efficiency over the complete load range. Apart from the small bypass input capacitor, only a small L-C filter is required at the output. Typically, a 3.3µH inductor and a 22µF ceramic capacitor are recommended for a 3.3V output (see table of recommended values).

At dropout, the step-down converter duty cycle increases to 100% and the output voltage tracks the input voltage minus the $R_{DS(ON)}$ drop of the P-channel high side MOSFET (plus the DC drop of the external inductor). The device integrates extremely low $R_{DS(ON)}$ MOSFETs to achieve low dropout voltage during 100% duty cycle operation. This is advantageous in applications requiring high output voltages (typically > 2.5V) at low input voltages.

The integrated low-loss MOSFET switches can provide greater than 95% efficiency at full load. Light-Load operation maintains high efficiency under light load conditions (typically <150mA). The MODE/SYNC pin allows optional "PWM only" mode. This maintains constant frequency and low output ripple across all load conditions. Alternatively, the IC can be synchronized to an external clock via the MODE/ SYNC input. External synchronization is maintained between 0.6MHz and 3.0MHz.

In battery-powered applications, as V_{IN} decreases, the converter dynamically adjusts the operating frequency prior to dropout to maintain the required duty cycle and provide accurate output regulation. Output regulation is maintained until the dropout voltage, or minimum input voltage, is reached. At 1.5A output load, dropout voltage headroom is approximately 200mV.

The step-down converter in the AAT2786 typically achieves better than ±0.5% output regulation across the input voltage and output load range. A current limit of 2.0A (typical) protects the IC and system components from short-circuit damage. Typical no load quiescent current is 42µA.

Thermal protection completely disables switching when the maximum junction temperature is detected. The junction over-temperature threshold is 140°C with 15°C of hysteresis. Once an over-temperature or over-current fault condition is removed, the output voltage automatically recovers.

Peak current mode control and optimized internal compensation provide high loop bandwidth and excellent response to input voltage and fast load transient events. Soft start eliminates output voltage overshoot when the step-down converter is enabled. Under-voltage lockout prevents spurious start-up events.

Control Loop

The step-down converter in the AAT2786 is a peak current mode step-down converter. The current through the P-channel MOSFET (high side) is sensed for current loop control, as well as short-circuit and overload protection. A fixed slope compensation signal is added to the sensed current to maintain stability for duty cycles greater than 50%. The peak current mode loop appears as a voltage-programmed current source in parallel with the output capacitor.

The output of the voltage error amplifier programs the current mode loop for the necessary peak switch current to force a constant output voltage for all load and line conditions. Internal loop compensation terminates the transconductance voltage error amplifier output. The reference voltage is internally set to program the converter output voltage greater than or equal to 0.6V.

Soft Start / Enable

Soft start limits the current surge seen at VIN and eliminates output voltage overshoot. When EN_BUCK input is pulled low the step-down converter is forced into a low-power, non-switching state. The total input current during shutdown is less than 1µA.

Current Limit and Over-Temperature Protection

For overload conditions, the peak input current in the step-down converter is limited. To minimize power dissipation and stresses under current limit and short-circuit conditions, switching is terminated after entering current limit for a series of pulses. Switching is terminated for seven consecutive clock cycles after a current limit has been sensed for a series of four consecutive clock cycles. Thermal protection completely disables switching when internal dissipation becomes excessive. The junction over-temperature threshold is 140°C with 15°C of hysteresis. Once an over-temperature or over-current fault conditions is removed, the output voltage automatically recovers.

Under-Voltage Lockout

Internal bias of all circuits is controlled via the VIN input. Under-voltage lockout (UVLO) in the step-down converter guarantees sufficient VIN bias and proper operation of all internal circuitry prior to activation.

LDO Functional Description

The LDO regulator in the AAT2786 is intended for applications with output current load requirements from no load to 150mA. The advanced circuit design of the AAT2786 LDO regulator has been specifically optimized for very fast start-up and shutdown timing. This proprietary CMOS LDO has also been tailored for superior transient response characteristics. These traits are particularly important for applications that require fast power supply timing, such as GSM cellular telephone handsets.

The high-speed turn-on capability of the LDO regulator is enabled through the implementation of a fast start control circuit, which accelerates the turn-on behavior of fundamental control and feedback circuits. Fast turn-off response time is achieved by an active output pull-down circuit, which is enabled when the LDO regulator is placed in shutdown mode. This active fast shutdown circuit has no adverse effect on normal device operation.

The AAT2786 LDO regulator has very fast transient response characteristics, which is an important feature for applications in which fast line and load transient response are required. This rapid transient response behavior is accomplished through the implementation of an active error amplifier feedback control. This proprietary circuit design is unique to this MicroPower LDO regulator.

The LDO regulator output has been specifically optimized to function with low-cost, low-ESR ceramic capacitors. However, the design will allow for operation over a wide range of capacitor types.

A bypass pin has been provided to allow the addition of an optional voltage reference bypass capacitor to reduce output self noise and increase power supply ripple rejection. Device self noise and PSRR will be improved by the addition of a small ceramic capacitor to this pin. However, increased CBYPASS values may slow down the LDO regulator turn-on time.

Enable Function

The AAT2786 features an LDO regulator enable/ disable function. This pin (EN) is active high and is compatible with CMOS logic. To assure the LDO regulator will switch on, the EN turn-on control level must be greater than 1.5V. The LDO regulator will go into the disable shutdown mode when the voltage on the EN pin falls below 0.6V. If the enable function is not needed in a specific application, it may be tied to V_{IN} to keep the LDO regulator in a continuously on state.

When the LDO regulator is in shutdown mode, an internal 1.5kΩ resistor is connected between VOUT and GND. This is intended to discharge C_{OUT} when the LDO regulator is disabled. The internal 1.5kΩ has no adverse effect on device turn-on time.

Short-Circuit Protection

The AAT2786 contains an internal short-circuit protection circuit that will trigger when the output load current exceeds the internal threshold limit. Under short-circuit conditions, the output of the LDO regulator will be current limited until the short-circuit condition is removed from the output or LDO regulator package power dissipation exceeds the device thermal limit.

Thermal Protection

The AAT2786 has an internal thermal protection circuit which will turn on when the device die temperature exceeds 150°C. The internal thermal protection circuit will actively turn off the LDO regulator output pass device to prevent the possibility of over temperature damage. The LDO regulator output will remain in a shutdown state until the internal die temperature falls back below the 150°C trip point.

The combination and interaction between the short circuit and thermal protection systems allows the LDO regulator to withstand indefinite short-circuit conditions without sustaining permanent damage.

No-Load Stability

The AAT2786 is designed to maintain output voltage regulation and stability under operational no load conditions. This is an important characteristic for applications where the output current may drop to zero.

Reverse Output-to-Input Voltage Conditions and Protection

Under normal operating conditions, a parasitic diode exists between the output and input of the LDO regulator. The input voltage should always remain greater than the output load voltage, maintaining a reverse bias on the internal parasitic diode. Conditions where VOUT might exceed VIN should be avoided since this would forward bias the internal parasitic diode and allow excessive current flow into the VOUT pin, possibly damaging the LDO regulator.

In applications where there is a possibility of V_{OUT} exceeding V_{IN} for brief amounts of time during normal operation, the use of a larger value C_{IN} capacitor is highly recommended. A larger value of C_{IN} with respect to C_{OUT} will effect a slower C_{IN} decay rate during shutdown, thus preventing V_{OUT} from exceeding V_{IN}. In applications where there is a greater danger of V_{OUT} exceeding V_{IN} for extended periods of time, it is recommended to place a Schottky diode across V_{IN} to V_{OUT} (connecting the cathode to V_{IN} and anode to V_{OUT}). The Schottky diode forward voltage should be less than 0.45V.

This LDO regulator has complete short-circuit and thermal protection. The integral combination of these two internal protection circuits gives the AAT2786 LDO regulator a comprehensive safety system to guard against extreme adverse operating conditions. Device power dissipation is limited to the package type and thermal dissipation properties. Refer to the Thermal Considerations section of this datasheet for details on device operation at maximum output current loads.

Component Selection For Step-Down Converter

Inductor Selection

The step-down converter uses peak current mode control with slope compensation to maintain stability for duty cycles greater than 50%. The output inductor value must be selected so the inductor current down slope meets the internal slope compensation requirements. The internal slope compensation for the adjustable and low voltage fixed versions is 0.75A/µs. This equates to a slope compensation that is 75% of the inductor current down slope for a 1.8V output and 1.8µH inductor.

$$m = \frac{0.75 \cdot V_O}{L} = \frac{0.75 \cdot 1.8V}{1.8\mu H} = 0.75 \frac{A}{\mu s}$$

$$L = \frac{0.75 \cdot V_O}{m} = \frac{0.75 \cdot 3.3V}{0.75 \frac{A}{\mu s}} = 3.3\mu H$$

The inductor should be set equal to the output voltage numeric value in micro henries (µH). This guarantees that there is sufficient internal slope compensation. Manufacturer's specifications list both the inductor DC current rating, which is a thermal limitation, and the peak current rating, which is determined by the saturation characteristics. The inductor should not show any appreciable saturation under normal load conditions. Some inductors may meet the peak and average current ratings yet result in excessive losses due to a high DCR. Always consider the losses associated with the DCR and its effect on the total converter efficiency when selecting an inductor.

The 3.3µH CDRH4D28 series Sumida inductor has a 49.2mΩ worst case DCR and a 1.57A DC current rating. At full 1.5A load, the inductor DC loss is 97mW which gives less than 1.5% loss in efficiency for a 1.5A, 3.3V output.

Input Capacitor

Select a 10µF to 22µF X7R or X5R ceramic capacitor for the input. To estimate the required input capacitor size, determine the acceptable input ripple level (V_{PP}) and solve for C. The calculated value varies with input voltage and is a maximum when V_{IN} is double the output voltage.

$$C_{IN} = \frac{\frac{V_O}{V_{IN}} \cdot \left(1 - \frac{V_O}{V_{IN}}\right)}{\left(\frac{V_{PP}}{I_O} - ESR\right) \cdot F_S}$$

$$\frac{V_O}{V_{IN}} \cdot \left(1 - \frac{V_O}{V_{IN}}\right) = \frac{1}{4} \text{ for } V_{IN} = 2 \cdot V_O$$

$$C_{IN(MIN)} = \frac{1}{\left(\frac{V_{PP}}{I_O} - ESR\right) \cdot 4 \cdot F_S}$$

Always examine the ceramic capacitor DC voltage coefficient characteristics when selecting the proper value. For example, the capacitance of a 10µF, 6.3V, X5R ceramic capacitor with 5.0V DC applied is actually about 6µF.

The maximum input capacitor RMS current is:

$$I_{RMS} = I_O \cdot \sqrt{\frac{V_O}{V_{IN}} \cdot \left(1 - \frac{V_O}{V_{IN}}\right)}$$

The input capacitor RMS ripple current varies with the input and output voltage and will always be less than or equal to half of the total DC load current.

$$\sqrt{\frac{V_O}{V_{IN}} \cdot \left(1 - \frac{V_O}{V_{IN}}\right)} = \sqrt{D \cdot (1 - D)} = \sqrt{0.5^2} = \frac{1}{2}$$

For $V_{IN} = 2 \cdot V_O$

$$I_{RMS(MAX)} = \frac{I_O}{2}$$

The term $\frac{V_O}{V_{IN}} \cdot \left(1 - \frac{V_O}{V_{IN}}\right)$ appears in both the input voltage ripple and input capacitor RMS current equations and is a maximum when V_O is twice V_{IN}. This is why the input voltage ripple and the input capacitor RMS current ripple are a maximum at 50% duty cycle.

The input capacitor provides a low impedance loop for the edges of pulsed current drawn by the AAT2786. Low ESR/ESL X7R and X5R ceramic capacitors are ideal for this function. To minimize stray inductance, the capacitor should be placed as closely as possible to the IC. This keeps the high frequency content of the input current localized, minimizing EMI and input voltage ripple. The proper placement of the input capacitor (C1) can be seen in the evaluation board layout in the Layout section of this datasheet (see Figure 2).

A laboratory test set-up typically consists of two long wires running from the bench power supply to the evaluation board input voltage pins. The inductance of these wires, along with the low-ESR ceramic input capacitor, can create a high Q network that may affect converter performance. This problem often becomes apparent in the form of excessive ringing in the output voltage during load transients. Errors in the loop phase and gain measurements can also result. Since the inductance of a short PCB trace feeding the input voltage is significantly lower than the power leads from the bench power supply, most applications do not exhibit this problem.

In applications where the input power source lead inductance cannot be reduced to a level that does not affect the converter performance, a high ESR tantalum or aluminum electrolytic should be placed in parallel with the low ESR/ESL bypass ceramic capacitor. This dampens the high Q network and stabilizes the system.

Output Capacitor

The output capacitor limits the output ripple and provides holdup during large load transitions. A 10µF to 22µF X5R or X7R ceramic capacitor typically provides sufficient bulk capacitance to stabilize the output during large load transitions and has the ESR and ESL characteristics necessary for low output ripple.

The output voltage droop due to a load transient is dominated by the capacitance of the ceramic output capacitor. During a step increase in load current, the ceramic output capacitor alone supplies the load current until the loop responds. Within two or three switching cycles, the loop responds and the inductor current increases to match the load current demand. The relationship of the output voltage droop during the three switching cycles to the output capacitance can be estimated by:

$$C_{OUT} = \frac{3 \cdot \Delta I_{LOAD}}{V_{DROOP} \cdot F_S}$$

Once the average inductor current increases to the DC load level, the output voltage recovers. The above equation establishes a limit on the minimum value for the output capacitor with respect to load transients.

The internal voltage loop compensation also limits the minimum output capacitor value to 10µF. This is due to its effect on the loop crossover frequency (bandwidth), phase margin, and gain margin. Increased output capacitance will reduce the crossover frequency with greater phase margin.

Adjustable Output Resistor Selection

The output voltage on the AAT2786 is programmed with external resistors R1 and R2. To limit the bias current required for the external feedback resistor string while maintaining good noise immunity, the minimum suggested value for R2 is 59kΩ. Although a larger value will further reduce quiescent current, it will also increase the impedance of the feedback node, making it more sensitive to external noise and interference. Table 1 summarizes the resistor values for various output voltages with R2 set to either 59kΩ for good noise immunity or 221kΩ for reduced no load input current.

V_{OUT}(V)	R_2 = 59kΩ R_1(kΩ)	R_2 = 221kΩ R_1(kΩ)
0.8	19.6	75
0.9	29.4	113
1.0	39.2	150
1.1	49.9	187
1.2	59.0	221
1.3	68.1	261
1.4	78.7	301
1.5	88.7	332
1.8	118	442
1.85	124	464
2.0	137	523
2.5	187	715
3.0	237	887
3.3	267	1000

Table 1: AAT2786 Resistor Values for Various Output Voltages.

Component Selection For LDO

Input Capacitor

Typically, a 1µF or larger capacitor is recommended for CIN in most applications. A C_{IN} capacitor is not required for basic LDO regulator operation. However, if the AAT2786 is physically located more than three centimeters from an input power source, a C_{IN} capacitor will be needed for stable operation. C_{IN} should be located as close to the device V_{IN} pin as practically possible. C_{IN} values greater than 1µF will offer superior input line transient response and will assist in maximizing the highest possible power supply ripple rejection.

Ceramic, tantalum, or aluminum electrolytic capacitors may be selected for C_{IN}. There is no specific capacitor ESR requirement for C_{IN}. However, for 150mA LDO regulator output operation, ceramic capacitors are recommended for C_{IN} due to their inherent capability over tantalum capacitors to withstand input current surges from low impedance sources, such as batteries in portable devices.

Output Capacitor

For proper load voltage regulation and operational stability, a capacitor is required between pins V_{OUT} and GND. The C_{OUT} capacitor connection to the LDO regulator ground pin should be made as direct as practically possible for maximum device performance.

The AAT2786 has been specifically designed to function with very low ESR ceramic capacitors. For best performance, ceramic capacitors are recommended.

Typical output capacitor values for maximum output current conditions range from 1µF to 10µF. Applications utilizing the exceptionally low output noise and optimum power supply ripple rejection characteristics of the AAT2786 should use 2.2µF or greater for C_{OUT}. If desired, C_{OUT} may be increased without limit.

In low output current applications where output load is less than 10mA, the minimum value for C_{OUT} can be as low as 0.47µF.

Bypass Capacitor and Low Noise Applications

A bypass capacitor pin is provided to enhance the low noise characteristics of the AAT2786 LDO regulator. The bypass capacitor is not necessary for operation of the AAT2786. However, for best device performance, a small ceramic capacitor should be placed between the bypass pin (BYP) and the device ground pin (GND). The value of C_{BYP} may range from 470pF to 10nF. For lowest noise and best possible power supply ripple rejection performance, a 10nF capacitor should be used. To practically realize the highest power supply ripple rejection and lowest output noise performance, it is critical that the capacitor connection between the BYP pin and GND pin be direct and PCB traces should be as short as possible. Refer to the PCB Layout Recommendations section of this datasheet for examples.

There is a relationship between the bypass capacitor value and the LDO regulator turn-on time and turn-off time. In applications where fast device turn-on and turn-off time are desired, the value of C_{BYP} should be reduced.

In applications where low noise performance and/ or ripple rejection are less of a concern, the bypass capacitor may be omitted. The fastest device turn on time will be realized when no bypass capacitor is used.

DC leakage on this pin can affect the LDO regulator output noise and voltage regulation performance. For this reason, the use of a low leakage, high quality ceramic (NPO or C0G type) or film capacitor is highly recommended.

Capacitor Characteristics

Ceramic composition capacitors are highly recommended over all other types of capacitors for use with the AAT2786. Ceramic capacitors offer many advantages over their tantalum and aluminum electrolytic counterparts. A ceramic capacitor typically has very low ESR, is lower cost, has a smaller PCB footprint, and is non-polarized. Line and load transient response of the LDO regulator is improved by using low-ESR ceramic capacitors. Since ceramic capacitors are non-polarized, they are not prone to incorrect connection damage.

Equivalent Series Resistance

ESR is a very important characteristic to consider when selecting a capacitor. ESR is the internal series resistance associated with a capacitor that includes lead resistance, internal connections, size and area, material composition, and ambient temperature. Typically, capacitor ESR is measured in milliohms for ceramic capacitors and can range to more than several ohms for tantalum or aluminum electrolytic capacitors.

Ceramic Capacitor Materials

Ceramic capacitors less than 0.1µF are typically made from NPO or C0G materials. NPO and C0G materials generally have tight tolerance and are very stable over temperature. Larger capacitor values are usually composed of X7R, X5R, Z5U, or Y5V dielectric materials. Large ceramic capacitors (i.e., greater than 2.2µF) are often available in low-cost Y5V and Z5U dielectrics. These two material types are not recommended for use with LDO regulators since the capacitor tolerance can vary more than ±50% over the operating temperature range of the device. A 2.2µF Y5V capacitor could be reduced to 1µF over temperature; this could cause problems for circuit operation. X7R and X5R dielectrics are much more desirable. The temperature tolerance of X7R dielectric is better than ±15%.

Capacitor area is another contributor to ESR. Capacitors that are physically large in size will have a lower ESR when compared to a smaller sized capacitor of an equivalent material and capacitance value. These larger devices can improve circuit transient response when compared to an equal value capacitor in a smaller package size.

Consult capacitor vendor datasheets carefully when selecting capacitors for LDO regulators.

Thermal Calculations

There are three types of losses associated with the AAT2786 step-down converter: switching losses, conduction losses, and quiescent current losses. Conduction losses are associated with the $R_{DS(ON)}$ characteristics of the power output switching devices. Switching losses are dominated by the gate charge of the power output switching devices. At full load, assuming continuous conduction mode (CCM), a simplified form of the step-down converter and LDO losses is given by:

$$P_{TOTAL} = \frac{I_O^2 \cdot (R_{DS(ON)H} \cdot V_{OBUCK} + R_{DS(ON)L} \cdot [V_{INBUCK} - V_{OUTBUCK}])}{V_{IN(BUCK)}}$$

$$+ (t_{sw} \cdot F_S \cdot I_{OBUCK} + I_{QBUCK}) \cdot V_{INBUCK} + (V_{INLDO} - V_{OUTLDO}) \cdot I_{OLDO}$$

I_{QBUCK} and I_{QLDO} are the step-down converter and LDO quiescent currents respectively. The term t_{SW} is used to estimate the full load step-down converter switching losses.

For the condition where the step-down converter is in dropout at 100% duty cycle, the total device dissipation reduces to:

$$P_{TOTAL} = I_{OBUCK}^2 \cdot R_{DS(ON)H} + (t_{SW} \cdot F_S \cdot I_{BUCK} + I_{QBUCK}) \cdot V_{INBUCK} + (V_{INLDO} - V_{OUTLDO}) \cdot I_{OLDO}$$

Since $R_{DS(ON)}$, quiescent current, and switching losses all vary with input voltage, the total losses should be investigated over the complete input voltage range.

Given the total losses, the maximum junction temperature can be derived from the θ_{JA} for the TDFN34-16 package, which is 50°C/W.

$$T_{J(MAX)} = P_{TOTAL} \cdot \Theta_{JA} + T_{AMB}$$

PCB Layout

The suggested PCB layout for the AAT2786 is shown in Figures 1 and 2. The following guidelines should be used to help ensure a proper layout.

1. The input and output capacitors (C2, C6, and C7) should connect as closely as possible to the input and output pins.
2. R1 and C3 are optional low pass filter components for the IN supply pin for the BUCK if additional noise decupling is required in a noisy system.
3. The connection of L1 to the LX pin should be as short as possible.
4. The feedback trace or FB pin should be separated from any power trace and connect as closely as possible to the load point. Sensing along a high-current load trace will degrade DC load regulation.
5. The resistance of the trace from the load return to PGND should be kept to a minimum. This will help to minimize any error in DC regulation due to differences in the potential of the internal signal ground and the power ground.
6. Connect unused signal pins to ground to avoid unwanted noise coupling.
7. For low output noise and highest possible power supply ripple rejection performance, it is critical to connect the bypass capacitor (C8) and output capacitor (C7) directly to the LDO regulator ground pin. This method will eliminate any load noise or ripple current feedback through the LDO regulator.
8. For good thermal coupling, PCB vias are required from the pad for the TDFN paddle to the bottom ground plane.

Printed Circuit Board Layout Recommendations

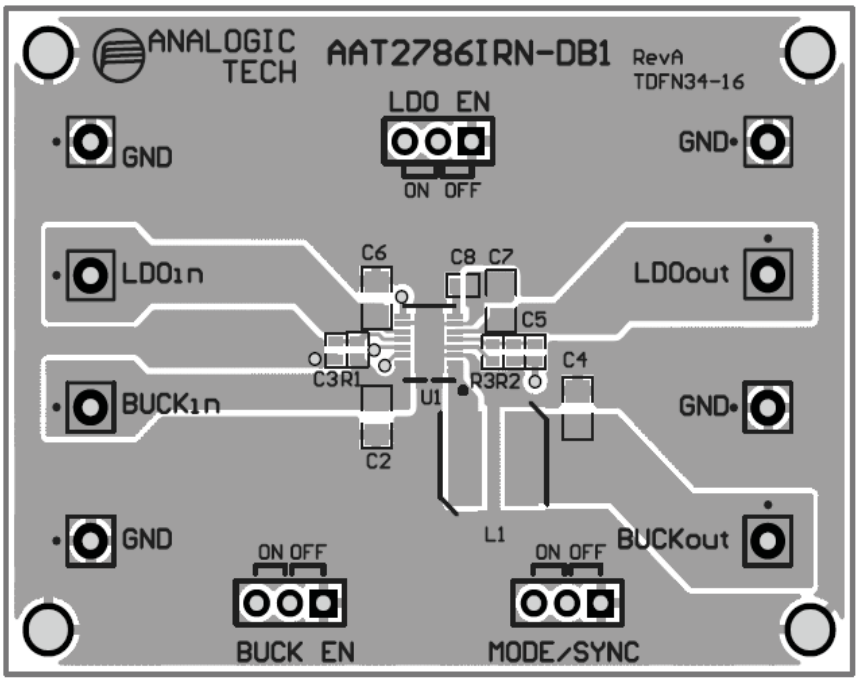


Figure 1: AAT2786 Evaluation Board Component Side Layout.

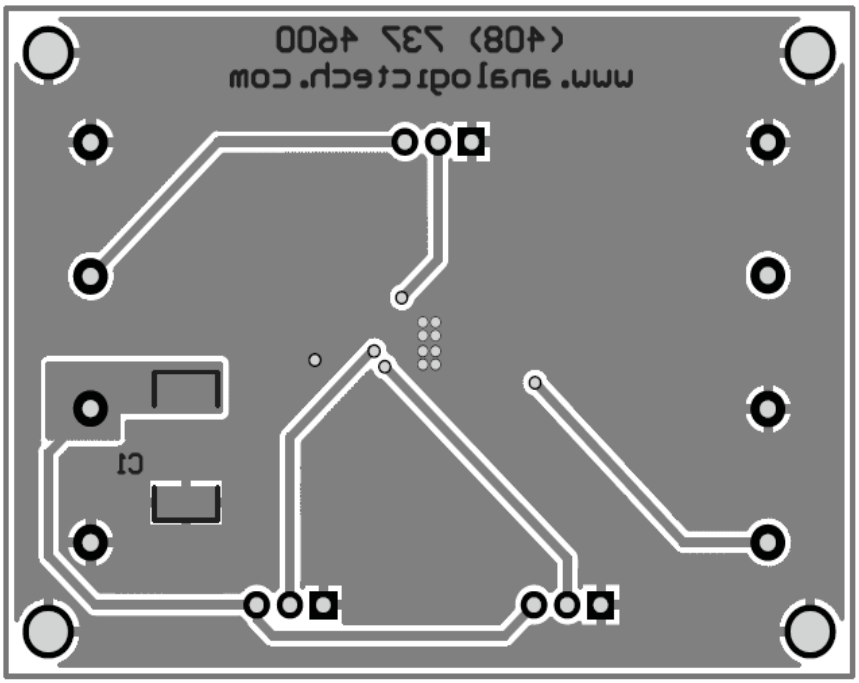


Figure 2: AAT2786 Evaluation Board Solder Side Layout.

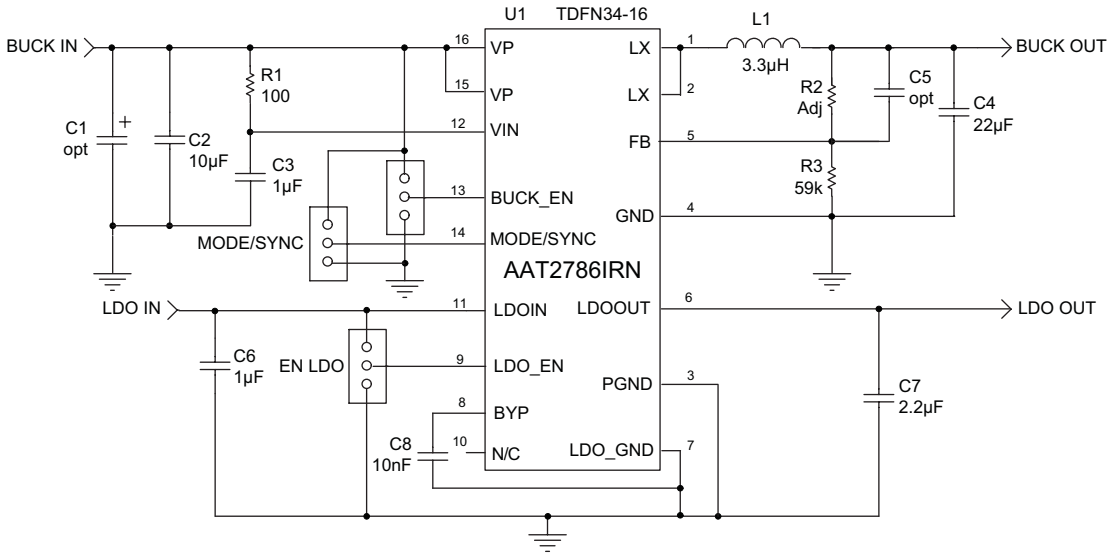


Figure 3: AAT2786 Evaluation Board Schematic.

Step-Down Converter Design Example

Specifications

V_{OBUCK} = 3.3V @ 1.5A, Pulsed Load ΔI_{LOAD} = 1.5A
V_{OLDO} = 2.5V @ 150mA
V_{IN} = 2.7V to 4.2V (3.6V nominal)
F_S = 1.2MHz
m = 0.75A/µs
T_{AMB} = 85°C in TDFN34-16 Package

3.3V Buck Output Inductor

$$L = \frac{0.75 \cdot V_O}{m} = \frac{0.75 \cdot 3.3V}{0.75\,\frac{A}{\mu s}} = 3.3\mu H \text{ (see Table 2)}$$

For Sumida inductor CDRH4D28, 3.3µH, DCR = 49.2mΩ max.

$$\Delta I = \frac{V_{OBUCK}}{L1 \cdot F_S} \cdot 1 - \left(\frac{V_{OBUCK}}{V_{INBUCK}}\right) = \frac{3.3V}{3.3\mu H \cdot 1.2MHz} \cdot \left(1 - \frac{3.3V}{4.2V}\right) = 179mA$$

$$I_{PK} = I_{OBUCK} + \frac{\Delta I_1}{2} = 1.5A + 0.089A = 1.59A$$

$$P_{L1} = I_{OUTBUCK}^2 \cdot DCR = 1.5A^2 \cdot 49.2m\Omega = 110mW$$

3.3V Buck Output Capacitor

V_{DROOP} = 0.2V

$$C_{OUT} = \frac{3 \cdot \Delta I_{LOAD}}{V_{DROOP} \cdot F_S} = \frac{3 \cdot 1.5A}{0.2V \cdot 1.2MHz} = 18.8\mu F; \text{ use } 22\mu F$$

$$I_{RMS(MAX)} = \frac{1}{2 \cdot \sqrt{3}} \cdot \frac{(V_{OUT}) \cdot (V_{IN(MAX)} - V_{OUT})}{L \cdot F_S \cdot V_{IN(MAX)}} = \frac{1}{2 \cdot \sqrt{3}} \cdot \frac{3.3V \cdot (4.2V - 3.3V)}{3.3\mu H \cdot 1.2MHz \cdot 4.2V} = 52mArms$$

$$P_{RMS} = ESR \cdot I_{RMS}^2 = 5m\Omega \cdot (52mA)^2 = 13.3\mu W$$

3.3V Buck Input Capacitor

Input Ripple V_{PP} = 50mV

$$C_{IN} = \frac{1}{\left(\frac{V_{PP}}{I_{OBUCK}} - ESR\right) \cdot 4 \cdot F_S} = \frac{1}{\left(\frac{50mV}{1.5A} - 5m\Omega\right) \cdot 4 \cdot 1.2MHz} = 7.3\mu F; \text{ use } 10\mu F$$

$$I_{RMS(MAX)} = \frac{I_{OBUCK}}{2} = 0.75Arms$$

$$P = ESR \cdot (I_{RMS}^2) = 5m\Omega \cdot (0.75A)^2 = 3mW$$

AAT2786 Losses

Total losses can be estimated by calculating the dropout (V_{IN} = V_{OBUCK}) losses where the power MOSFET $R_{DS(ON)}$ will be at the maximum value. All values assume an 85°C ambient temperature and a 120°C junction temperature with the TDFN 50°C/W package.

$$P_{TOTAL} = I_{OBUCK}^2 \cdot R_{DS(ON)H} + (V_{INLDO} - V_{OUTLDO}) \cdot I_{OLDO}$$

$$= 1.5A^2 \cdot 0.16\Omega + (4.2 - 2.5) \cdot 150mA$$

$$= 615mW$$

$$T_{J(MAX)} = T_{AMB} + \Theta_{JA} \cdot P_{LOSS} = 85°C + (50°C/W) \cdot 615mW = 116°C$$

The total losses are also investigated at the nominal lithium-ion battery voltage (3.6V). The simplified version of the $R_{DS(ON)}$ losses assumes that the N-channel and P-channel $R_{DS(ON)}$ are equal.

$$P_{TOTAL} = I_{OBUCK}^2 \cdot R_{DS(ON)H} + (t_{sw} \cdot F_S \cdot I_{BUCK} + I_{QBUCK}) \cdot V_{INBUCK} + (V_{INLDO} - V_{OUTLDO}) - I_{OLDO}$$

$$= 1.5A^2 \cdot 152m\Omega + (5ns \cdot 1.2MHz \cdot 1.5A + 50\mu A) \cdot 3.6V + (4.2V - 2.5V) \cdot 150mA$$

$$= 630mW$$

$$T_{J(MAX)} = T_{AMB} + \Theta_{JA} \cdot P_{LOSS} = 85°C + (50°C/W) \cdot 6300mW = 117°C$$

V_{OUT} (V)	Inductance (µH)	Part Number	Manufacturer	Size (mm)	Rated Current (A)	I_{RMS} (A)	I_{SAT} (A)	DCR (Ω)
3.3	3.3	CDRH4D28	Sumida	5x5x3	1.57			36.4
2.5	2.2	CDRH4D28	Sumida	5x5x3	2.04			23.2
1.8	1.8	CDRH4D28	Sumida	5x5x3	2.2			20.4
1.5	1.8	CDRH4D28	Sumida	5x5x3	2.2			20.4
1.2	1.2	CDRH4D28	Sumida	5x5x3	2.56			17.5
1.0	1.0	SD3114-1.0	Cooper	3.1x3.1x1.45		1.67	2.07	0.042
0.8	1.0	SD3114-1.0	Cooper	3.1x3.1x1.45		1.67	2.07	0.042
0.6	1.0	SD3114-1.0	Cooper	3.1x3.1x1.45		1.67	2.07	0.042

Table 2: Surface Mount Inductors.

Manufacturer	Part Number	Value	Voltage	Temp. Co.	Case
Murata	GRM21BR60J106KE19	10µF	6.3V	X5R	0805
Murata	GRM21BR60J226ME39	22µF	6.3V	X5R	0805

Table 3: Surface Mount Capacitors.

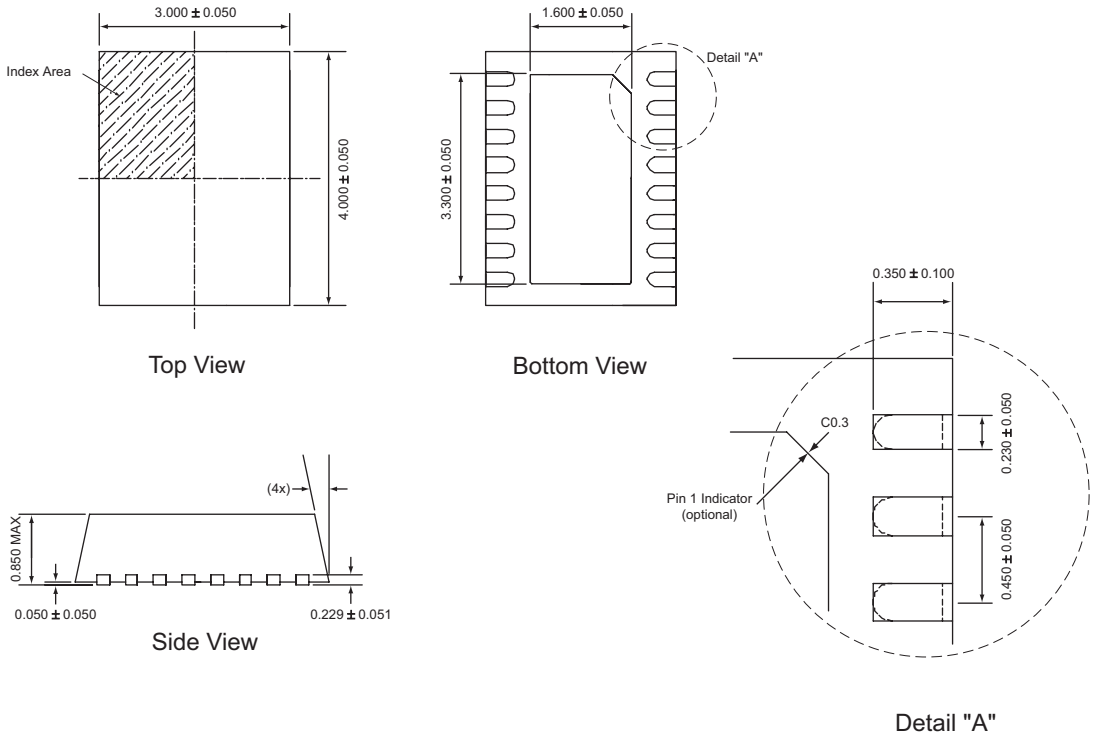
Ordering Information

Package	Part Marking[1]	LDO Output Voltage	Part Number (Tape and Reel)[2]
TDFN34-16	3KXYY	E = 1.2V	**AAT2786IRN-AE-T1**

All AnalogicTech products are offered in Pb-free packaging. The term "Pb-free" means semiconductor products that are in compliance with current RoHS standards, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. For more information, please visit our website at http://www.analogictech.com/about/quality.aspx.

Package Information[3]

TDFN34-16



All dimensions in millimeters.

1. XYY = assembly and date code.
2. Sample stock is generally held on part numbers listed in **BOLD**.
3. The leadless package family, which includes QFN, TQFN, DFN, TDFN and STDFN, has exposed copper (unplated) at the end of the lead terminals due to the manufacturing process. A solder fillet at the exposed copper edge cannot be guaranteed and is not required to ensure a proper bottom solder connection.

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