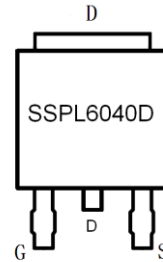
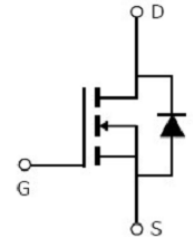


Main Product Characteristics:

V_{DS}	60V
$R_{DS(on)}$	34m Ω (typ.)
I_D	33A


TO-252 (D-PAK)

Marking and pin Assignment

Schematic diagram
Features and Benefits:

- Advanced Process Technology
- Special designed for PWM, load switching and general purpose applications
- Ultra low on-resistance with low gate charge
- Fast switching and reverse body recovery
- 175°C operating temperature


Description:

These N-Channel enhancement mode power field effect transistors are produced using silikron proprietary MOSFET technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switch mode power supplies.

Absolute max Rating:

Symbol	Parameter	Max.	Units
I_D @ TC = 25°C	Continuous Drain Current, V_{GS} @ 10V ^①	33	A
I_D @ TC = 100°C	Continuous Drain Current, V_{GS} @ 10V ^①	23	
I_{DM}	Pulsed Drain Current ^②	132	
P_D @ TC = 25°C	Power Dissipation ^③	45	W
	Linear Derating Factor	0.3	W/°C
V_{DS}	Drain-Source Voltage	60	V
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy @ L=1.0mH	112	mJ
I_{AS}	Avalanche Current @ L=1.0mH	15	A
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C

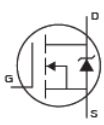
Thermal Resistance

Symbol	Characterizes	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-case ^③	—	3.3	°C/W
$R_{\theta JA}$	Junction-to-ambient ($t \leq 10s$) ^④	—	80	°C/W

Electrical Characterizes @ $T_A=25^\circ\text{C}$ unless otherwise specified

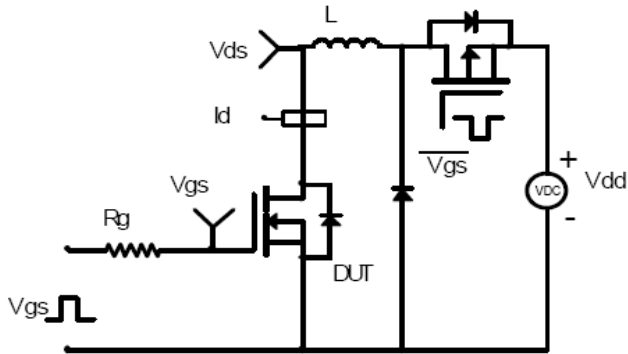
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source breakdown voltage	60	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$R_{DS(on)}$	Static Drain-to-Source on-resistance	—	34	40	mΩ	$V_{GS}=10V, I_D = 10A$
		—	60	—		$T_J = 125^\circ\text{C}$
$V_{GS(th)}$	Gate threshold voltage	2	—	4	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
		—	2.5	—		$T_J = 125^\circ\text{C}$
I_{DSS}	Drain-to-Source leakage current	—	—	1	μA	$V_{DS} = 60V, V_{GS} = 0V$
		—	—	50		$T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source forward leakage	—	—	100	nA	$V_{GS} = 20V$
		—	—	-100		$V_{GS} = -20V$
Q_g	Total gate charge	—	14	—	nC	$I_D = 10A,$ $V_{DS}=44V,$ $V_{GS} = 10V$
Q_{gs}	Gate-to-Source charge	—	4.2	—		
Q_{gd}	Gate-to-Drain("Miller") charge	—	5.3	—		
$t_{d(on)}$	Turn-on delay time	—	10	—	ns	$V_{GS}=10V, V_{DD}=28V,$ $R_L=2.6\Omega,$ $R_{GEN}=24\Omega$ $I_D=10A$
t_r	Rise time	—	36	—		
$t_{d(off)}$	Turn-Off delay time	—	26	—		
t_f	Fall time	—	25	—		
C_{iss}	Input capacitance	—	597	—	pF	$V_{GS} = 0V$
C_{oss}	Output capacitance	—	155	—		$V_{DS} = 25V$
C_{rss}	Reverse transfer capacitance	—	33	—		$f = 1MHz$

Source-Drain Ratings and Characteristics

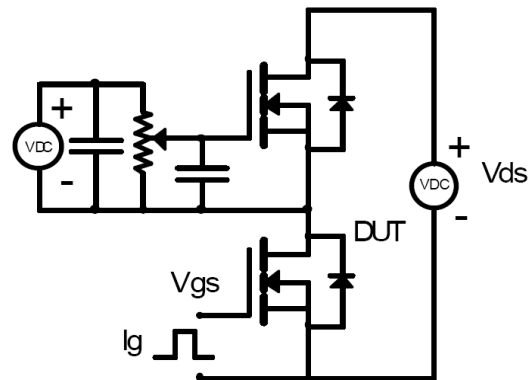
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	33	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode)	—	—	132	A	
V_{SD}	Diode Forward Voltage	—	0.76	1.3	V	$I_S=10A, V_{GS}=0V, T_J = 25^\circ\text{C}$
t_{rr}	Reverse Recovery Time	—	28	—	ns	$T_J = 25^\circ\text{C}, I_F = 10A,$ $di/dt = 100A/\mu s$
Q_{rr}	Reverse Recovery Charge	—	38	—	nC	

Test circuits and Waveforms

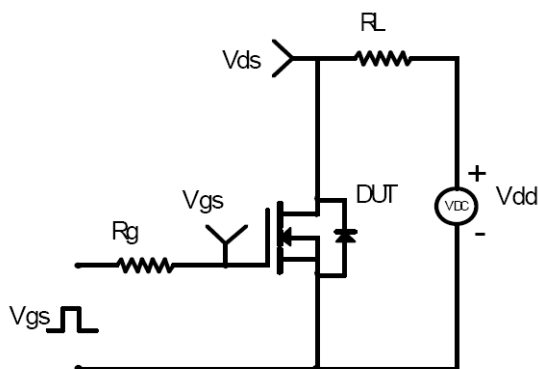
EAS Test Circuit:



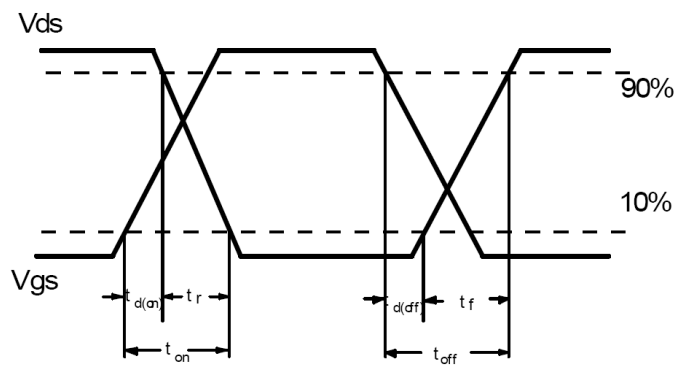
Gate charge test circuit:



Switching Time Test Circuit:



Switching Waveforms:



Notes:

- ① Calculated continuous current based on maximum allowable junction temperature.
- ② Repetitive rating; pulse width limited by max. junction temperature.
- ③ The power dissipation PD is based on max. junction temperature, using junction-to-case thermal resistance.
- ④ The value of $R_{\theta JA}$ is measured with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with $T_A = 25^\circ\text{C}$

Typical electrical and thermal characteristics

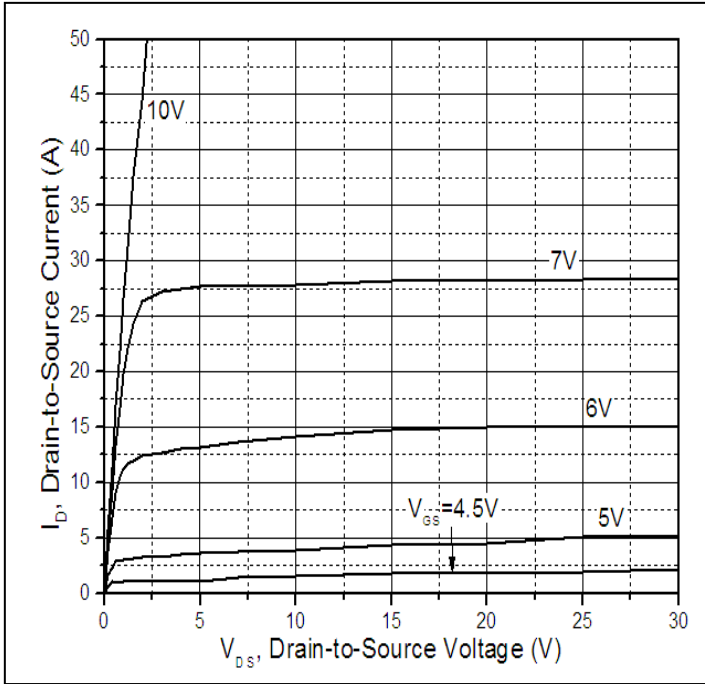


Figure 1: Typical Output Characteristics

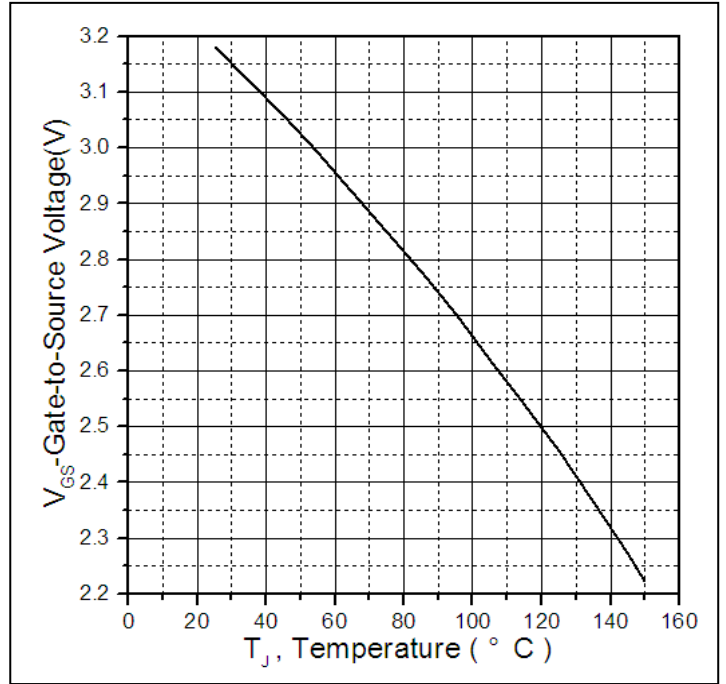


Figure 2: Gate to source cut-off voltage

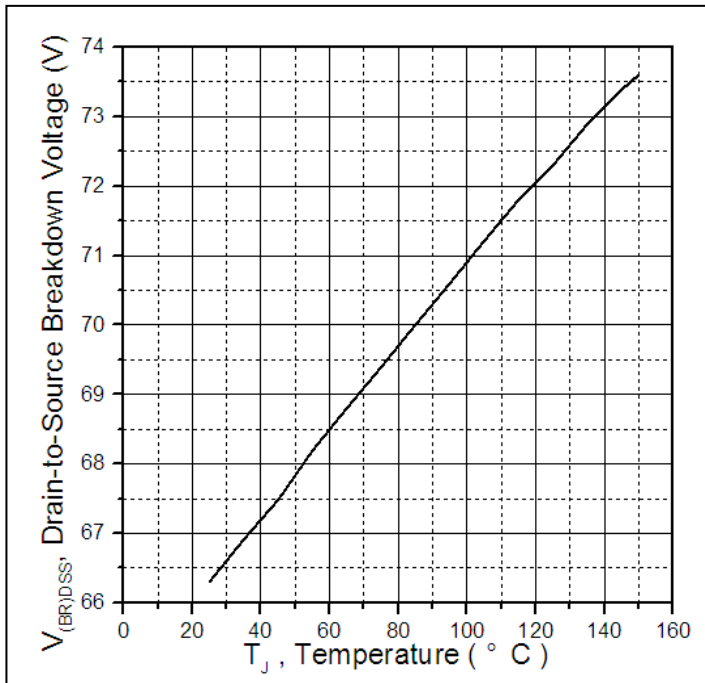


Figure 3: Drain-to-Source Breakdown Voltage Vs. Case Temperature

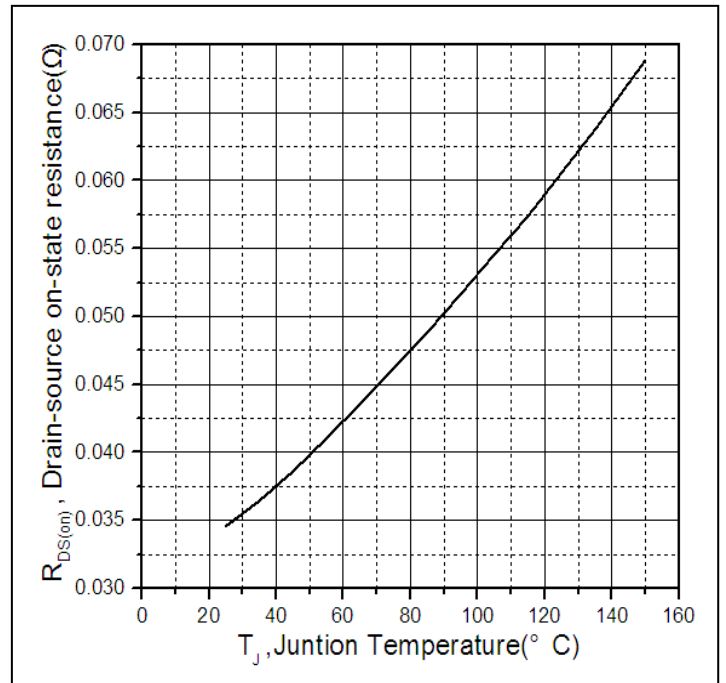


Figure 4: Normalized On-Resistance Vs. Case Temperature

Typical electrical and thermal characteristics

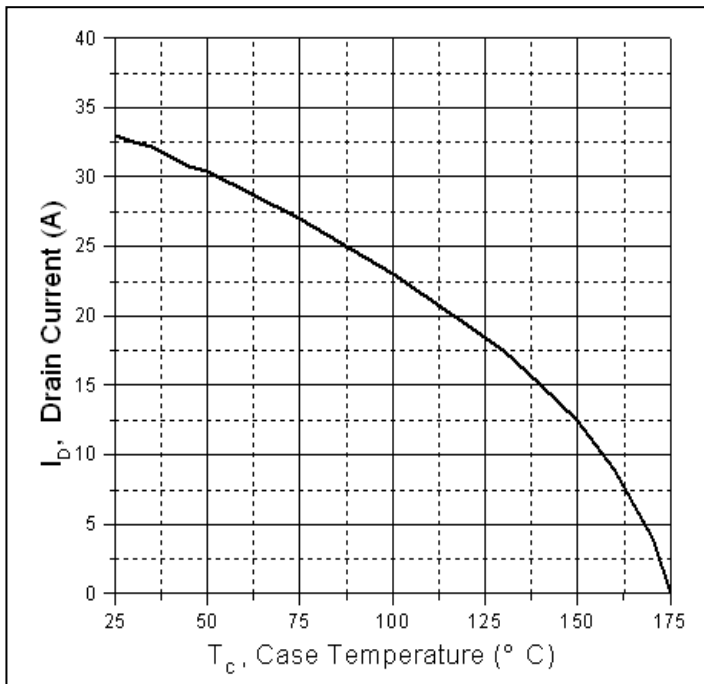


Figure 5. Maximum Drain Current Vs. Case Temperature

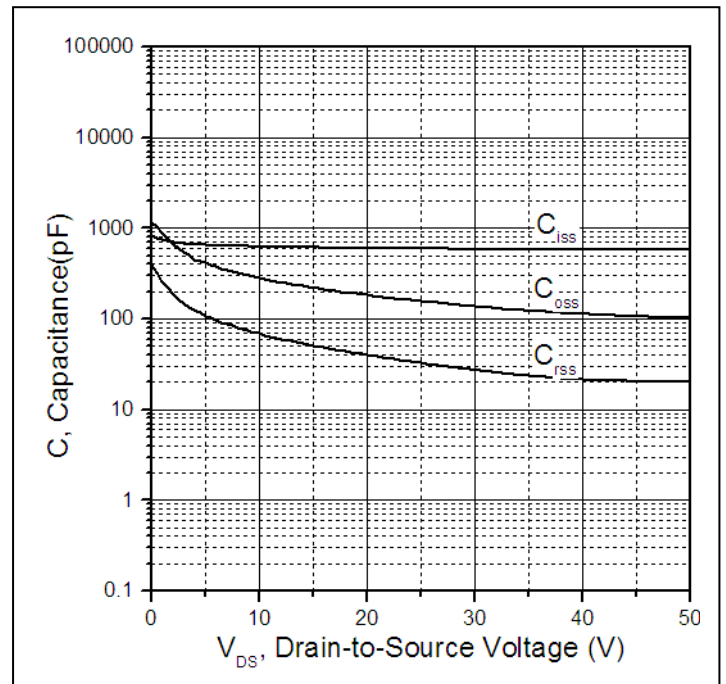


Figure 6. Typical Capacitance Vs. Drain-to-Source Voltage

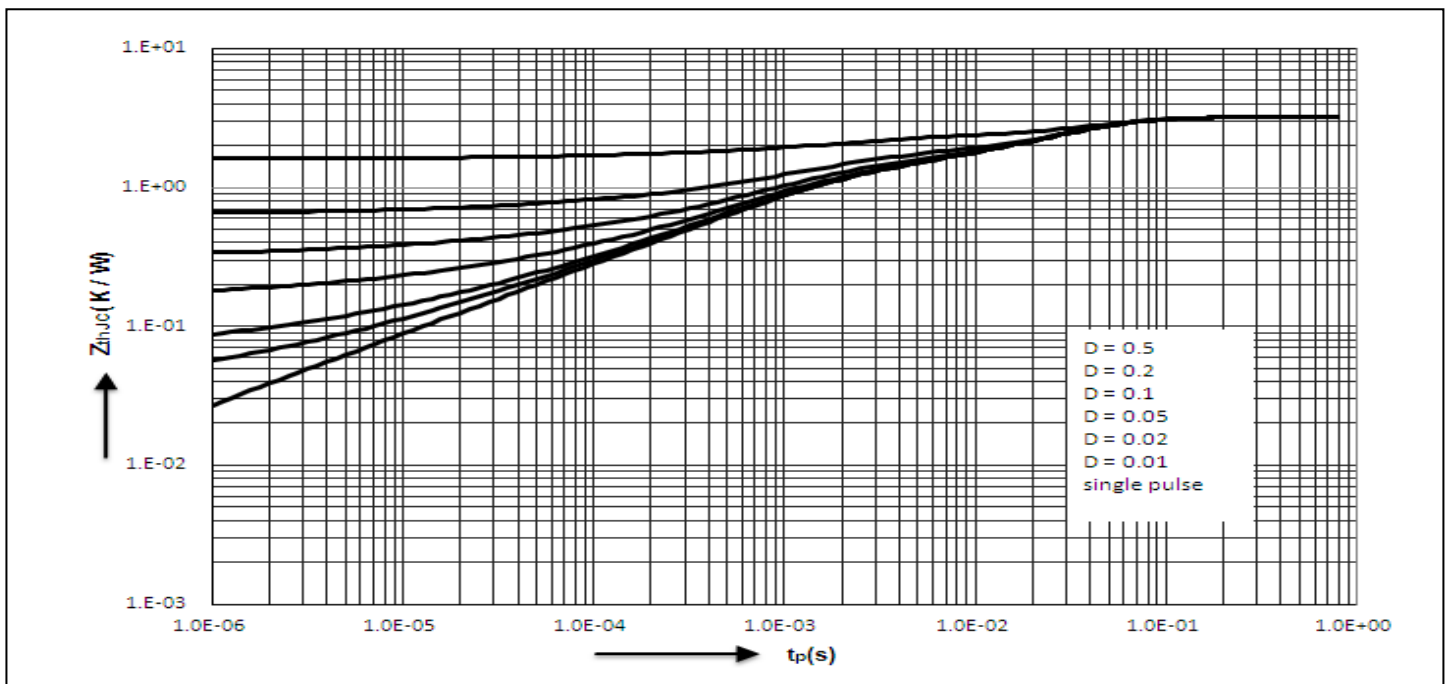
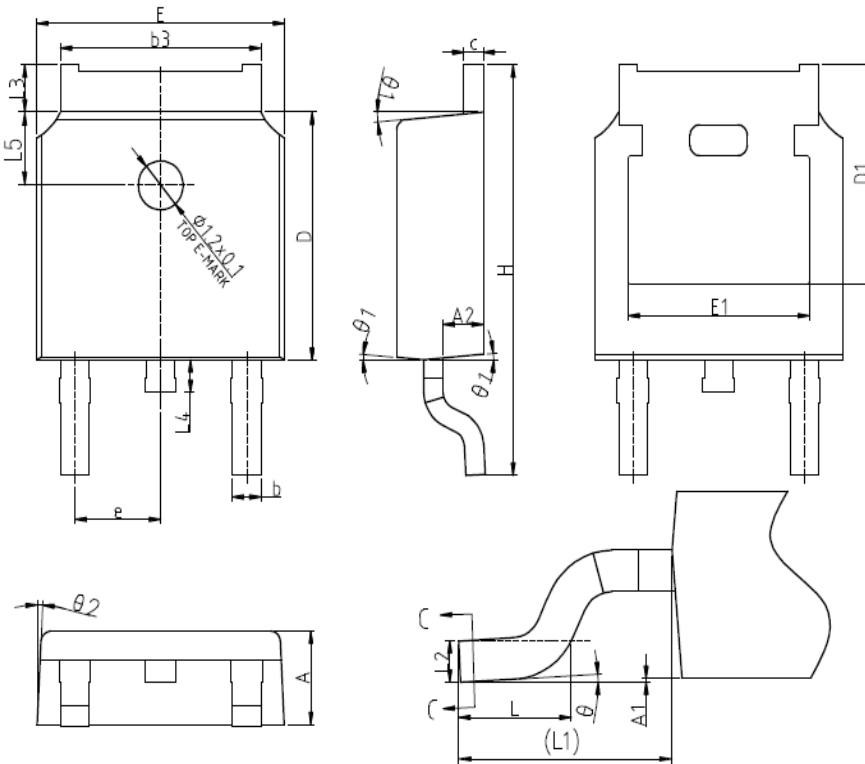


Figure7. Maximum Effective Transient Thermal Impedance, Junction-to-Case

Mechanical Data:
TO-252 PACKAGE OUTLINE DIMENSION


Symbol	Dimension In Millimeters			Dimension In Inches		
	Min	Nom	Max	Min	Nom	Max
A	2.200	2.300	2.380	0.087	0.091	0.094
A1	0.000	-	0.100	0.000	-	0.004
A2	0.970	1.070	1.170	0.038	0.042	0.046
b	0.720	0.780	0.850	0.028	0.031	0.033
b1	0.710	0.760	0.810	0.028	0.030	0.032
b3	5.230	5.330	5.460	0.206	0.210	0.215
c	0.470	0.530	0.580	0.019	0.021	0.023
c1	0.460	0.510	0.560	0.018	0.020	0.022
D	6.000	6.100	6.200	0.236	0.240	0.244
D1	5.350 (REF)			0.211 (REF)		
E	6.500	6.600	6.700	0.256	0.260	0.264
E1	4.700	4.830	4.920	0.185	0.190	0.194
e	2.286 (REF)			0.090 (REF)		
H	9.900	10.100	10.300	0.390	0.398	0.406
L	1.400	1.500	1.700	0.055	0.059	0.067
L1	2.90 (REF)			0.114 (REF)		
L2	0.51 (BSC)			0.020 (BSC)		
L3	0.900	-	1.250	0.035	-	0.049
L4	0.600	0.800	1.000	0.024	0.031	0.039
L5	1.700	1.800	1.900	0.067	0.071	0.075
θ	0°	-	8°	0°	-	8°
θ1	5°	7°	9°	5°	7°	9°
θ2	5°	7°	9°	5°	7°	9°

Ordering and Marking Information**Device Marking: SSPL6040D**

Package (Available)
TO-252(D-PAK)
Operating Temperature Range
C : -55 to175 °C

Devices per Unit

Package Type	Units/Tape	Tapes/Inner Box	Units/Inner Box	Inner Boxes/Carton Box	Units/Carton Box
TO-252	3000	2	6000	5	30000

Reliability Test Program

Test Item	Conditions	Duration	Sample Size
High Temperature Reverse Bias(HTRB)	$T_j=125^{\circ}\text{C}$ to 175°C @ 80% of Max $V_{DSS}/V_{CES}/V_R$	168 hours 500 hours 1000 hours	3 lots x 77 devices
High Temperature Gate Bias(HTGB)	$T_j=125^{\circ}\text{C}$ or 175°C @ 100% of Max V_{GSS}	168 hours 500 hours 1000 hours	3 lots x 77 devices

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