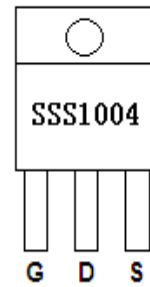


Main Product Characteristics

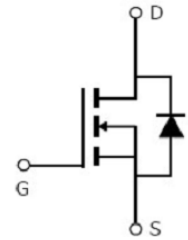
V_{DS}	100V
$R_{DS(on)}$	3.7m Ω (typ.)
I_D	180A ①



TO-220



Marking and pin
Assignment



Schematic diagram

Features and Benefits

- Advanced Process Technology
- Special designed for PWM, load switching and general purpose applications
- Ultra low on-resistance with low gate charge
- Fast switching and reverse body recovery
- 175°C operating temperature



Description

It utilizes the latest processing techniques to achieve the high cell density and reduces the on-resistance with high repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in power switching application and a wide variety of other applications.

Absolute max Rating

Symbol	Parameter	Max.	Units
I_D @ TC = 25°C	Continuous Drain Current, V_{GS} @ 10V	180 ①	A
I_D @ TC = 100°C	Continuous Drain Current, V_{GS} @ 10V	130 ①	
I_{DM}	Pulsed Drain Current ②	670	
P_D @TC = 25°C	Power Dissipation ③	375	W
	Linear Derating Factor	2.5	W/°C
V_{DS}	Drain-Source Voltage	100	V
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy @ L=0.3mH	1045	mJ
I_{AS}	Avalanche Current @ L=0.3mH	83.5	A
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +175	°C

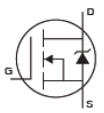
Thermal Resistance

Symbol	Characterizes	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-case ③	—	0.4	°C/W
$R_{\theta JA}$	Junction-to-ambient ($t \leq 10s$) ④	—	62	°C/W
	Junction-to-Ambient (PCB mounted, steady-state) ④	—	40	°C/W

Electrical Characterizes @ $T_A = 25^\circ\text{C}$ unless otherwise specified

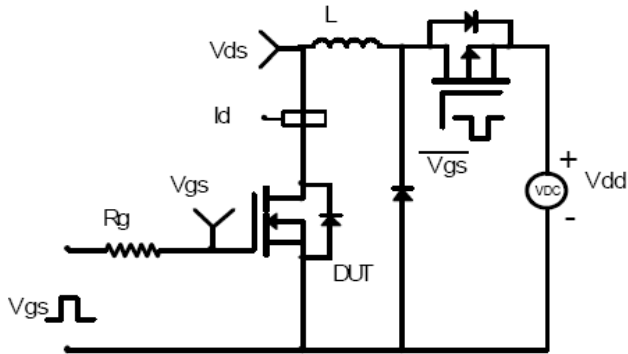
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source breakdown voltage	100	—	—	V	$V_{GS} = 0V, I_D = 1mA$
$R_{DS(on)}$	Static Drain-to-Source on-resistance	—	3.7	4.7	mΩ	$V_{GS}=10V, I_D=106A$
		—	8.4	—		$T_J = 125^\circ\text{C}$
$V_{GS(th)}$	Gate threshold voltage	2.0	—	4.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
		—	2.2	—		$T_J = 125^\circ\text{C}$
I_{DSS}	Drain-to-Source leakage current	—	—	1	μA	$V_{DS} = 120V, V_{GS} = 0V$
		—	—	50		$T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source forward leakage	—	—	100	nA	$V_{GS} = 20V$
		—	—	-100		$V_{GS} = -20V$
Q_g	Total gate charge	—	224	—	nC	$I_D = 50A,$ $V_{DS}=50V,$ $V_{GS} = 10V$
Q_{gs}	Gate-to-Source charge	—	80	—		
Q_{gd}	Gate-to-Drain("Miller") charge	—	55	—		
$t_{d(on)}$	Turn-on delay time	—	40	—	nS	$V_{GS}=10V, V_{DD}=65V,$ $R_L=0.87\Omega,$ $R_{GEN}=2.6\Omega$ $I_D=75A$
t_r	Rise time	—	141	—		
$t_{d(off)}$	Turn-Off delay time	—	95	—		
t_f	Fall time	—	101	—		
C_{iss}	Input capacitance	—	5634	—	pF	$V_{GS} = 0V$
C_{oss}	Output capacitance	—	657	—		$V_{DS} = 50V$
C_{rss}	Reverse transfer capacitance	—	12.6	—		$f = 1MHz$

Source-Drain Ratings and Characteristics

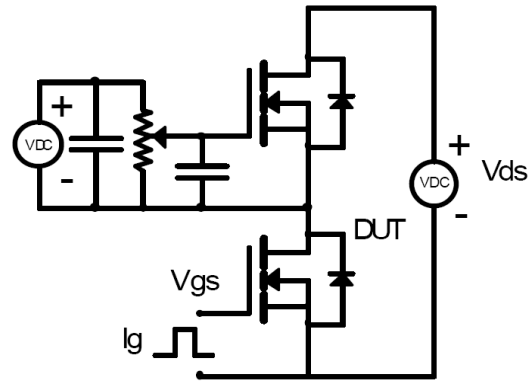
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	180 ①	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode)	—	—	670	A	
V_{SD}	Diode Forward Voltage	—	0.9	1.3	V	

Test circuits and Waveforms

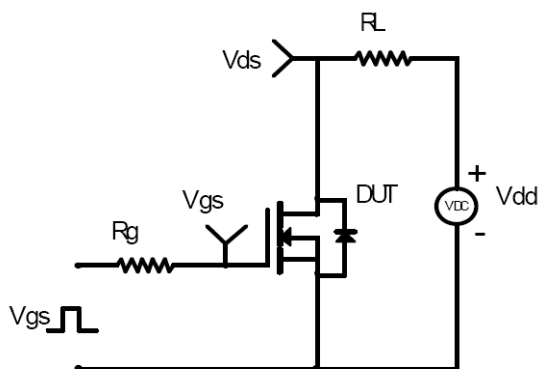
EAS Test Circuit:



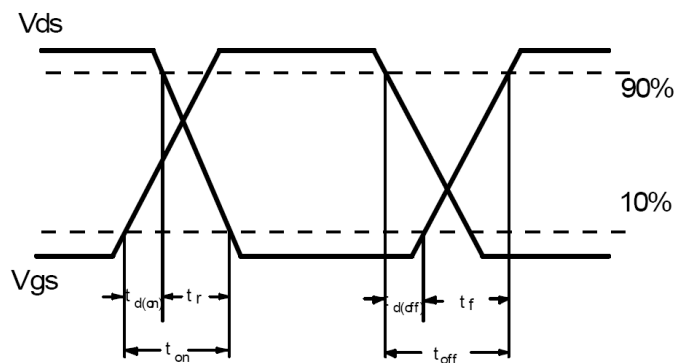
Gate charge test circuit:



Switching Time Test Circuit:



Switching Waveforms:



Notes:

- ① Calculated continuous current based on maximum allowable junction temperature.
- ② Repetitive rating; pulse width limited by max. junction temperature.
- ③ The power dissipation PD is based on max. junction temperature, using junction-to-case thermal resistance.
- ④ The value of $R_{\theta JA}$ is measured with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with $T_A = 25^\circ\text{C}$

Typical electrical and thermal characteristics

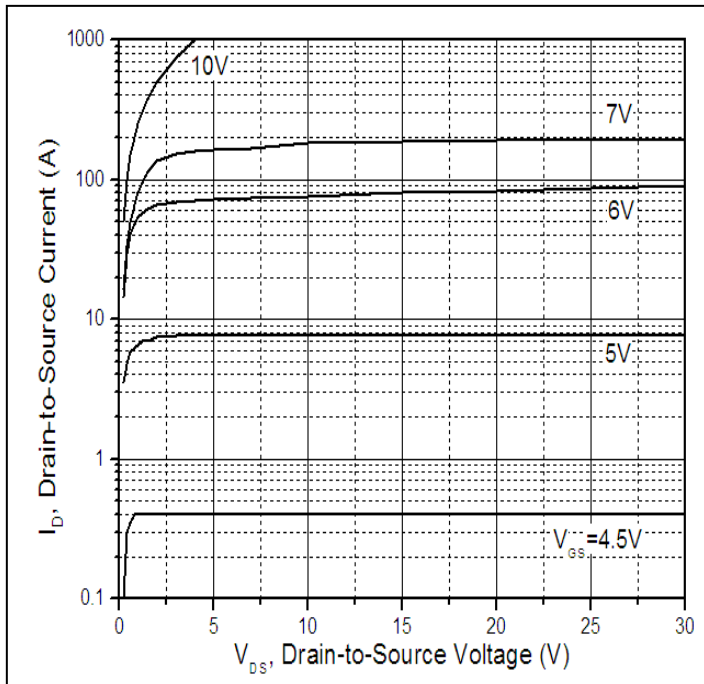


Figure 1: Typical Output Characteristics

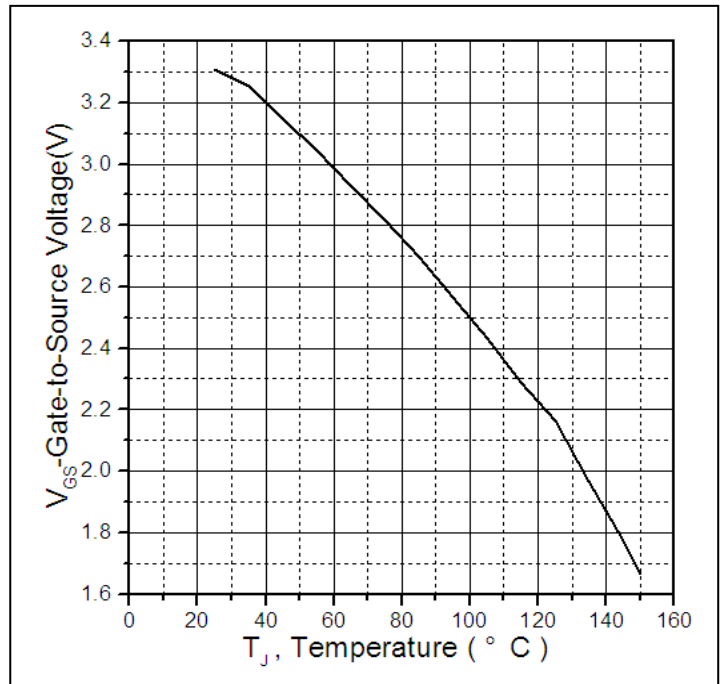


Figure 2. Gate to source cut-off voltage

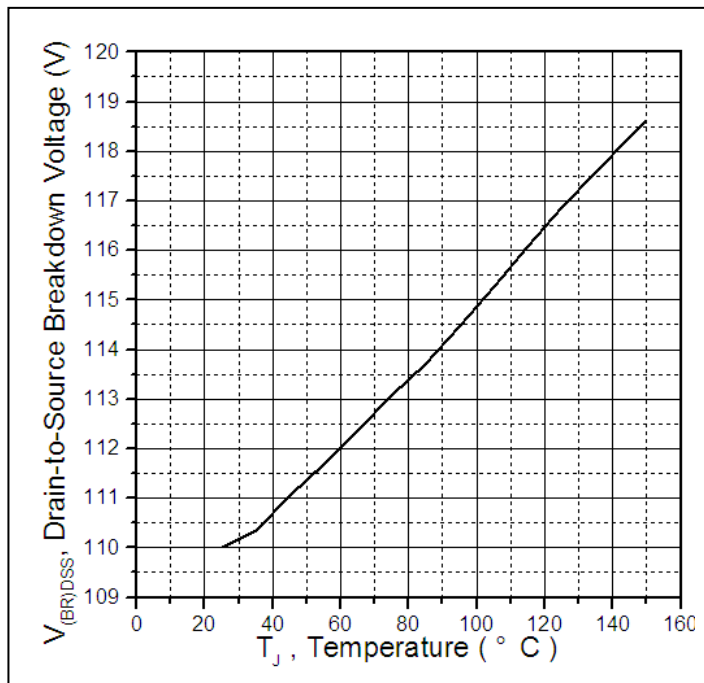


Figure 3. Drain-to-Source Breakdown Voltage Vs. Case Temperature

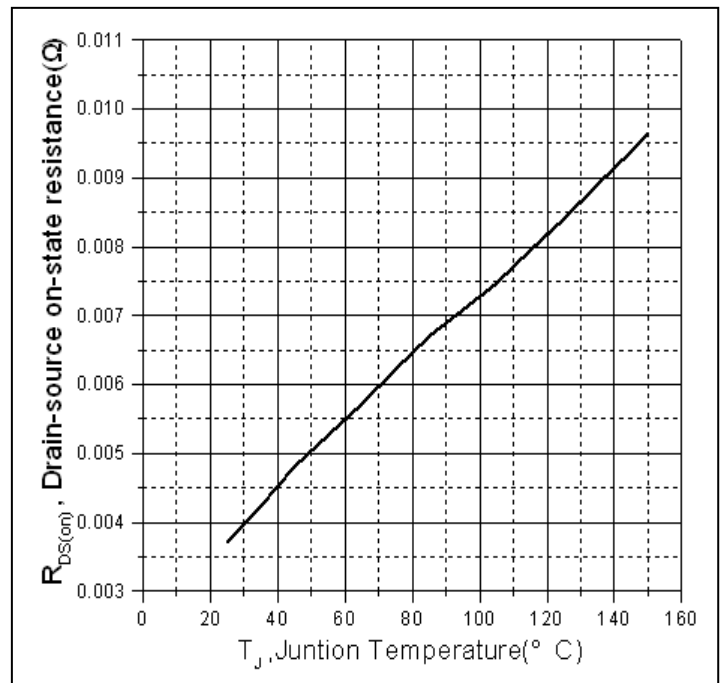


Figure 4: Normalized On-Resistance Vs. Case Temperature

Typical electrical and thermal characteristics

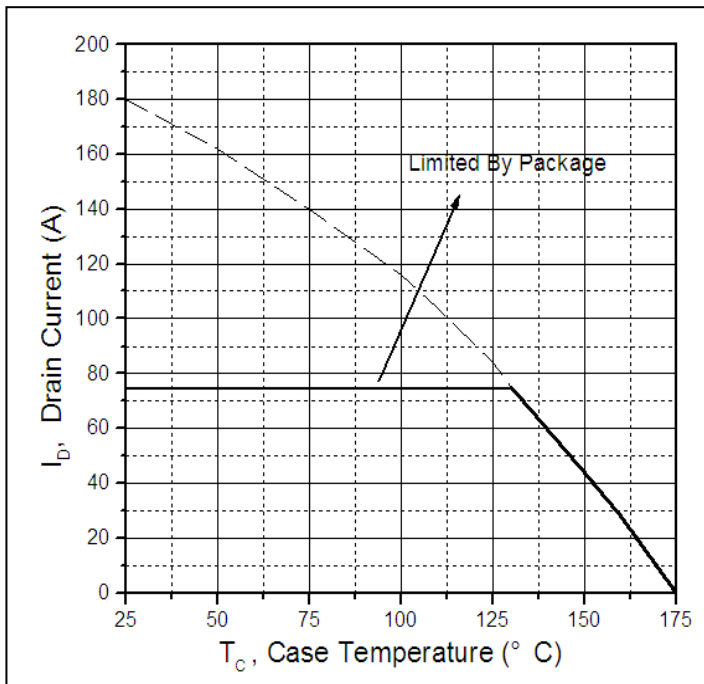


Figure 5. Maximum Drain Current Vs. Case Temperature

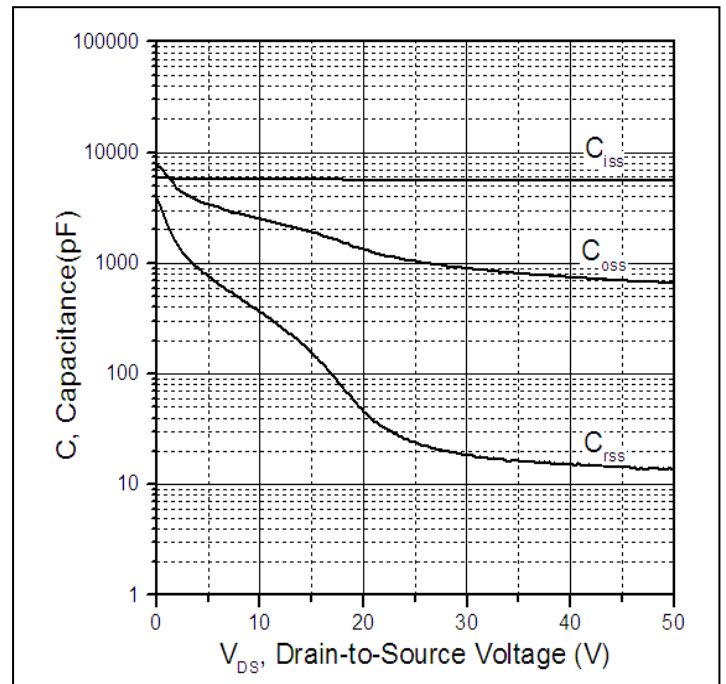


Figure 6. Typical Capacitance Vs. Drain-to-Source Voltage

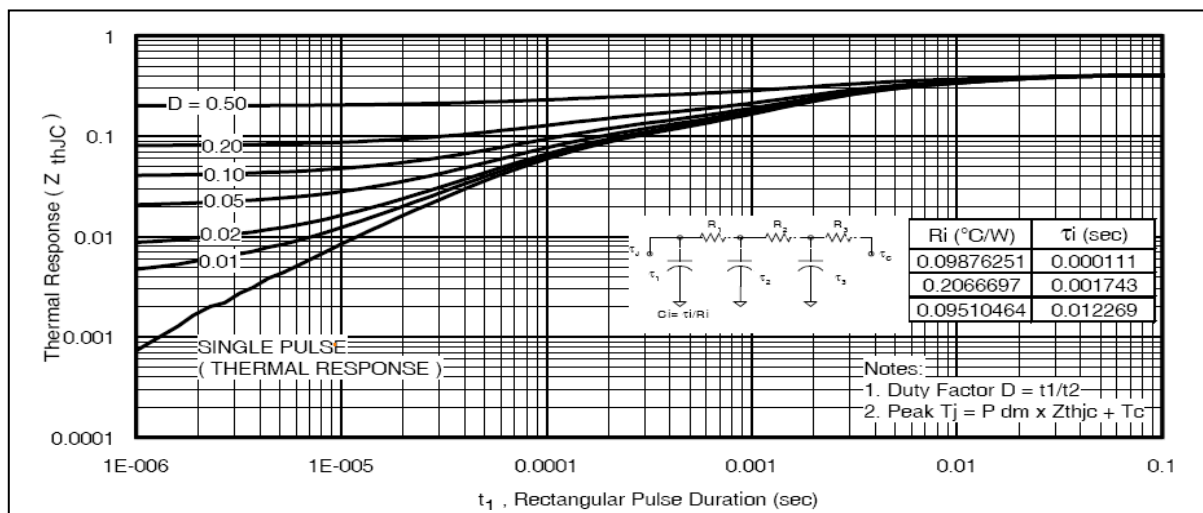
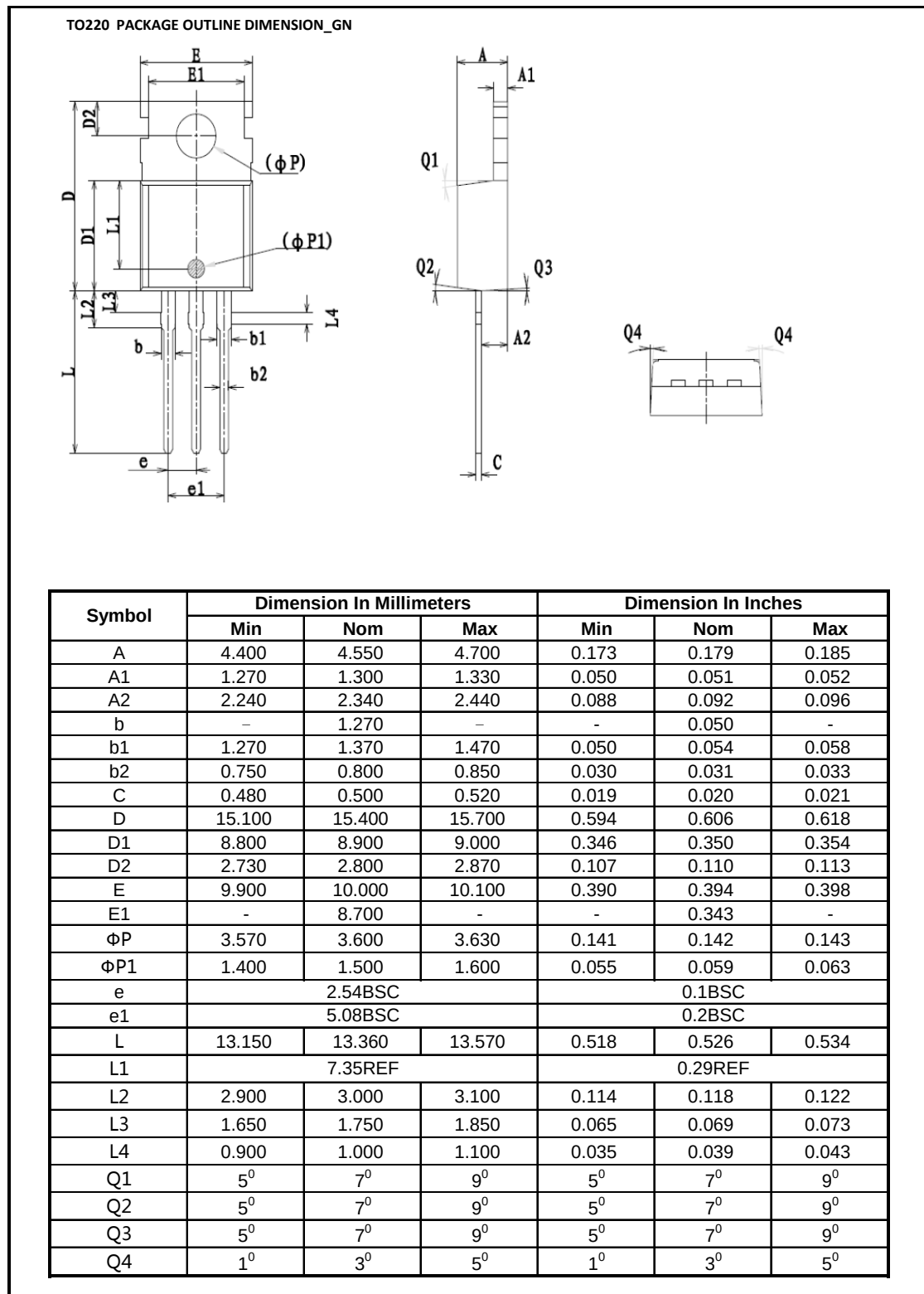


Figure7. Maximum Effective Transient Thermal Impedance, Junction-to-Case

Mechanical Data:



Ordering and Marking Information**Device Marking: SSS1004****Package (Available)****TO-220****Operating Temperature Range****C : -55 to 175 °C****Devices per Unit**

Package Type	Units/ Tube	Tubes/Inner Box	Units/Inner Box	Inner Boxes/Carton Box	Units/Carton Box
TO-220	50	20	1000	6	6000

Reliability Test Program

Test Item	Conditions	Duration	Sample Size
High Temperature Reverse Bias(HTRB)	$T_j=125^{\circ}\text{C}$ to 175°C @ 80% of Max $V_{DSS}/V_{CES}/V_R$	168 hours 500 hours 1000 hours	3 lots x 77 devices
High Temperature Gate Bias(HTGB)	$T_j=125^{\circ}\text{C}$ or 175°C @ 100% of Max V_{GSS}	168 hours 500 hours 1000 hours	3 lots x 77 devices

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