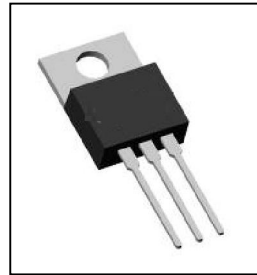
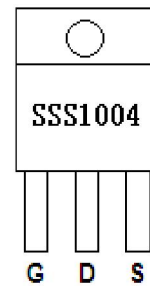


Main Product Characteristics

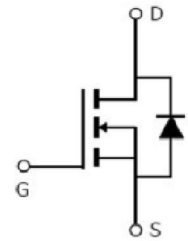
V_{DS}	100V
$R_{DS(on)}$	3.4m Ω (typ.)
I_D	180A ①



TO-220



Marking and Pin Assignment



Schematic Diagram

Features and Benefits

- Advanced Process Technology
- Special designed for PWM, load switching and general purpose applications
- Ultra low on-resistance with low gate charge
- Fast switching and reverse body recovery
- 175°C operating temperature
- Lead free product



Description

It utilizes the latest processing techniques to achieve the high cell density and reduces the on-resistance with high repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in power switching application and a wide variety of other applications.

Absolute Max Rating

Symbol	Parameter	Max.	Units
I_D @ TC = 25°C	Continuous Drain Current, V_{GS} @ 10V	180 ①	A
I_D @ TC = 100°C	Continuous Drain Current, V_{GS} @ 10V	130 ①	
I_{DM}	Pulsed Drain Current ②	670	
P_D @ TC = 25°C	Power Dissipation ③	375	W
	Linear Derating Factor	2.5	W/°C
V_{DS}	Drain-Source Voltage	100	V
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy @ L=0.3mH	1045	mJ
I_{AS}	Avalanche Current @ L=0.3mH	83.5	A
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +175	°C

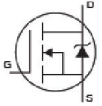
Thermal Resistance

Symbol	Characteristics	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-case ③	—	0.4	°C/W
$R_{\theta JA}$	Junction-to-ambient ($t \leq 10s$) ④	—	62	°C/W
	Junction-to-Ambient (PCB mounted, steady-state) ④	—	40	°C/W

Electrical Characteristics @ $T_A=25^\circ\text{C}$ unless otherwise specified

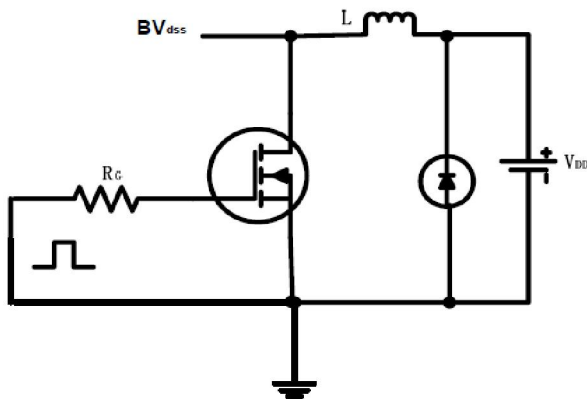
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source breakdown voltage	100	—	—	V	$V_{GS} = 0V, I_D = 1mA$
$R_{DS(on)}$	Static Drain-to-Source on-resistance	—	3.4	4.0	mΩ	$V_{GS}=10V, I_D=75A$
		—	7.7	—		$T_J = 125^\circ\text{C}$
$V_{GS(th)}$	Gate threshold voltage	2.0	—	4.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
		—	2.2	—		$T_J = 125^\circ\text{C}$
I_{DSS}	Drain-to-Source leakage current	—	—	1	μA	$V_{DS} = 120V, V_{GS} = 0V$
		—	—	50		$T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source forward leakage	—	—	100	nA	$V_{GS} = 20V$
		—	—	-100		$V_{GS} = -20V$
Q_g	Total gate charge	—	224	—	nC	$I_D = 50A,$ $V_{DS}=50V,$ $V_{GS} = 10V$
Q_{gs}	Gate-to-Source charge	—	80	—		
Q_{gd}	Gate-to-Drain("Miller") charge	—	55	—		
$t_{d(on)}$	Turn-on delay time	—	40	—	nS	$V_{GS}=10V, V_{DD} = 65V,$ $R_L=0.87\Omega,$ $R_{GEN}=2.6\Omega$ $I_D = 75A$
t_r	Rise time	—	141	—		
$t_{d(off)}$	Turn-Off delay time	—	95	—		
t_f	Fall time	—	101	—		
C_{iss}	Input capacitance	—	5634	—	pF	$V_{GS} = 0V$
C_{oss}	Output capacitance	—	657	—		$V_{DS} = 50V$
C_{rss}	Reverse transfer capacitance	—	12.6	—		$f = 1MHz$

Source-Drain Ratings and Characteristics

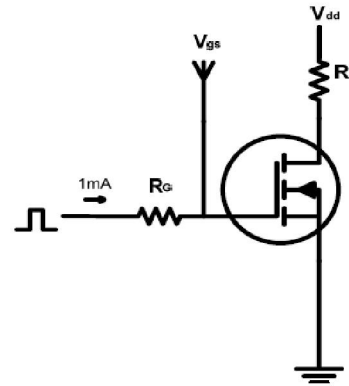
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	180 ①	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode)	—	—	670	A	
V_{SD}	Diode Forward Voltage	—	0.9	1.3	V	

Test Circuits and Waveforms

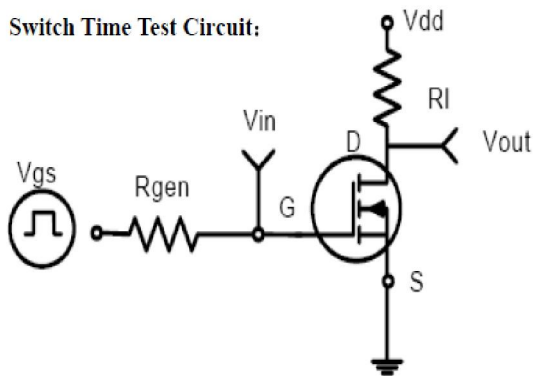
EAS test circuits:



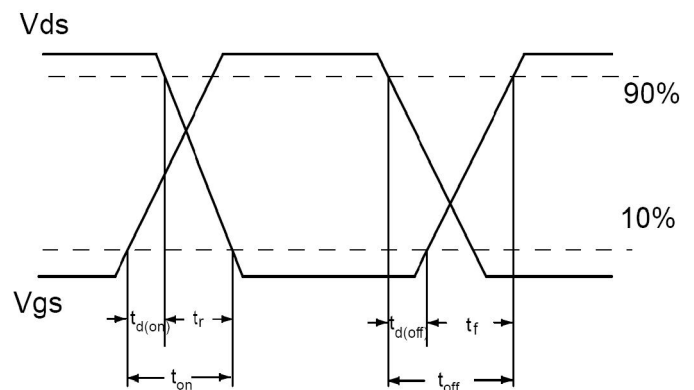
Gate charge test circuit:



Switch Time Test Circuit:



Switch Waveforms:



Notes:

- ① Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 75A.
- ② Repetitive rating; pulse width limited by max. junction temperature.
- ③ The power dissipation PD is based on max. junction temperature, using junction-to-case thermal resistance.
- ④ The value of $R_{\theta JA}$ is measured with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with $T_A = 25^\circ\text{C}$

Typical Electrical and Thermal Characteristics

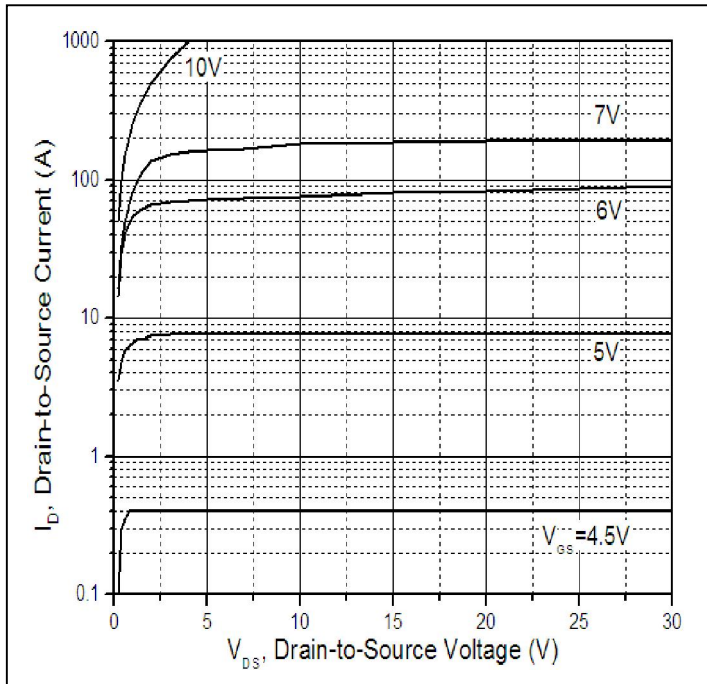


Figure 1: Typical Output Characteristics

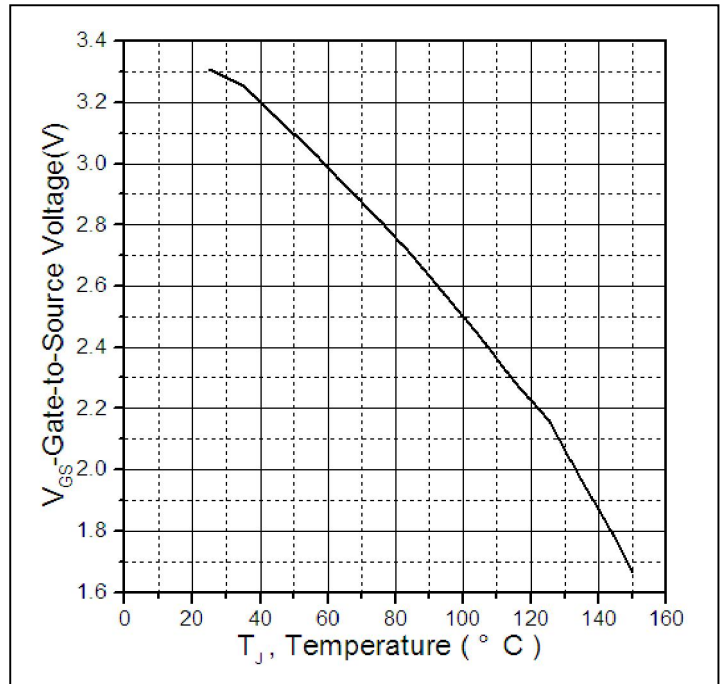


Figure 2: Gate to source cut-off voltage

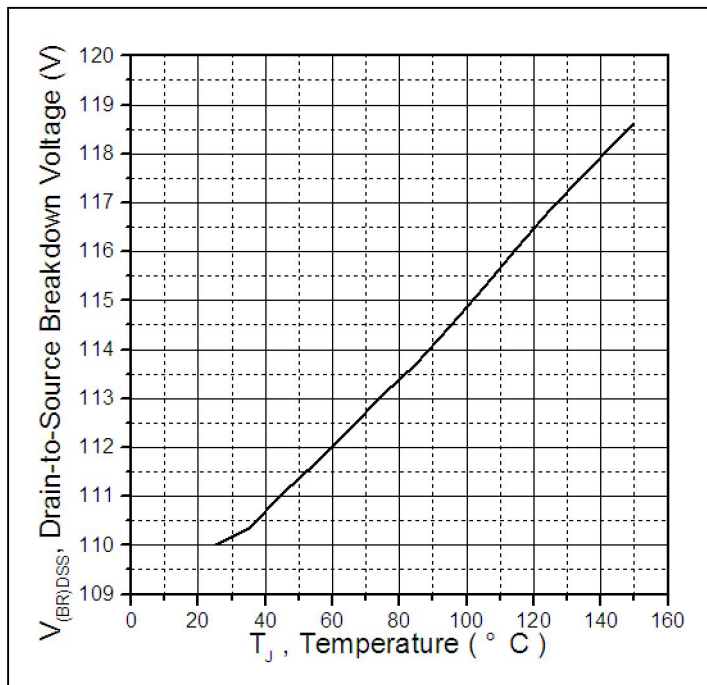


Figure 3: Drain-to-Source Breakdown Voltage Vs. Case Temperature

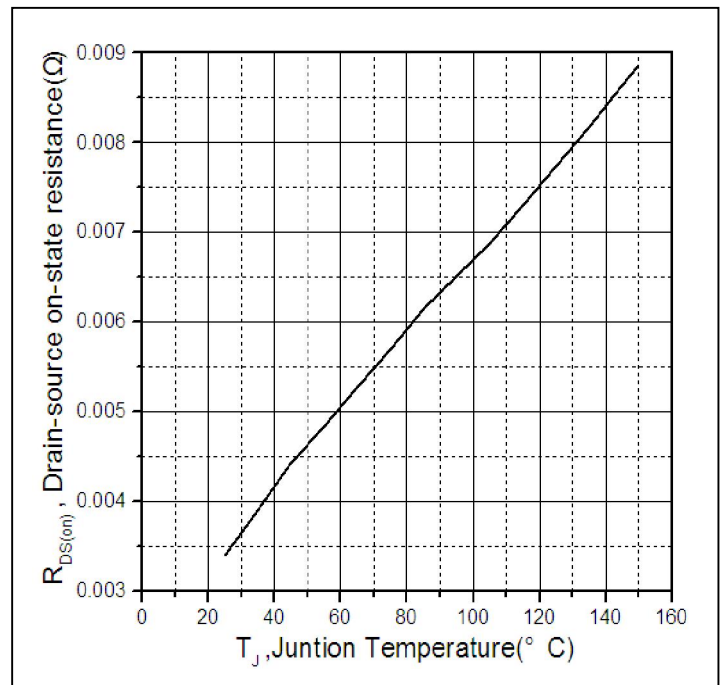


Figure 4: Normalized On-Resistance Vs. Case Temperature

Typical Electrical and Thermal Characteristics

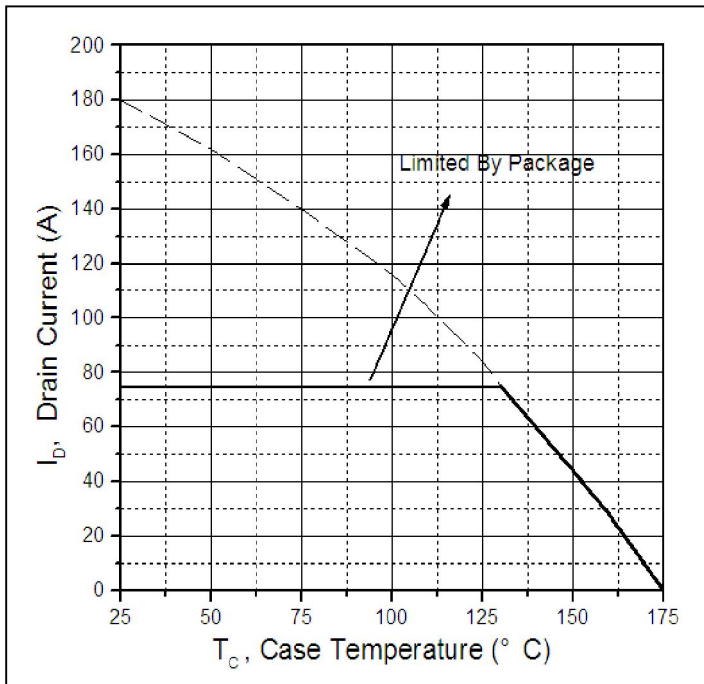


Figure 5. Maximum Drain Current Vs. Case Temperature

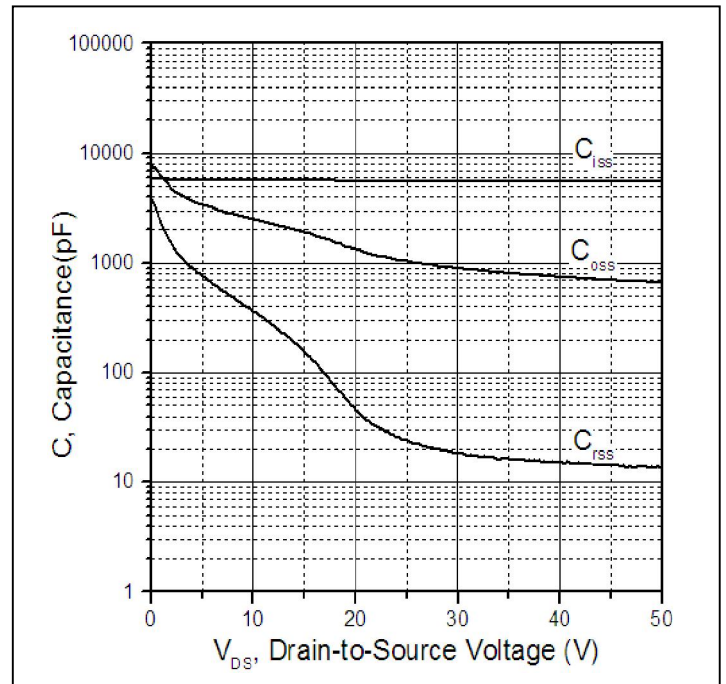


Figure 6. Typical Capacitance Vs. Drain-to-Source Voltage

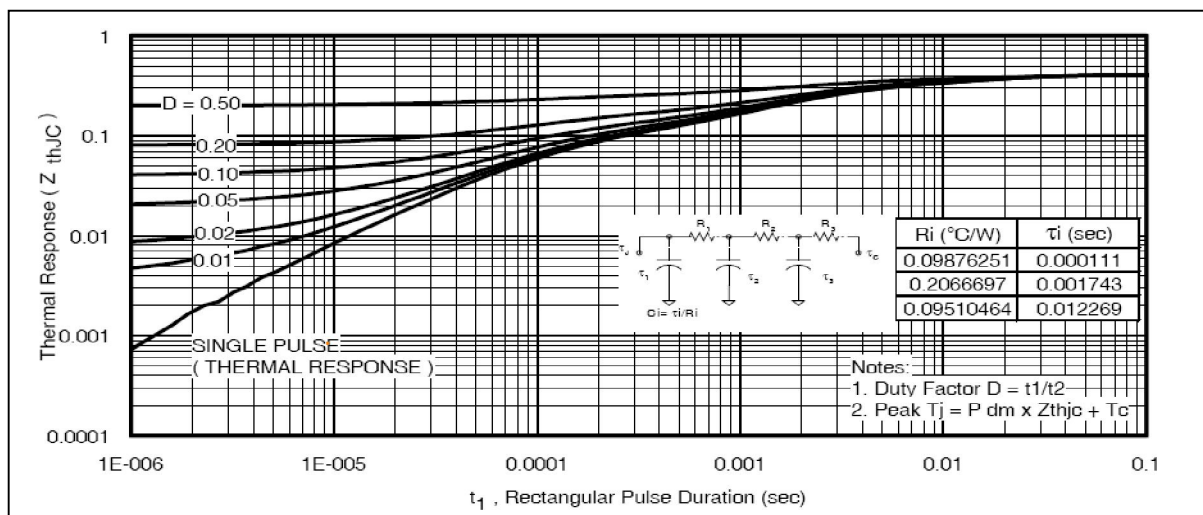
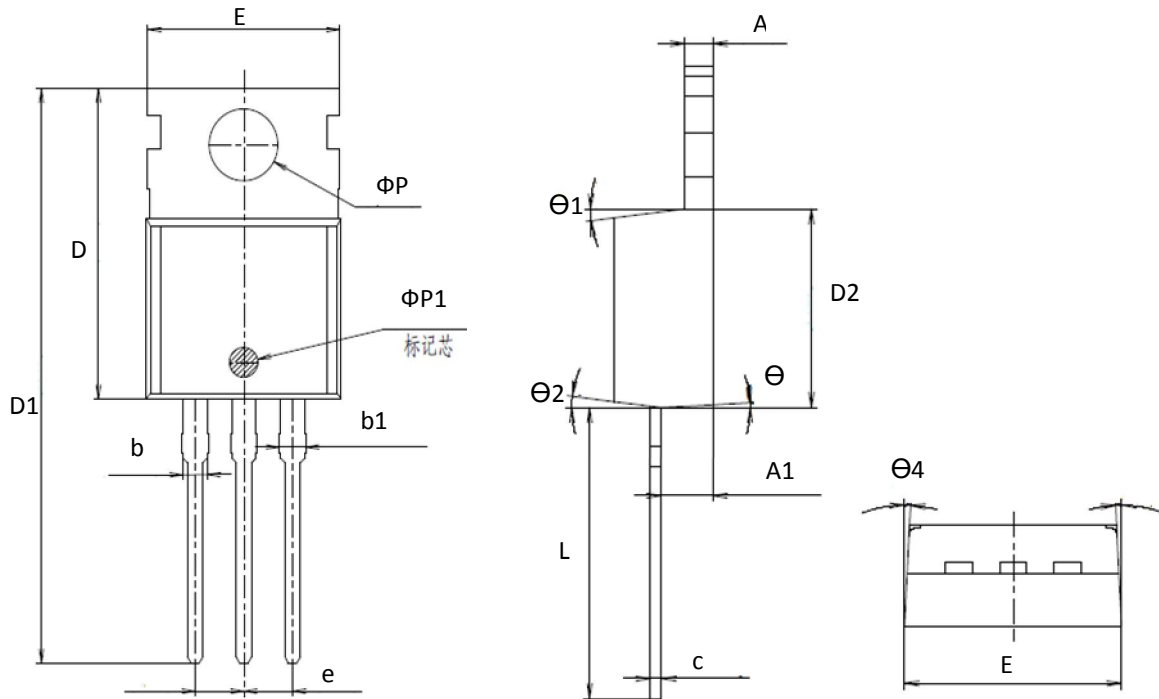


Figure7. Maximum Effective Transient Thermal Impedance, Junction-to-Case

Mechanical Data

TO-220 PACKAGE OUTLINE DIMENSION_GN



Symbol	Dimension In Millimeters			Dimension In Inches		
	Min	Nom	Max	Min	Nom	Max
A	-	1.300	-	-	0.051	-
A1	2.200	2.400	2.600	0.087	0.094	0.102
b	-	1.270	-	-	0.050	-
b1	1.270	1.370	1.470	0.050	0.054	0.058
c	-	0.500	-	-	0.020	-
D	-	15.600	-	-	0.614	-
D1	-	28.700	-	-	1.130	-
D2	-	9.150	-	-	0.360	-
E	9.900	10.000	10.100	0.390	0.394	0.398
E1	-	10.160	-	-	0.400	-
ΦP	-	3.600	-	-	0.142	-
ΦP1		1.500			0.059	
e	2.54BSC			0.1BSC		
L	12.900	13.100	13.300	0.508	0.516	0.524
Θ1	-	7°	-	-	7°	-
Θ2	-	7°	-	-	7°	-
Θ3	-	3°	-	5°	7°	9°
Θ4	-	3°	-	1°	3°	5°

**SSS1004****100V N-Channel MOSFET**

Ordering and Marking Information

Device Marking: SSS1004**Package (Available)****TO-220****Operating Temperature Range****C : -55 to 175 °C**

Devices per Unit

Package Type	Units/Tube	Tubes/Inner Box	Units/Inner Box	Inner Boxes/Carton Box	Units/Carton Box
TO-220	50	20	1000	6	6000

Reliability Test Program

Test Item	Conditions	Duration	Sample Size
High Temperature Reverse Bias(HTRB)	$T_j=125^{\circ}\text{C}$ to 175°C @ 80% of Max $V_{\text{DSS}}/V_{\text{CES}}/V_{\text{R}}$	168 hours 500 hours 1000 hours	3 lots x 77 devices
High Temperature Gate Bias(HTGB)	$T_j=125^{\circ}\text{C}$ or 175°C @ 100% of Max V_{GSS}	168 hours 500 hours 1000 hours	3 lots x 77 devices