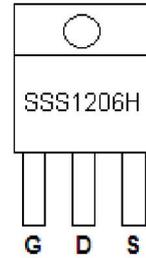


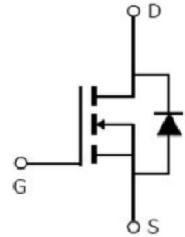
M



TO-247



marking and Pin
Assignment



Schematic Diagram

Features and Benefits

- Advanced Process Technology
- Special designed for PWM, load switching and general purpose applications
- Ultra low on-resistance with low gate charge
- Fast switching and reverse body recovery
- 175°C operating temperature
- Lead free product



Description

It utilizes the latest processing techniques to achieve the high cell density and reduces the on-resistance with high repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in power switching application and a wide variety of other applications.

Absolute Max Rating

Symbol	Parameter	Max.	Units
$I_D @ TC = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	180 ①	A
$I_D @ TC = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	130 ①	
I_{DM}	Pulsed Drain Current ②	670	
$P_D @ TC = 25^\circ C$	Power Dissipation ③	375	W
	Linear Derating Factor	2.5	W/°C
V_{DS}	Drain-Source Voltage	120	V
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy @ L=0.3mH	1148	mJ
I_{AS}	Avalanche Current @ L=0.3mH	87.5	A
$T_J \quad T_{STG}$	Operating Junction and Storage Temperature Range	-55 to +175	°C

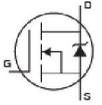
Thermal Resistance

Symbol	Characteristics	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-case ③	—	0.4	°C/W
$R_{\theta JA}$	Junction-to-ambient ($t \leq 10s$) ④	—	62	°C/W
	Junction-to-Ambient (PCB mounted, steady-state) ④	—	40	°C/W

Electrical Characteristics @ $T_A=25^\circ C$ unless otherwise specified

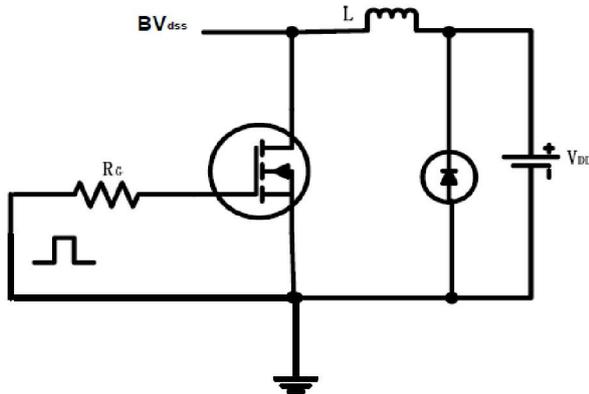
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source breakdown voltage	120	—	—	V	$V_{GS} = 0V, I_D = 1mA$
$R_{DS(on)}$	Static Drain-to-Source on-resistance	—	4.7	6.0	m Ω	$V_{GS}=10V, I_D=75A$
		—	10.6	—		$T_J = 125^\circ C$
$V_{GS(th)}$	Gate threshold voltage	2.0	—	4	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
		—	2.2	—		$T_J = 125^\circ C$
I_{DSS}	Drain-to-Source leakage current	—	—	1	μA	$V_{DS} = 120V, V_{GS} = 0V$
		—	—	50		$T_J = 125^\circ C$
I_{GSS}	Gate-to-Source forward leakage	—	—	100	nA	$V_{GS} = 20V$
		—	—	-100		$V_{GS} = -20V$
Q_g	Total gate charge	—	201	—	nC	$I_D = 50A,$ $V_{DS}=50V,$ $V_{GS} = 10V$
Q_{gs}	Gate-to-Source charge	—	88	—		
Q_{gd}	Gate-to-Drain("Miller") charge	—	36	—		
$t_{d(on)}$	Turn-on delay time	—	41	—	nS	$V_{GS}=10V, V_{DD}=65V,$ $R_L=0.87\Omega,$ $R_{GEN}=2.6\Omega$ $I_D = 75A$
t_r	Rise time	—	114	—		
$t_{d(off)}$	Turn-Off delay time	—	90	—		
t_f	Fall time	—	100	—		
C_{iss}	Input capacitance	—	5634	—	pF	$V_{GS} = 0V$ $V_{DS} = 50V$ $f = 1MHz$
C_{oss}	Output capacitance	—	657	—		
C_{rss}	Reverse transfer capacitance	—	12.6	—		

Source-Drain Ratings and Characteristics

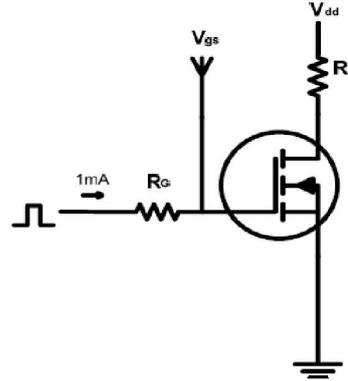
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	180 ①	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode)	—	—	670	A	
V_{SD}	Diode Forward Voltage	—	0.9	1.3	V	

Test Circuits and Waveforms

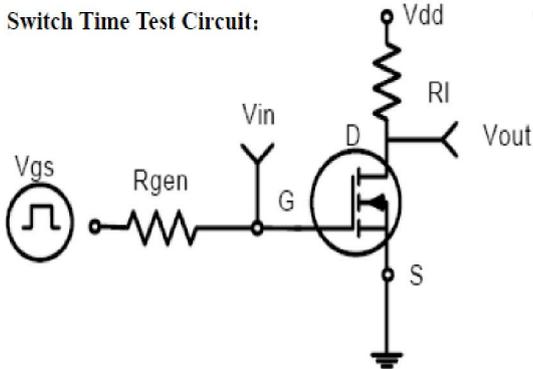
EAS test circuits:



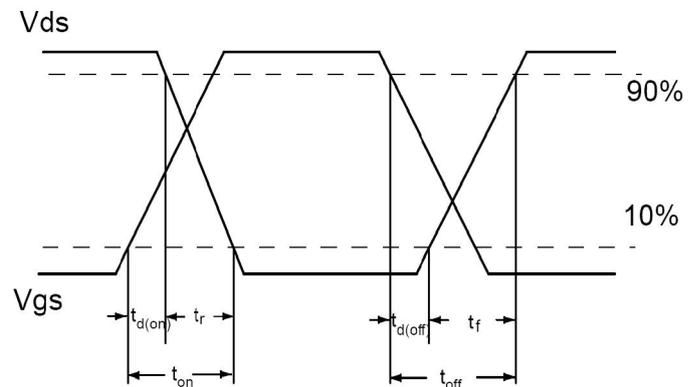
Gate charge test circuit:



Switch Time Test Circuit:



Switch Waveforms:



Notes:

- ① Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 75A.
- ② Repetitive rating; pulse width limited by max. junction temperature.
- ③ The power dissipation PD is based on max. junction temperature, using junction-to-case thermal resistance.
- ④ The value of $R_{\theta JA}$ is measured with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with $T_A = 25^\circ\text{C}$

Typical Electrical and Thermal Characteristics

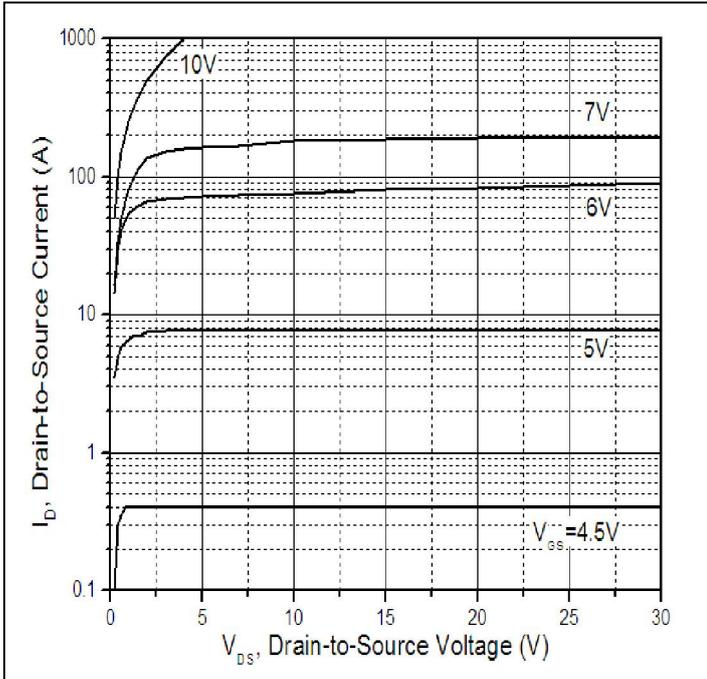


Figure 1: Typical Output Characteristics

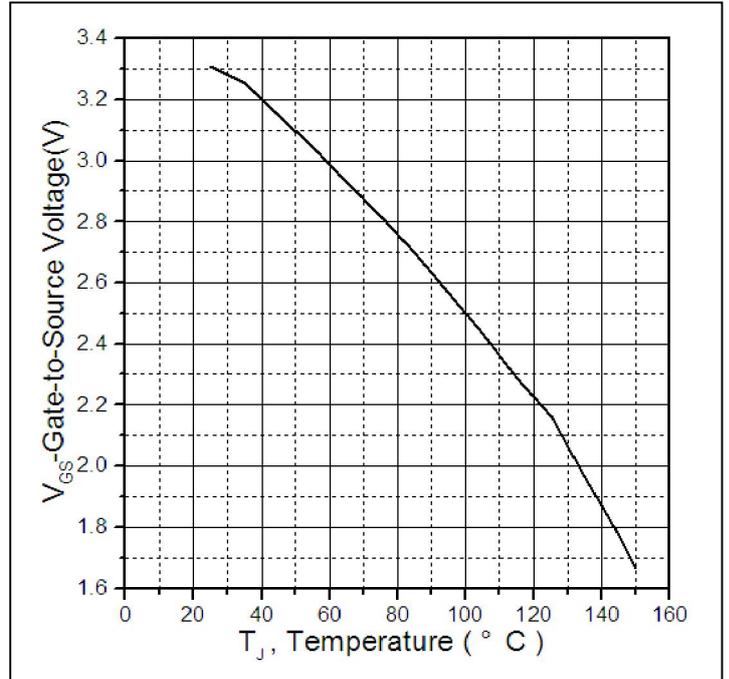


Figure 2. Gate to source cut-off voltage

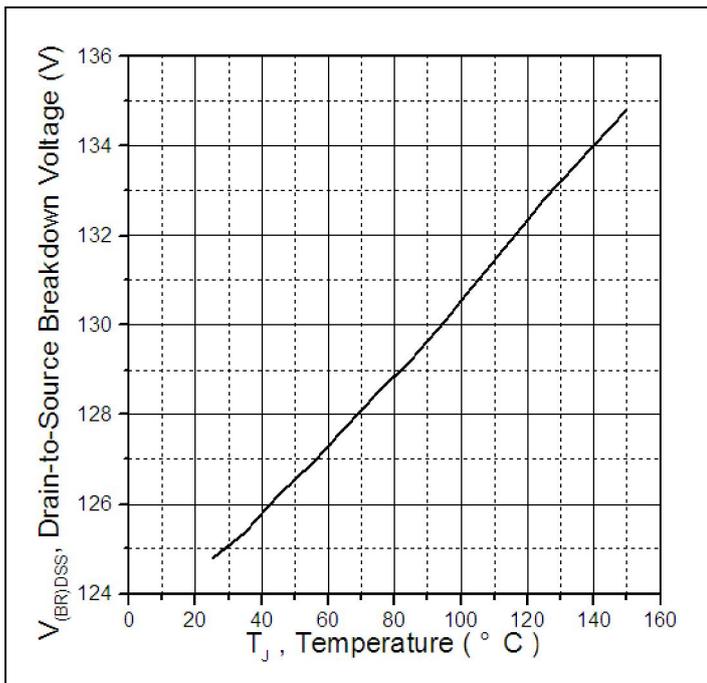


Figure 3. Drain-to-Source Breakdown Voltage Vs. Case Temperature

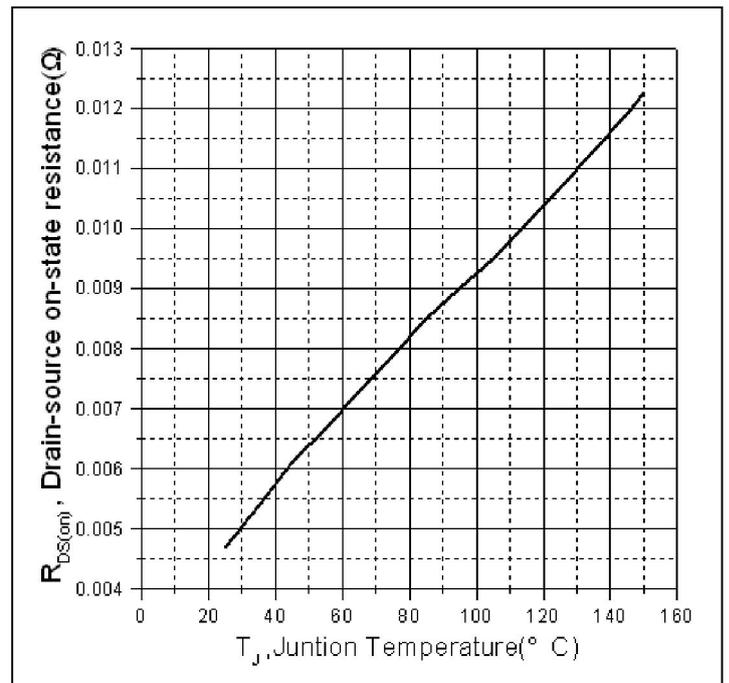


Figure 4: Normalized On-Resistance Vs. Case Temperature

Typical Electrical and Thermal Characteristics

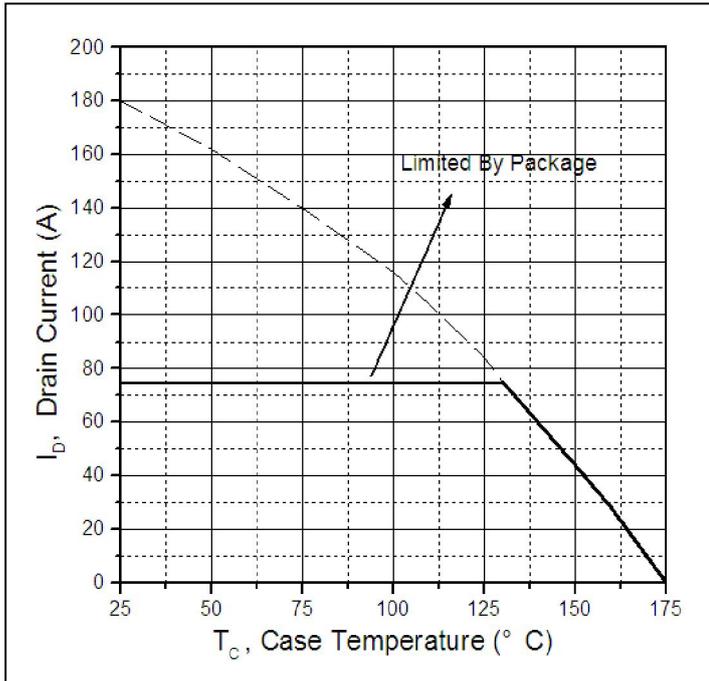


Figure 5. Maximum Drain Current Vs. Case Temperature

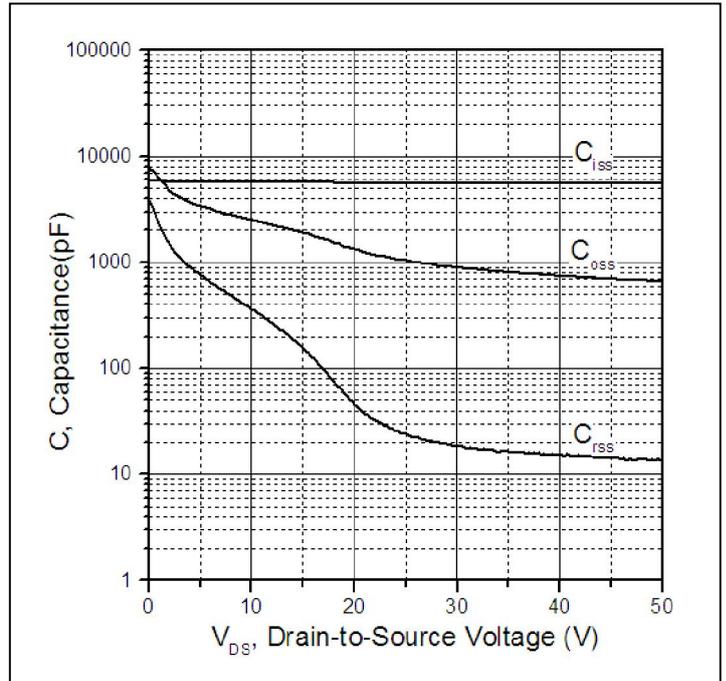


Figure 6. Typical Capacitance Vs. Drain-to-Source Voltage

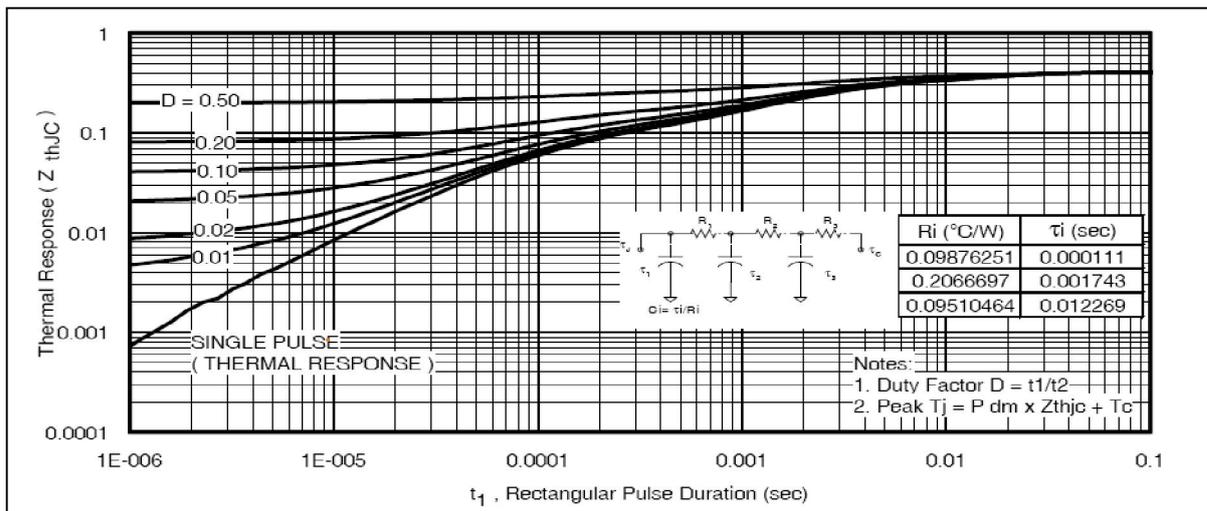
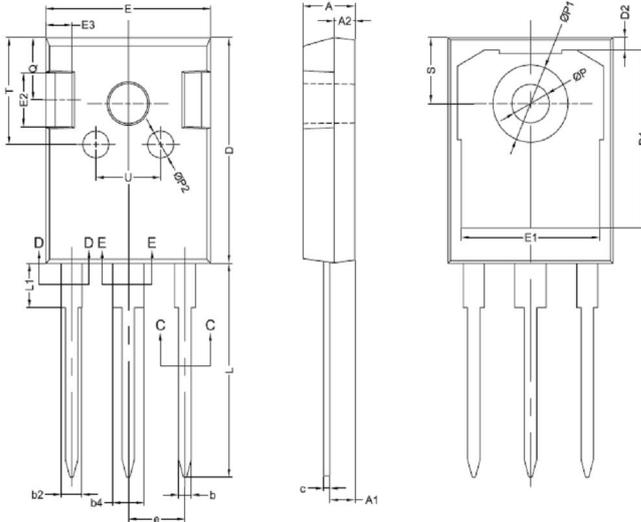


Figure7. Maximum Effective Transient Thermal Impedance, Junction-to-Case

Mechanical Data

TO-247 PACKAGE OUTLINE DIMENSION



Symbol	Dimension In Millimeters			Dimension In Inches		
	Min	Nom	Max	Min	Nom	Max
A	4.900	5.000	5.100	0.193	0.197	0.201
A1	2.300	2.405	2.510	0.091	0.095	0.099
A2	1.900	2.000	2.100	0.075	0.079	0.083
b	1.160	-	1.260	0.046	-	0.050
b1	1.150	1.185	1.220	0.045	0.047	0.048
b2	1.960	-	2.060	0.077	-	0.081
b3	1.950	1.985	2.020	0.077	0.078	0.080
b4	2.960	-	3.060	0.117	-	0.120
b5	2.950	2.985	3.020	0.116	0.118	0.119
c	0.590	-	0.660	0.023	-	0.026
c1	0.580	0.600	0.620	0.023	0.024	0.024
D	20.900	21.000	21.100	0.823	0.827	0.831
D1	16.250	16.550	16.850	0.640	0.652	0.663
D2	1.050	1.200	1.350	0.041	0.047	0.053
E	15.700	15.800	15.900	0.618	0.622	0.626
E1	13.100	13.300	13.500	0.516	0.524	0.531
E2	4.900	5.000	5.100	0.193	0.197	0.201
E3	2.400	2.500	2.600	0.094	0.098	0.102
e	5.44BSC			0.214BSC		
L	19.800	19.950	20.100	0.780	0.785	0.791
L1	-	-	4.300	-	-	0.169
P	3.500	3.600	3.700	0.138	0.142	0.146
P1	-	-	7.400	-	-	0.291
P2	2.400	2.500	2.600	0.094	0.098	0.102
Q	5.600	-	6.000	0.220	-	0.236
S	6.15BSC			0.242BSC		
T	9.800	-	10.200	0.386	-	0.402
U	6.000	-	6.400	0.236	-	0.252



Ordering and Marking Information

Device Marking: SSS1206H

Package (Available)
TO-247
Operating Temperature Range
C : -55 to 175 °C

Devices per Unit

Package Type	Units/Tube	Tubes/Inner Box	Units/Inner Box	Inner Boxes/Carton Box	Units/Carton Box
TO-247	30	11	330	6	1980

Reliability Test Program

Test Item	Conditions	Duration	Sample Size
High Temperature Reverse Bias(HTRB)	$T_j=125^{\circ}\text{C}$ to 175°C @ 80% of Max $V_{\text{DSS}}/V_{\text{CES}}/V_{\text{R}}$	168 hours 500 hours 1000 hours	3 lots x 77 devices
High Temperature Gate Bias(HTGB)	$T_j=125^{\circ}\text{C}$ or 175°C @ 100% of Max V_{GSS}	168 hours 500 hours 1000 hours	3 lots x 77 devices