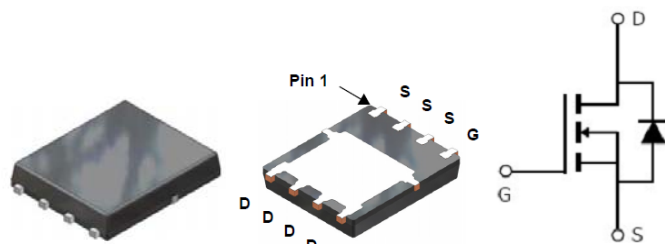


Main Product Characteristics:

V_{DSS}	30V
$R_{DS(on)}$	1.9m Ω (typ.)
I_D	130A



PPAK5*6-8L

Schematic diagram

Features and Benefits:

- Advanced MOSFET process technology
- Special designed for PWM, load switching and general purpose applications
- Ultra low on-resistance with low gate charge
- Fast switching and reverse body recovery
- 150°C operating temperature


Description:

It utilizes the latest processing techniques to achieve the high cell density and reduces the on-resistance with high repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in power switching application and a wide variety of other applications.

Absolute max Rating:

Symbol	Parameter	Max.	Units
I_D @ TC = 25°C	Continuous Drain Current, V_{GS} @ 10V①	130	A
I_D @ TC = 100°C	Continuous Drain Current, V_{GS} @ 10V①	100	
I_{DM}	Pulsed Drain Current②	327	
P_D @TC = 25°C	Power Dissipation③	90	W
V_{DS}	Drain-Source Voltage	30	V
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy ②	152	mJ
I_{AR}	Avalanche Current @ L=0.3mH②	55	A
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C

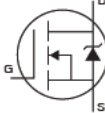
Thermal Resistance

Symbol	Characterizes	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-case ^③	—	2	°C/W
$R_{\theta JA}$	Junction-to-ambient ($t \leq 10s$) ^④	—	50	°C/W

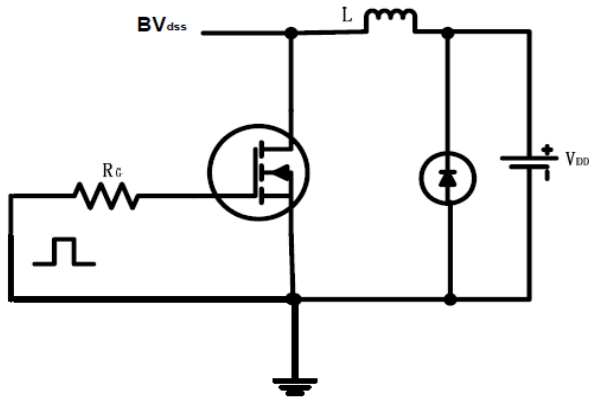
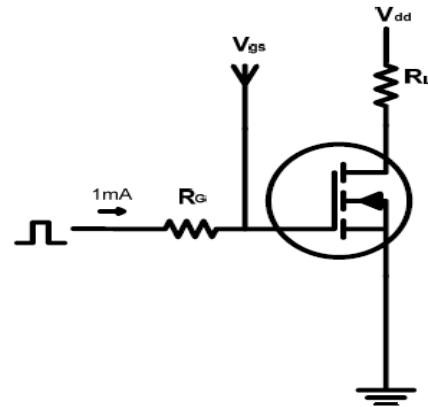
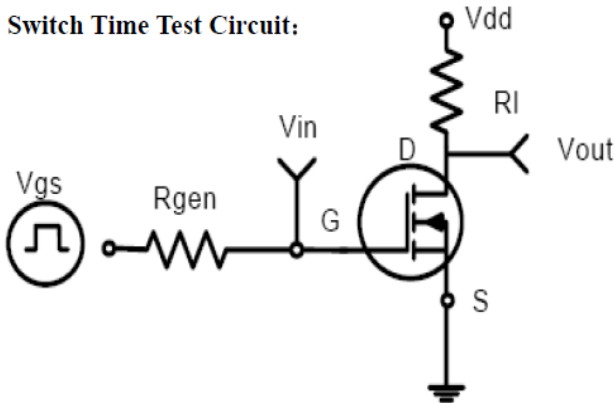
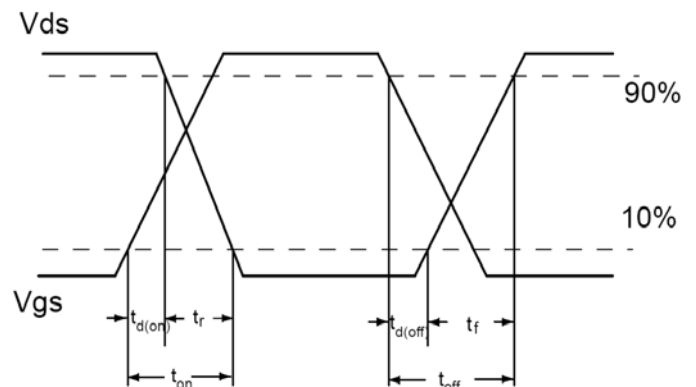
Electrical Characterizes@ $T_A=25^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source breakdown voltage	30	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$R_{DS(on)}$	Static Drain-to-Source on-resistance	—	1.9	2.4	mΩ	$V_{GS}=10V, I_D = 30A$
		—	2.5	3.3		$V_{GS}=4.5V, I_D = 15A$
$R_{DS(on)}$	Static Drain-to-Source on-resistance	—	4	5	mΩ	$V_{GS}=4.5V, I_D = 16A$
		—	5	—		$T_J = 125^\circ\text{C}$
$V_{GS(th)}$	Gate threshold voltage	1	1.6	2.8	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
		—	1.0	—		$T_J = 125^\circ\text{C}$
I_{DSS}	Drain-to-Source leakage current	—	—	1	μA	$V_{DS} = 24V, V_{GS} = 0V$
		—	—	50		$T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source forward leakage	—	—	100	nA	$V_{GS} = 20V$
		—	—	-100		$V_{GS} = -20V$
Q_g	Total gate charge	—	40	—	nC	$V_{DS}=15V,$ $I_D=24A,$ $V_{GS}=4.5V$
Q_{gs}	Gate-to-Source charge	—	6	—		
Q_{gd}	Gate-to-Drain("Miller") charge	—	19	—		
$t_{d(on)}$	Turn-on delay time	—	20	—	ns	$V_{GS}=10V, V_{DS}=15V,$ $R_{GEN}=1\Omega, I_D=1A$
t_r	Rise time	—	32	—		
$t_{d(off)}$	Turn-Off delay time	—	75	—		
t_f	Fall time	—	28	—		
C_{iss}	Input capacitance	—	4800	—	pF	$V_{GS} = 0V$
C_{oss}	Output capacitance	—	735	—		$V_{DS} = 25V$
C_{rss}	Reverse transfer capacitance	—	420	—		$f = 1MHz$

Source-Drain Ratings and Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	130	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode)	—	—	327	A	
V_{SD}	Diode Forward Voltage	—	0.85	1.3	V	$I_S=50A, V_{GS}=0V$
t_{rr}	Reverse Recovery Time	—	49	—	ns	$T_J = 25^\circ\text{C}, I_F = 1A,$ $di/dt = 100A/\mu s$
Q_{rr}	Reverse Recovery Charge	—	18	—	nC	

Test circuits and Waveforms

EAS test circuits:

Gate charge test circuit:

Switch Time Test Circuit:

Waveforms:


Notes:

- ① The maximum current rating is limited by bond-wires.
- ② Repetitive rating; pulse width limited by max. junction temperature.
- ③ The power dissipation P_D is based on max. junction temperature, using junction-to-case thermal resistance.
- ④ The value of $R_{\theta JA}$ is measured with the device mounted on 1in 2 FR-4 board with 2oz. Copper, in a still air environment with $T_A = 25^\circ\text{C}$
- ⑤ These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)} = 175^\circ\text{C}$.

Typical electrical characteristics

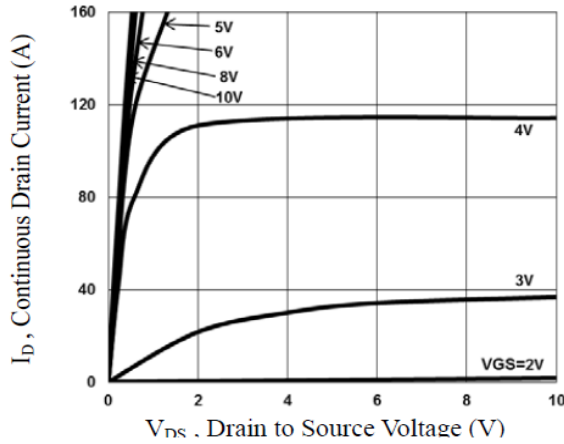


Figure 1: Typical Output Characteristics

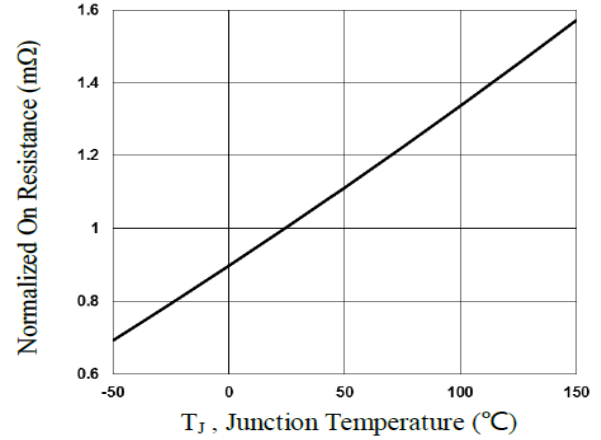


Figure 2: Normalized RDSON vs. TJ

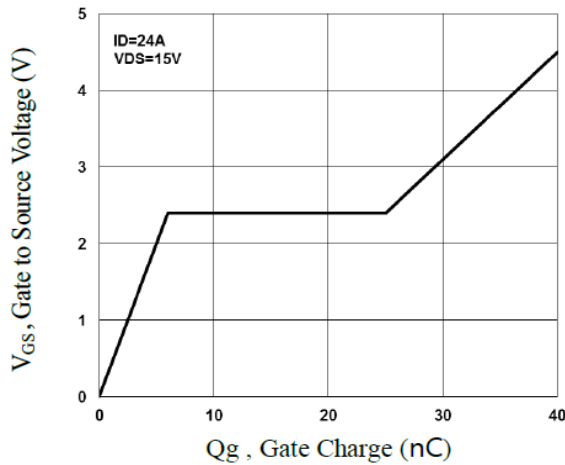


Figure 3: Gate-Charge Characteristics

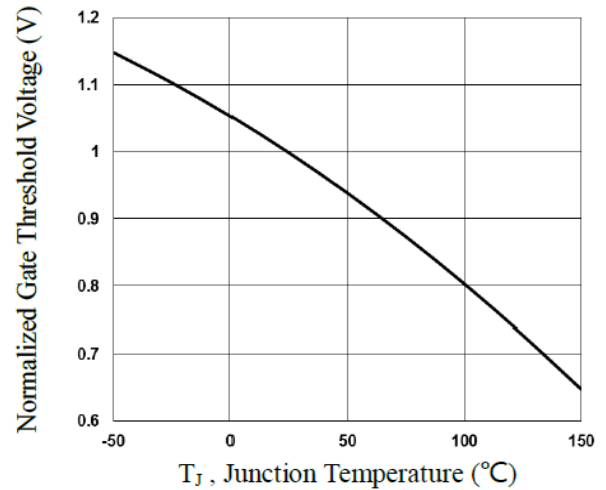


Figure 4: Normalized Vth vs. TJ

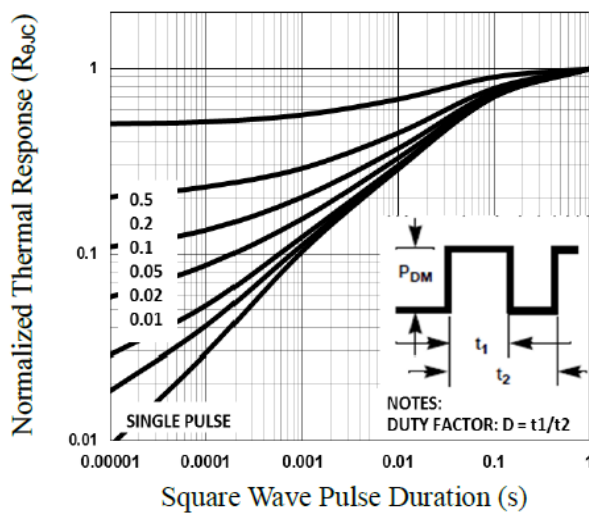


Figure 5: Normalized Thermal transient Impedance Curve

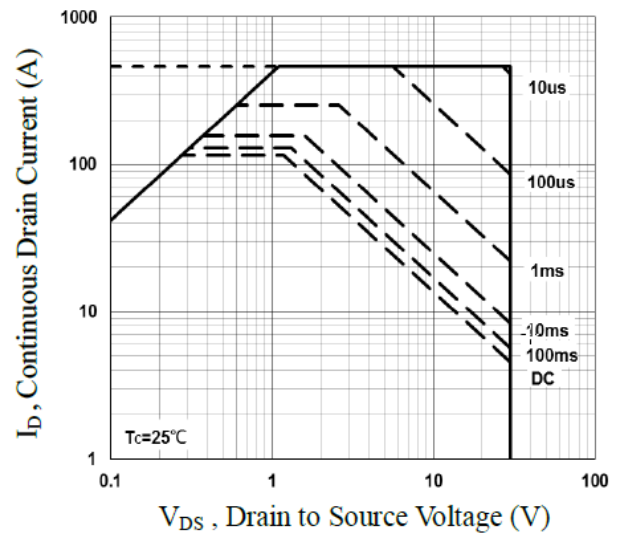
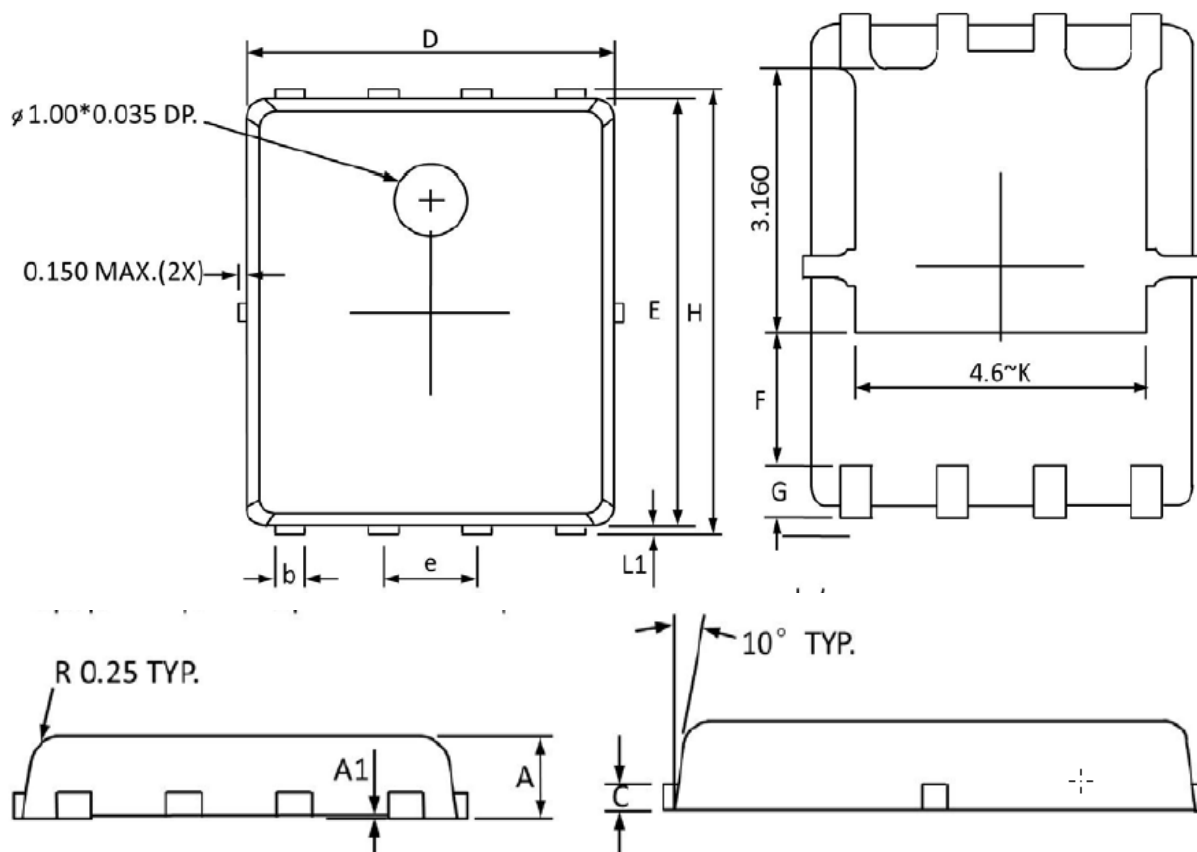


Figure 6: Maximum Safe Operation Area

Mechanical Data:
PPAK5x6 PACKAGE INFORMATION


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.800	1.000	0.032	0.039
A1	0.000	0.005	0.000	0.000
b	0.350	0.490	0.014	0.019
C	0.254 Ref		0.254 Ref	
D	4.900	5.100	0.193	0.200
E	5.700	5.900	0.225	0.232
e	1.27 BSC		1.27 BSC	
F	1.600 Ref		1.600 Ref	
G	0.600 Ref		0.600 Ref	
H	5.950	6.200	0.235	0.244
L1	0.100	0.180	0.004	0.007
K	3.200 Ref		3.200 Ref	

Ordering and Marking Information**Device Marking: SSF3960J7-HF****Package (Available)****PPAK 5*6-8L****Operating Temperature Range****C : -55 to 150 °C****Devices per Unit**

Package Type	Units/ Tube	Tubes/Inner Box	Units/Inner Box	Inner Boxes/Carton Box	Units/Carton Box
PPAK5*6	5000	1	5000	5	25000

Reliability Test Program

Test Item	Conditions	Duration	Sample Size
High Temperature Reverse Bias(HTRB)	$T_J=125^{\circ}\text{C}$ to 150°C @ 80% of Max $V_{DSS}/V_{CES}/V_R$	168 hours 500 hours 1000 hours	3 lots x 77 devices
High Temperature Gate Bias(HTGB)	$T_J=125^{\circ}\text{C}$ to 150°C @ 100% of Max V_{GSS}	168 hours 500 hours 1000 hours	3 lots x 77 devices

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