



SSF2649

20V Dual P-Channel MOSFET

DESCRIPTION

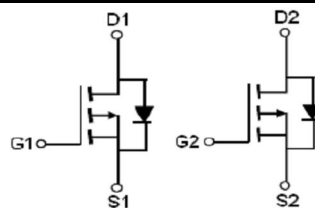
The SSF2649 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge. It has been optimized for power management applications requiring a wide range of gate drive voltage ratings.

GENERAL FEATURES

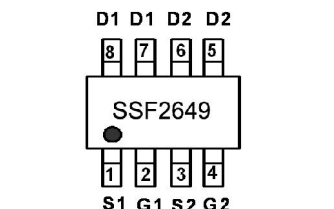
- $V_{DS} = -20V, I_D = -2.9A$
 $R_{DS(ON)} < 98m\Omega @ V_{GS} = -2.5V$
 $R_{DS(ON)} < 58m\Omega @ V_{GS} = -4.5V$
- High Power and current handling capability
- Lead free product
- Surface Mount Package

APPLICATIONS

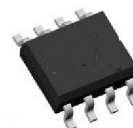
- Battery protection
- Load switch
- Power management



Schematic Diagram



Marking and Pin Assignment



SOP-8 Top View

PACKAGE MARKING AND ORDERING INFORMATION

Device Marking	Device	Device Package	Reel Size	Tape Width	Quantity
SSF2649	SSF2649	SOP-8	-	-	-

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-20	V
Gate-Source Voltage	V_{GS}	± 12	V
Drain Current-Continuous@ Current-Pulsed (Note 1)	I_D	-7.9	A
	I_{DM}	-30	A
Maximum Power Dissipation	P_D	5	W
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	$^\circ C$

THERMAL CHARACTERISTICS

Thermal Resistance, Junction-to-Ambient (Note 2)	$R_{\theta JA}$	85	$^\circ C/W$
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ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0V, I_D = -250\mu A$	-20			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -20V, V_{GS} = 0V$			-1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS} = \pm 12V, V_{DS} = 0V$			± 100	nA



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ON CHARACTERISTICS (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-0.7		-3.0	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=-4.5V, I_D=-2.9A$		49	58	mΩ
		$V_{GS}=-2.7V, I_D=-1.5A$		82	98	
DYNAMIC CHARACTERISTICS (Note4)						
Input Capacitance	C_{iss}	$V_{DS}=-20V, V_{GS}=0V,$ $F=1.0MHz$		1040		PF
Output Capacitance	C_{oss}			156		PF
Reverse Transfer Capacitance	C_{rss}			112		PF
SWITCHING CHARACTERISTICS (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=-10V, I_D=-1A$ $V_{GS}=-4.5V, R_{GEN}=6\Omega$		9		nS
Turn-on Rise Time	t_r			8		nS
Turn-Off Delay Time	$t_{d(off)}$			87		nS
Turn-Off Fall Time	t_f			38		nS
Total Gate Charge	Q_g	$V_{DS}=-10V,$ $I_D=-4.7A, V_{GS}=-4.5V$		12		nC
Gate-Source Charge	Q_{gs}			2.7		nC
Gate-Drain Charge	Q_{gd}			1.5		nC
DRAIN-SOURCE DIODE CHARACTERISTICS						
Diode Forward Voltage (Note 3)	V_{SD}	$V_{GS}=0V, I_S=-2.9A$			-1.0	V

NOTES:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production testing.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

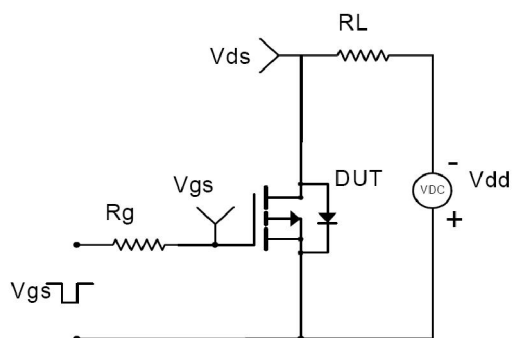


Figure 1: Switching Test Circuit

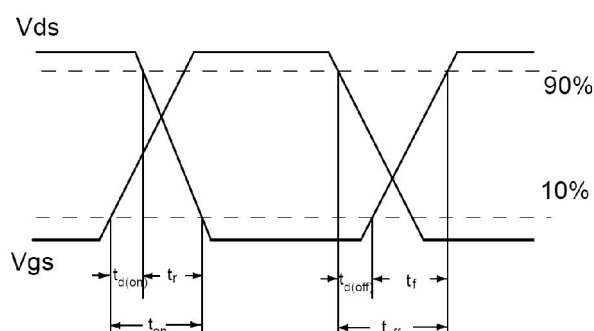


Figure 2: Switching Waveforms

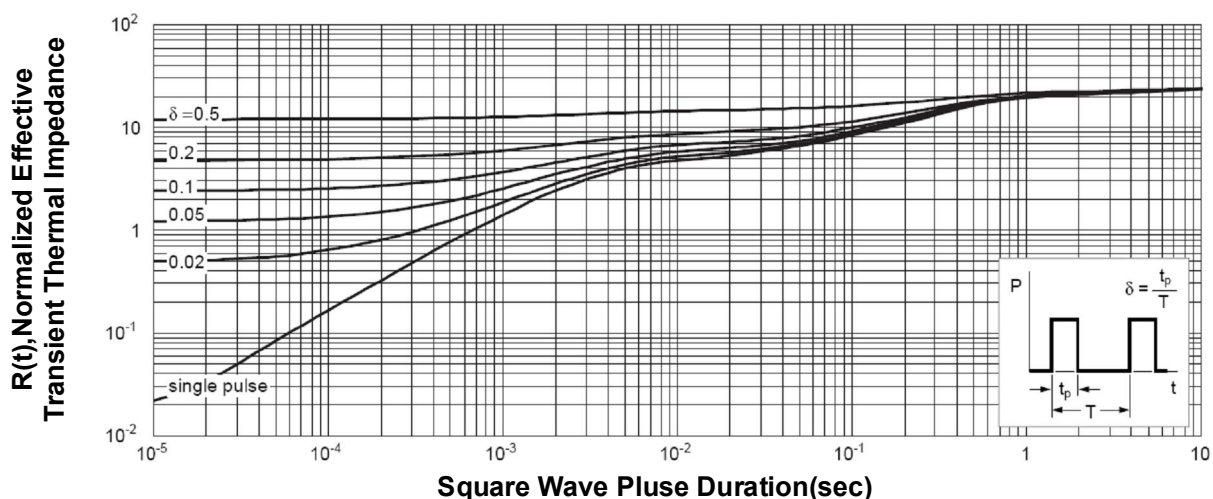
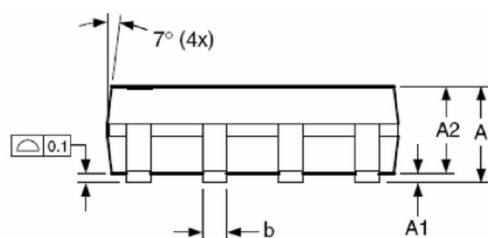
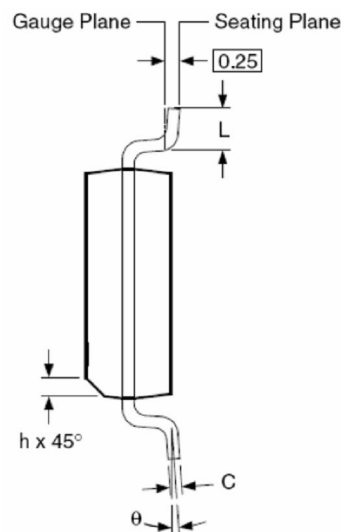
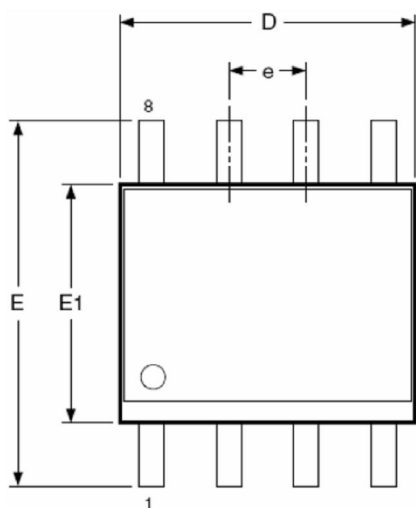
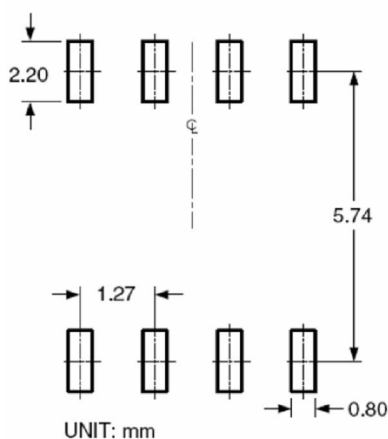


Figure 3 Normalized Maximum Transient Thermal Impedance

SOP-8 PACKAGE INFORMATION



RECOMMENDED LAND PATTERN



Dimensions in millimeters

Symbols	Min.	Nom.	Max.
A	1.35	1.65	1.75
A1	0.10	—	0.25
A2	1.25	1.50	1.65
b	0.31	—	0.51
c	0.17	—	0.25
D	4.80	4.90	5.00
E1	3.80	3.90	4.00
e	1.27 BSC		
E	5.80	6.00	6.20
h	0.25	—	0.50
L	0.40	—	1.27
θ	0°	—	8°

Dimensions in inches

Symbols	Min.	Nom.	Max.
A	0.053	0.065	0.069
A1	0.004	—	0.010
A2	0.049	0.059	0.065
b	0.012	—	0.020
c	0.007	—	0.010
D	0.189	0.193	0.197
E1	0.150	0.154	0.157
e	0.050 BSC		
E	0.228	0.236	0.244
h	0.010	—	0.020
L	0.016	—	0.050
θ	0°	—	8°

NOTES:

1. Dimensions are inclusive of plating
2. Package body sizes exclude mold flash and gate burrs. Mold flash at the non-lead sides should be less than 6 mils.
3. Dimension L is measured in gauge plane.
4. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.