



N-Channel Enhancement Mode Field Effect Transistor

General Description

These are N-Channel enhancement mode silicon gate power field effect transistors. They are advanced power MOSFETs designed, this advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switch mode power supply, power factor correction, electronic lamp ballast based on half bridge.

Features

- 4.5A, 600V(See Note), $R_{DS(on)} < 2.5\Omega @ V_{GS} = 10V$
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability
- Equivalent Type: FQPF5N60C

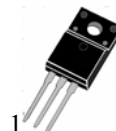
Maximum Ratings (Ta=25°C unless otherwise specified)

T_{stg}	Storage Temperature	-----	-55~150°C
T_j	Operating Junction Temperature	-----	150°C
V_{DSS}	Drain-Source Voltage	-----	600V
V_{GSS}	Gate-Source Voltage	-----	±30V
I_D	Drain Current (Continuous)($T_c=25^\circ C$)	-----	4.5A
I_{DM}	Pulsed Drain Current (Note 1)	-----	18A
P_D	Maximum Power Dissipation ($T_c=25^\circ C$)	-----	33W
	Derate Above 25°C	-----	0.26W/°C
E_{AS}	Pulsed Avalanche Energy (Note 2)	-----	210mJ
I_{AR}	Avalanche Current (Note 1)	-----	4.5A
E_{AR}	Repetitive Avalanche Energy (Note 1)	-----	10mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	-----	4.5V/ns

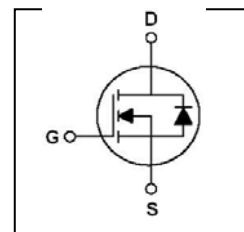
Thermal Characteristics

Symbol	Items	TO-220F	Unit
Rthj-case	Thermal Resistance Junction-case	Max 3.79	°C/W
Rthj-amb	Thermal Resistance Junction-ambient	Max 62.5	°C/W

TO-220F



1- G 2-D 3-S



**Electrical Characteristics** ($T_a=25^{\circ}\text{C}$ unless otherwise specified)

Symbol	Items	Min.	Typ.	Max.	Unit	Conditions
Off Characteristics						
BV _{DSS}	Drain-Source Breakdown Voltage	600			V	I _D =250μA , V _{GS} =0V
I _{DSS}	Zero Gate Voltage Drain Current			1	μA	V _{DS} =600V, V _{GS} =0V
				10	μA	V _{DS} =480V, V _{GS} =0V,T _j =125℃
I _{GSS}	Gate – Body Leakage			±100	nA	V _{GS} = ±30V , V _{DS} =0V
On Characteristics						
V _{GS(th)}	Gate Threshold Voltage	2.5		4.5	V	V _{DS} = V _{GS} , I _D =250μA
R _{DS(on)}	Static Drain-Source On-Resistance		2.0	2.5	Ω	V _{GS} =10V, I _D =2.25A
Dynamic Characteristics and Switching Characteristics						
C _{iss}	Input Capacitance		530	690	pF	V _{DS} = 25 V, V _{GS} = 0V, f = 1.0 MHz
C _{oss}	Output Capacitance		57	74	pF	
C _{rss}	Reverse Transfer Capacitance		7	9	pF	
t _{d(on)}	Turn - On Delay Time		11	33	nS	V _{DS} = 300V, I _D =4.5A, R _G = 25 Ω (Note 4,5)
tr	Rise Time		45	90	nS	
t _{d(off)}	Turn - Off Delay Time		40	88	nS	
t _f	Fall Time		48	100	nS	
Q _g	Total Gate Charge		15	19	nC	V _{DS} =480V, I _D =4.5A, V _{GS} = 10 V (Note 4,5)
Q _{gs}	Gate–Source Charge		4		nC	
Q _{gd}	Gate–Drain Charge		7		nC	
Drain-Source Diode Characteristics and Maximun Ratings						
I _S	Continuous Source–Drain Diode Forward Current			4.5	A	
I _{SM}	Pulsed Drain-Source Diode Forward Current			18	A	
V _{SD}	Source–Drain Diode Forward On–Voltage			1.4	V	I _S =4.5A,V _{GS} =0

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. $L=18.9\text{mH}$, $I_{AS}=4.5\text{A}$, $V_{DD}=50\text{V}$, $R_G=25\Omega$, Starting $T_j=25^{\circ}\text{C}$
3. $I_{SD}\leq 4.5\text{A}$, $di/dt\leq 200\text{A}/\mu\text{S}$, $V_{DD}\leq BV_{DSS}$, Starting $T_j=25^{\circ}\text{C}$
4. Pulse Test: Pulse width $\leq 300\mu\text{S}$, Duty Cycle $\leq 2\%$
5. Essentially independent of operating temperature



Typical Characteristics

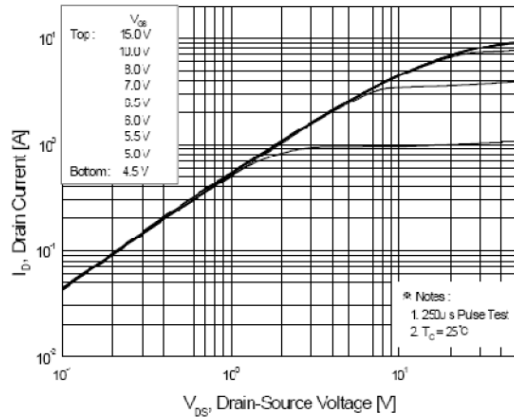


Figure 1. On Region Characteristics

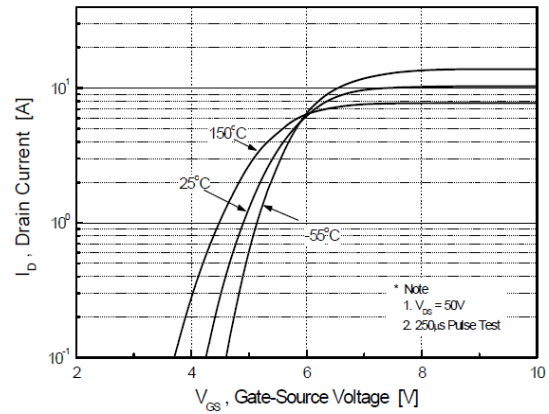


Figure 2. Transfer Characteristics

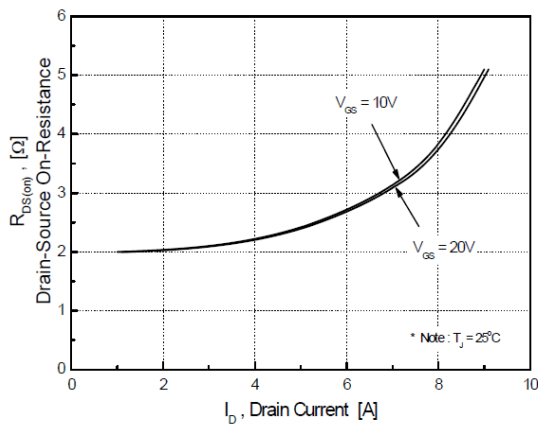


Figure 3. On Resistance Variation vs Drain Current and Gate Voltage

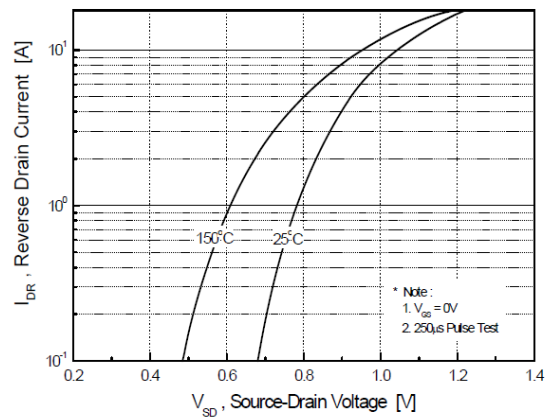


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

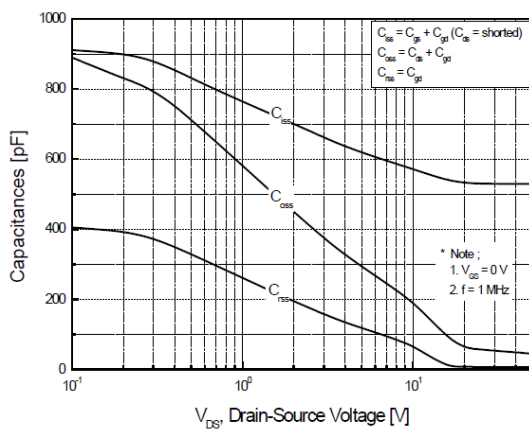


Figure 5. Capacitance Characteristics

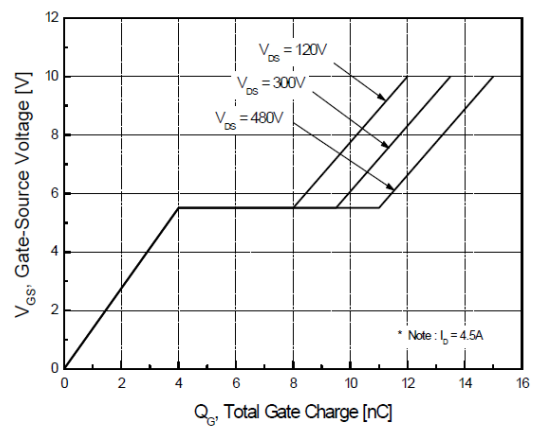


Figure 6. Gate Charge Characteristics



Typical Characteristics

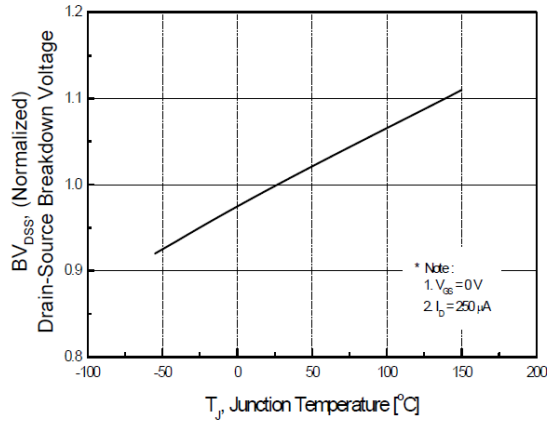


Figure 7. Breakdown Voltage Variation vs Temperature

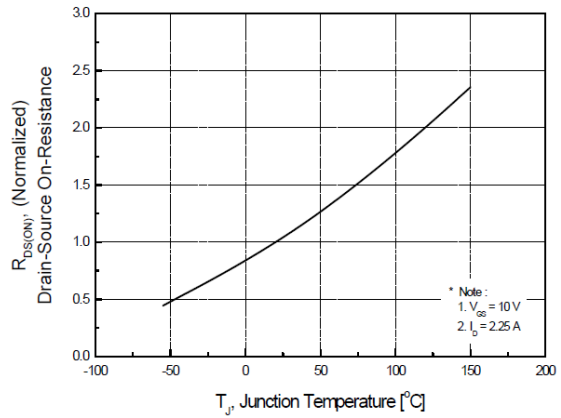


Figure 8. On-Resistance Variation vs Temperature

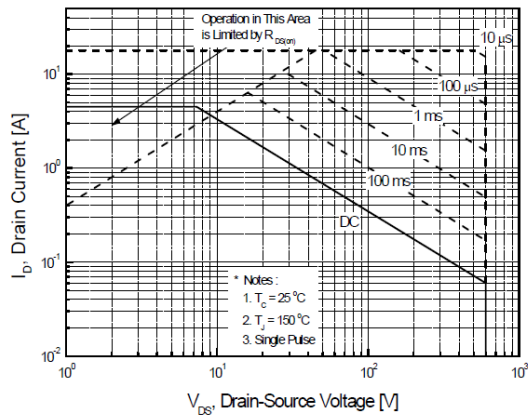


Figure 9. Maximum Safe Operating Area

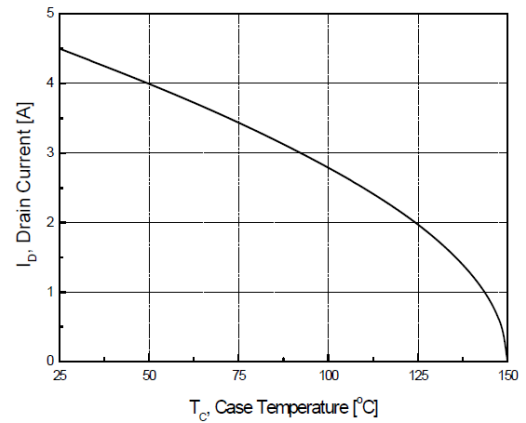


Figure 10. Maximum Drain Current vs Case Temperature

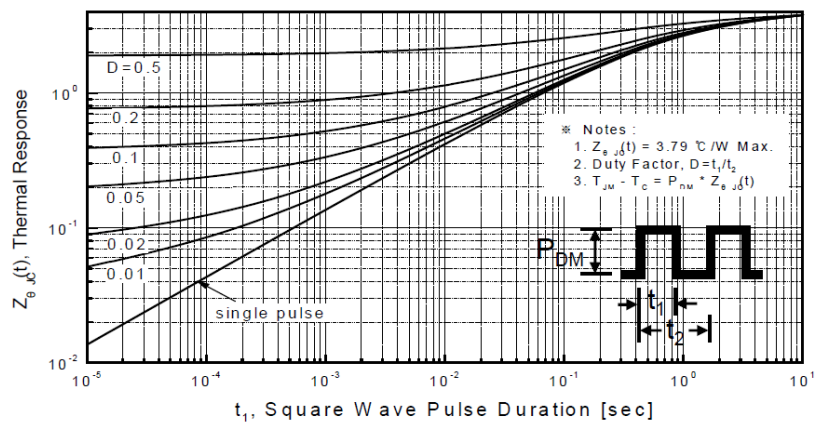


Figure 11. Transient Thermal Response Curve



Typical Characteristics

Fig 12. Gate Charge Test Circuit & Waveform

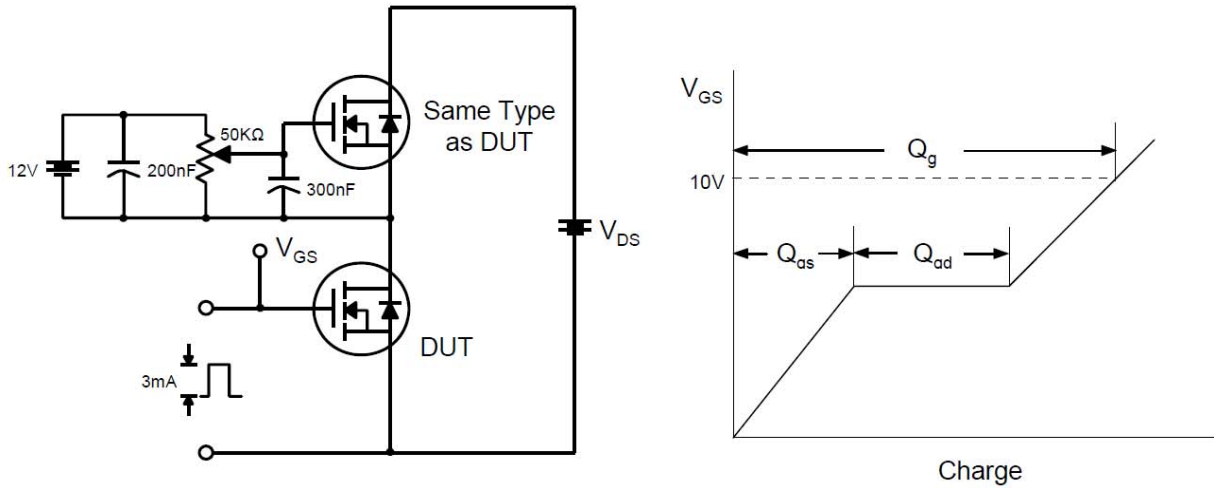


Fig 13. Resistive Switching Test Circuit & Waveforms

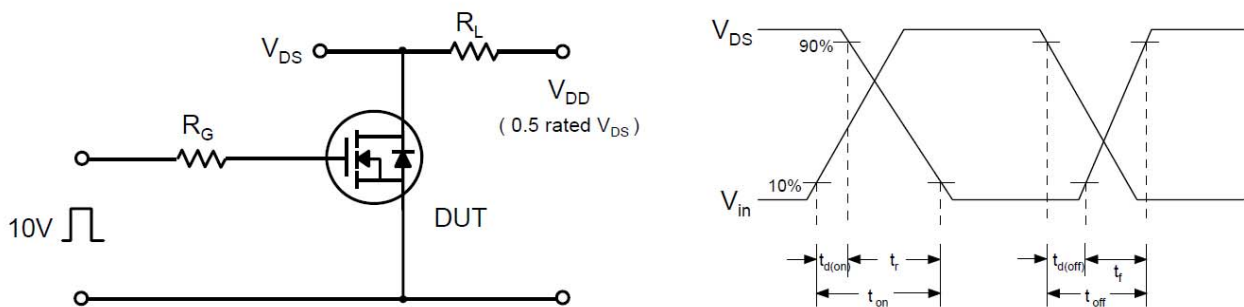


Fig 14. Unclamped Inductive Switching Test Circuit & Waveforms

