

MOTOROLA SEMICONDUCTOR TECHNICAL DATA

Designer's Data Sheet

Power Field Effect Transistor P-Channel Enhancement Mode Silicon Gate TMOS

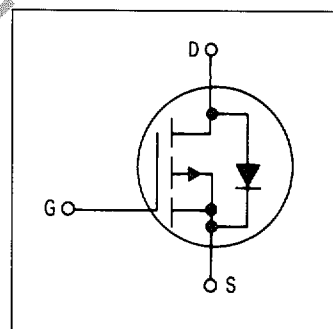
These TMOS Power FETs are designed for medium voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS} , $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads



MTH20P08
MTH20P10
MTM20P08
MTM20P10

TMOS POWER FETs
20 AMPERES
 $r_{DS(on)} = 0.15 \text{ OHM}$
80 and 100 VOLTS

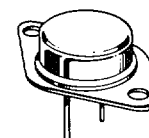


MAXIMUM RATINGS

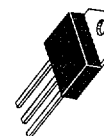
Rating	Symbol	MTM and MTH		Unit
		20P08	20P10	
Drain-Source Voltage	V_{DSS}	80	100	Vdc
Drain-Gate Voltage ($R_{GS} = 1 \text{ M}\Omega$)	V_{DGR}	80	100	Vdc
Gate-Source Voltage	V_{GS}	± 20		Vdc
Drain Current Continuous	I_D	20		Adc
Pulsed	I_{DM}	80		
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	125	1	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	-65 to 150		°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case	$R_{\theta JC}$	1	°C/W
Junction to Ambient	$R_{\theta JA}$	30	
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	°C



MTM20P08
MTM20P10
CASE 1-04
TO-244A
(TO-3)



MTH20P08
MTH20P10
CASE 340-01
TO-218AC

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.



MOTOROLA

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
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OFF CHARACTERISTICS

Drain-Source Breakdown Voltage ($V_{GS} = 0$, $I_D = 0.25\text{ mA}$) MTH20P08, MTM20P08 MTH20P10, MTM20P10	$V_{(BR)DSS}$	80 100	— —	Vdc
Zero Gate Voltage Drain Current ($V_{DS} = \text{Rated } V_{DSS}$, $V_{GS} = 0$) ($V_{DS} = 0.8 \text{ Rated } V_{DSS}$, $V_{GS} = 0$, $T_J = 125^\circ\text{C}$)	I_{DSS}	— —	0.2 1	mAdc
Gate-Body Leakage Current, Forward ($V_{GSF} = 20\text{ Vdc}$, $V_{DS} = 0$)	I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse ($V_{GSR} = 20\text{ Vdc}$, $V_{DS} = 0$)	I_{GSSR}	—	100	nAdc

ON CHARACTERISTICS*

Gate Threshold Voltage ($V_{DS} = V_{GS}$, $I_D = 1\text{ mA}$) $T_J = 100^\circ\text{C}$	$V_{GS(th)}$	2 1.5	4.5 4	Vdc
Static Drain-Source On-Resistance ($V_{GS} = 10\text{ Vdc}$, $I_D = 10\text{ Adc}$)	$r_{DS(on)}$	—	0.15	Ohm
Drain-Source On-Voltage ($V_{GS} = 10\text{ V}$) ($I_D = 20\text{ Adc}$) ($I_D = 10\text{ Adc}$, $T_J = 100^\circ\text{C}$)	$V_{DS(on)}$	— —	3.2 3	Vdc
Forward Transconductance ($V_{DS} = 1\text{ V}$, $I_D = 10\text{ A}$)	g_{fs}	5	—	mhos

DYNAMIC CHARACTERISTICS

Input Capacitance	($V_{DS} = 25\text{ V}$, $V_{GS} = 0$, $f = 1\text{ MHz}$)	C_{iss}	—	2000	pF
Output Capacitance		C_{oss}	—	950	
Reverse Transfer Capacitance		C_{rrs}	—	400	

SWITCHING CHARACTERISTICS* ($T_J = 100^\circ\text{C}$)

Turn-On Delay Time	($V_{DD} = 25\text{ V}$, $I_D = 0.5 \text{ Rated } I_D$ $R_{gen} = 50\text{ ohms}$) See Figures 12 and 13	$t_{d(on)}$	—	45	ns
Rise Time		t_r	—	200	
Turn-Off Delay Time		$t_{d(off)}$	—	150	
Fall Time		t_f	—	150	
Total Gate Charge	($V_{DS} = 0.8 \text{ Rated } V_{DSS}$, $I_D = \text{Rated } I_D$, $V_{GS} = 10\text{ V}$) See Figure 11	Q_g	52 (Typ)	75	nC
Gate-Source Charge		Q_{gs}	22 (Typ)	—	
Gate-Drain Charge		Q_{gd}	30 (Typ)	—	

SOURCE DRAIN DIODE CHARACTERISTICS*

Forward On-Voltage	($I_S = \text{Rated } I_D$ $V_{GS} = 0$) See Figures 15 and 16	V_{SD}	2.8 (Typ)	4	Vdc
Forward Turn-On Time		t_{on}	100 (Typ)	—	ns
Reverse Recovery Time		t_{rr}	350 (Typ)	—	ns

*Pulse Test: Pulse Width $\leq 300\text{ }\mu\text{s}$, Duty Cycle $\leq 2\%$.

TYPICAL ELECTRICAL CHARACTERISTICS

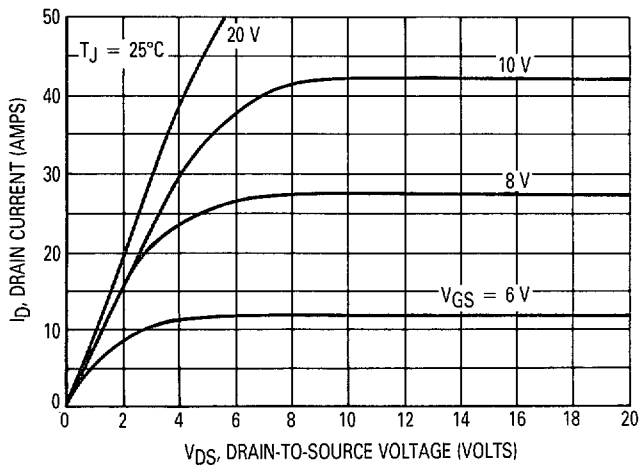


Figure 1. On-Region Characteristics

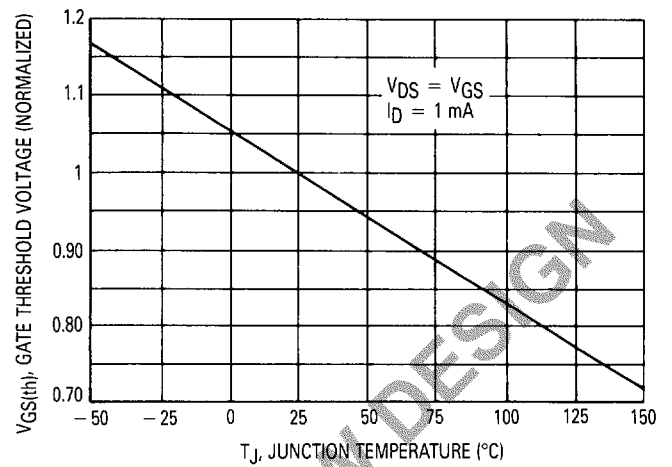


Figure 2. Gate-Threshold Voltage Variation With Temperature

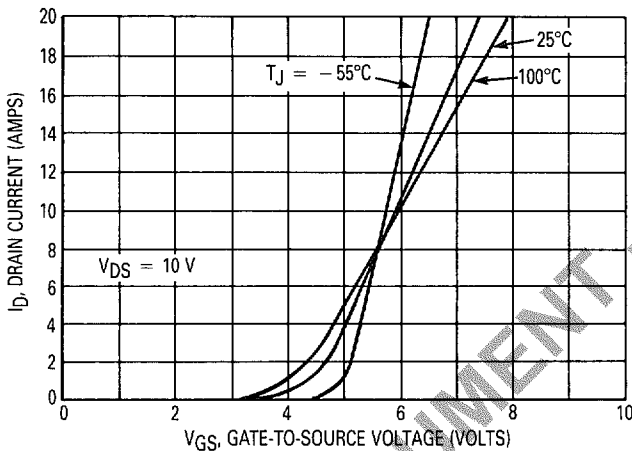


Figure 3. Transfer Characteristics

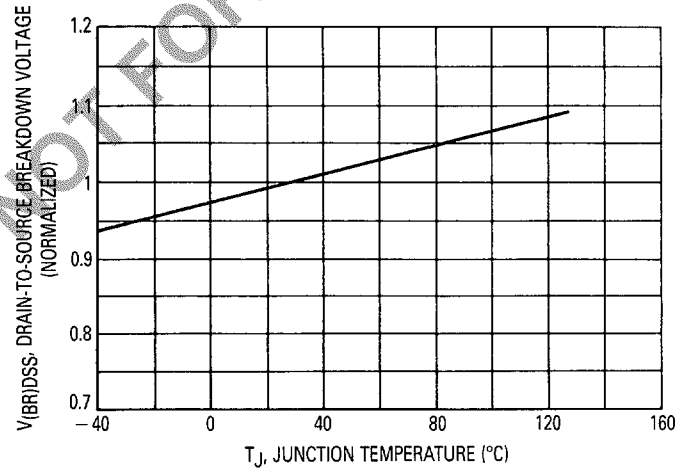


Figure 4. Breakdown Voltage Variation With Temperature

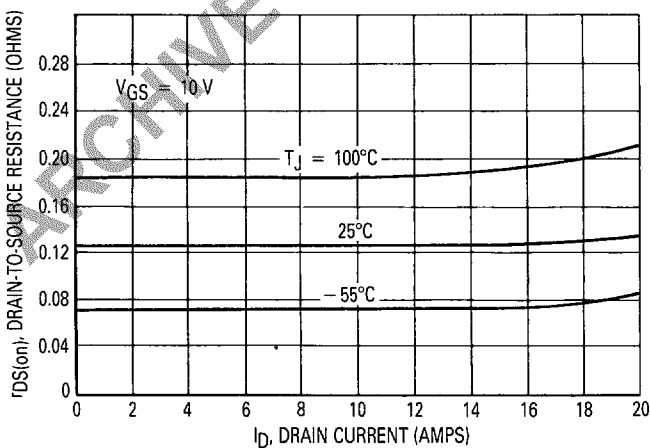


Figure 5. On-Resistance versus Drain Current

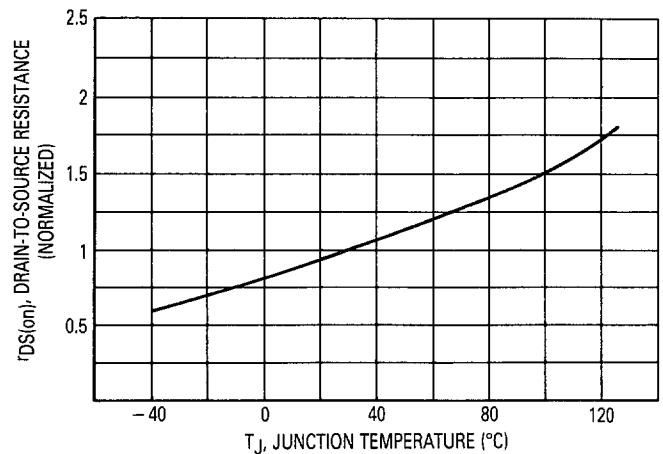


Figure 6. On-Resistance Variation With Temperature

SAFE OPERATING AREA INFORMATION

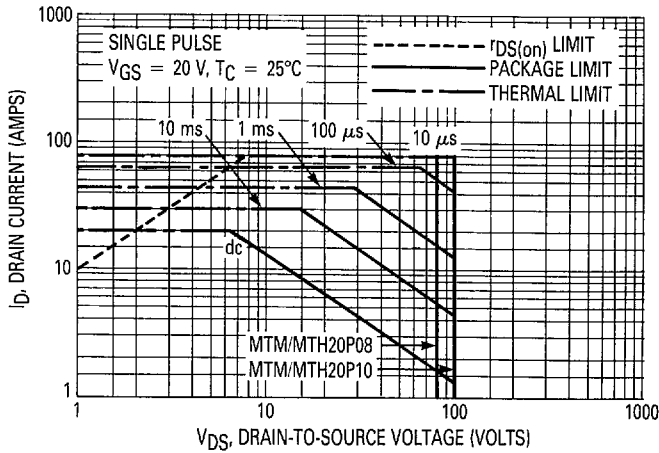


Figure 7. Maximum Rated Forward Biased Safe Operating Area

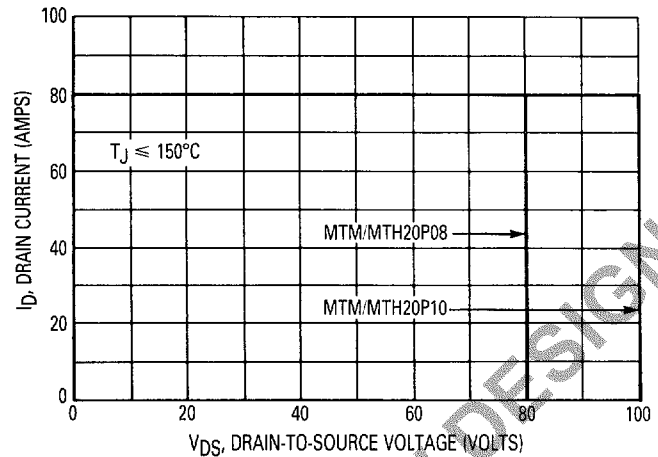


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

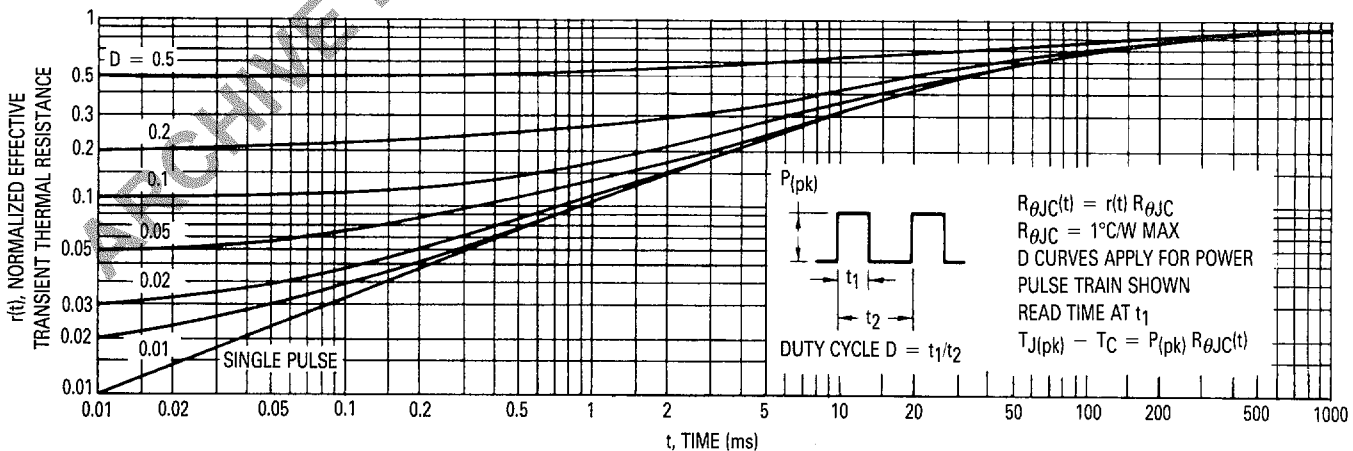


Figure 9. Thermal Response

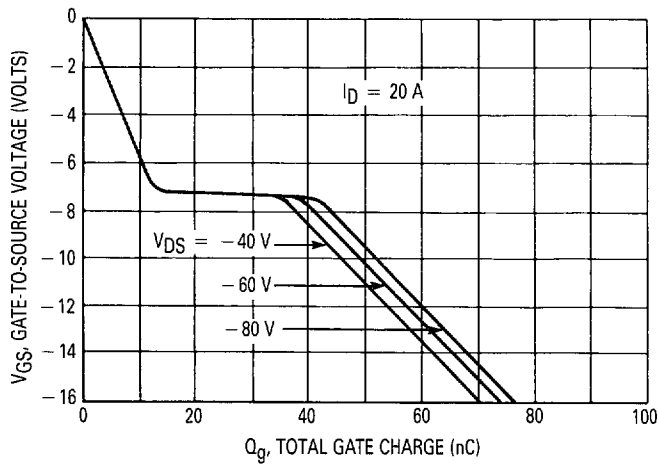


Figure 10. Capacitance Variation

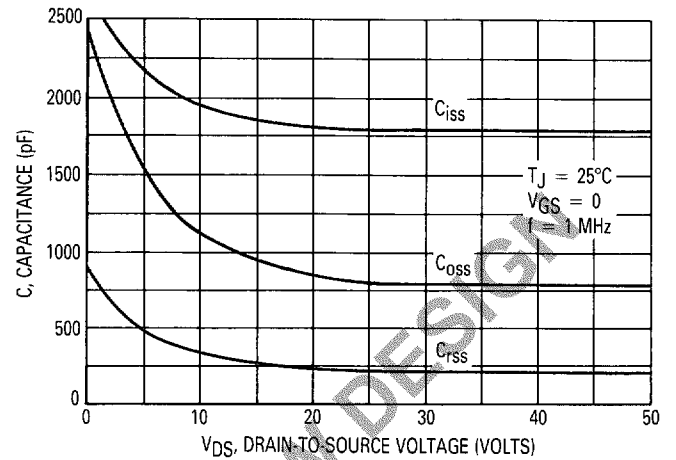


Figure 11. Gate Charge versus Gate-To-Source Voltage

RESISTIVE SWITCHING

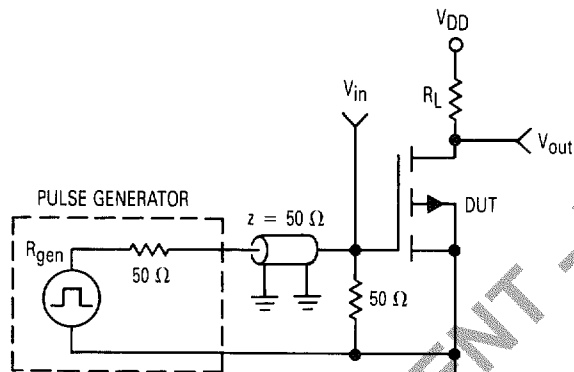


Figure 12. Switching Test Circuit

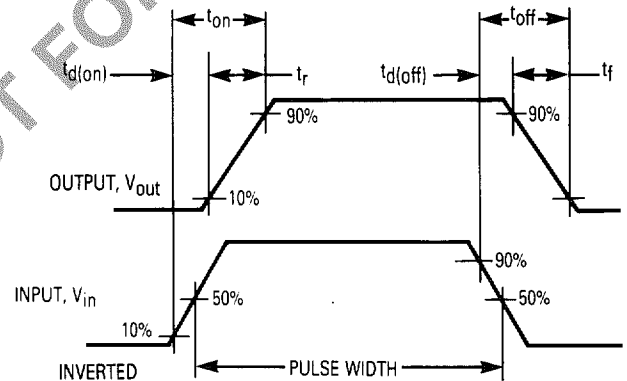
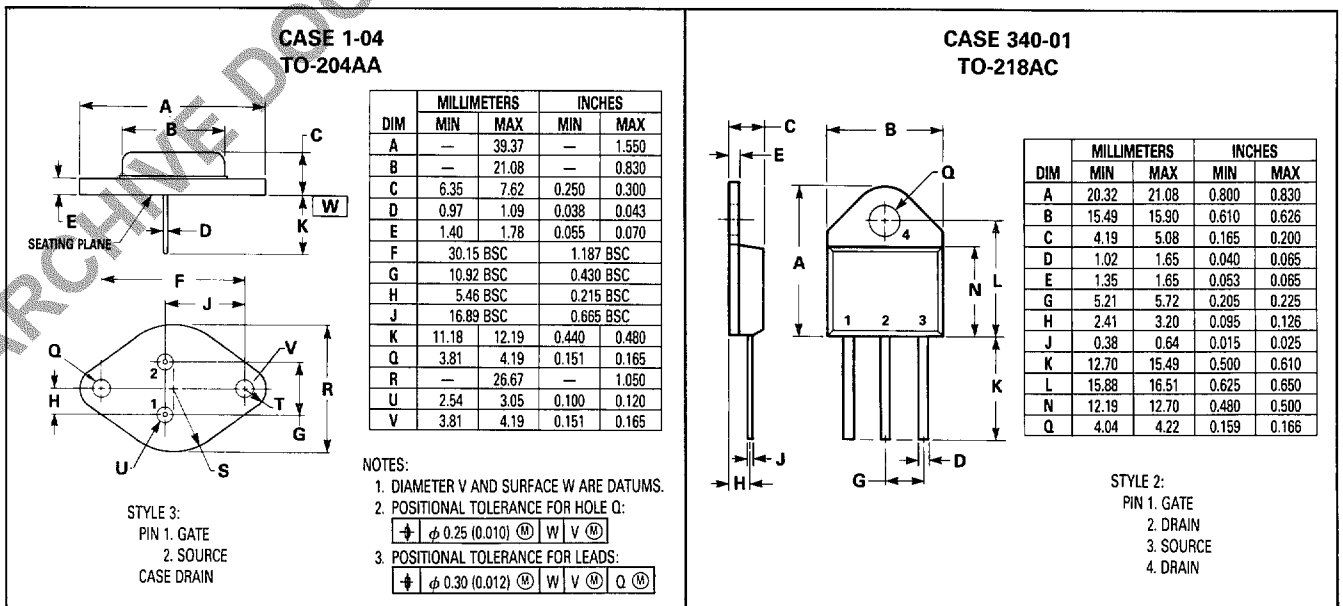


Figure 13. Switching Waveforms

OUTLINE DIMENSIONS



TMOS SOURCE-TO-DRAIN DIODE CHARACTERISTICS

In the fabrication of a TMOS FET, a diode is formed across the source-to-drain terminals as shown in Figure 14. Reversal of the drain voltage will cause current flow in the reverse direction. This diode may be used in circuits

requiring external fast recovery diodes, therefore, typical characteristics of the on voltage, forward turn-on and reverse recovery times are given.

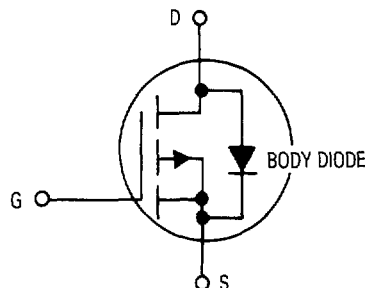


Figure 14. TMOS FET With Source-To-Drain Diode

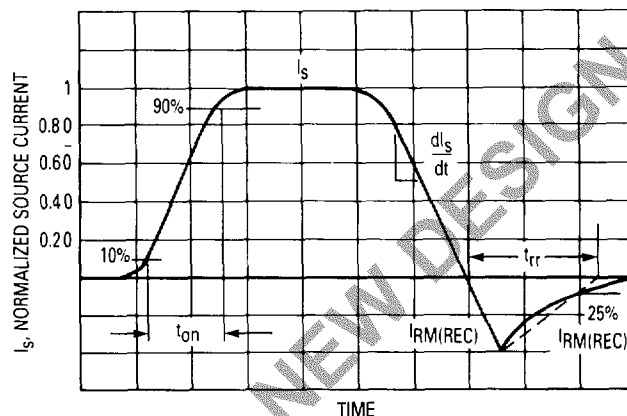


Figure 15. Diode Switching Waveform

NOTE: DUT is Shown as an N-Channel TMOS but can also be a P-Channel when appropriately connected. DUT Driver is the same device as DUT Diode (or Complement for P-Channel DUT Diode)

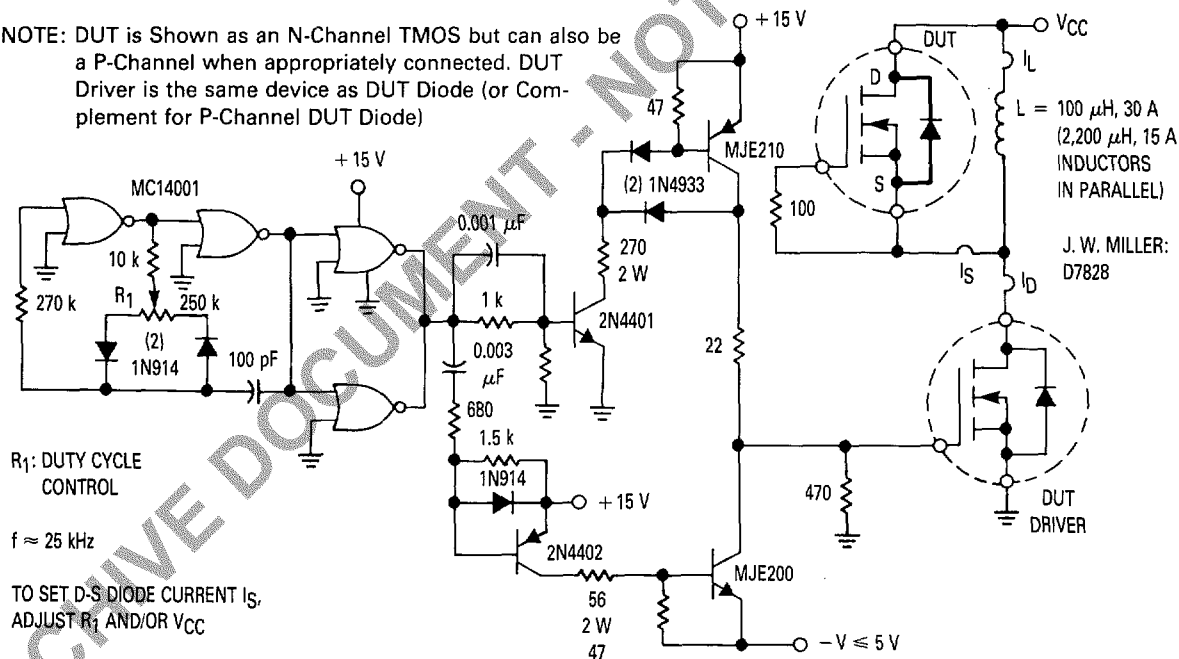


Figure 16. TMOS Diode Switching Test Circuit

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