

**MMC 362**

FREQUENCY DIVIDER

GENERAL DESCRIPTION

MMC 362 frequency divider is a metal gate CMOS integrated circuit. The time base of the circuit is provided by connecting a 4 MHz quartz and a RC network to the on-chip CMOS inverter/amplifier. The circuit provides multiplexing signals at a 1 KHz rate, with a 25% duty cycle, and clock signals of period, 0.1 s, 1 s, 1 s and 1 min. The circuit is supplied in a 16-lead dual-in-line package.

FEATURES

- wide supply range, 3 ... 18 V
- 4 MHz crystal-controlled operation
- available in 16-lead dual-in-line package

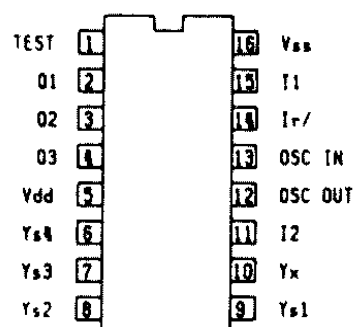
ABSOLUTE MAXIMUM RATINGS

V_{DD}	Supply voltage	-0.5 ... 18	V
V_I	Input voltage	-0.5 ... $V_{DD} + 0.5$	V
I_I	DC input current	+10	mA
P_D	Total power dissipation	200	mW
T_A	Operating temperature	-40 ... +85	°C
T_S	Storage temperature	-65 ... +150	°C

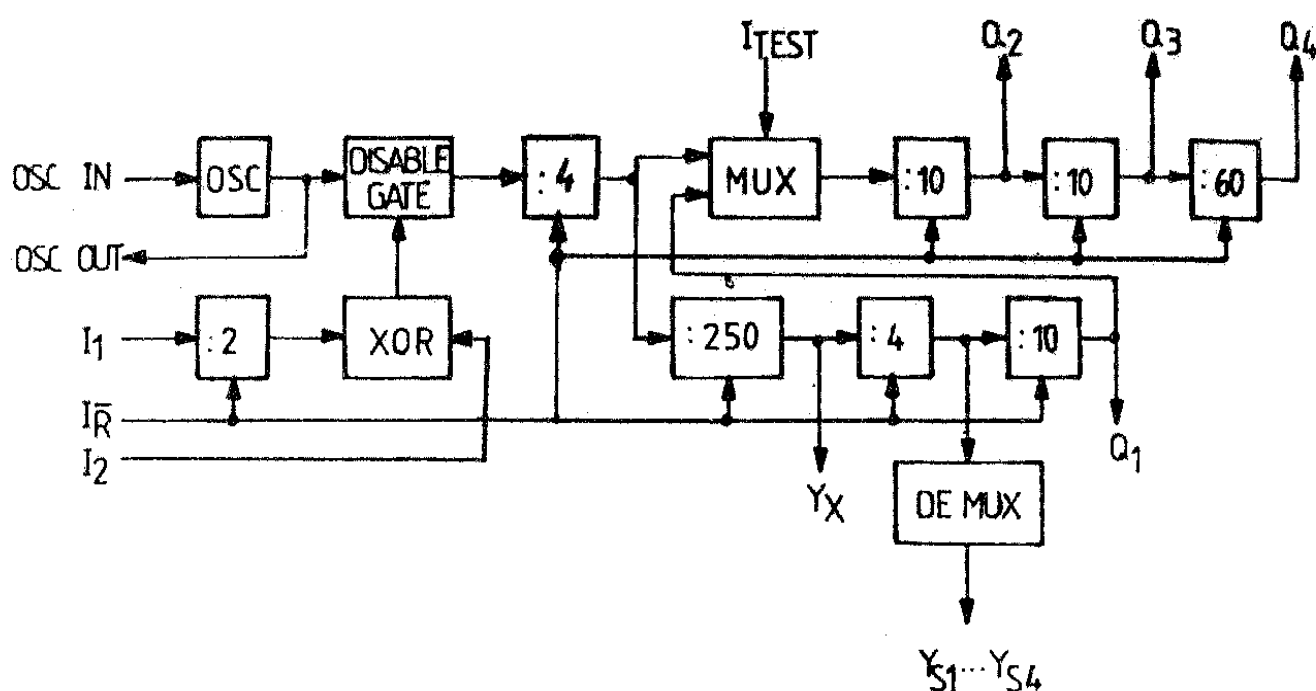
RECOMMENDED OPERATING CONDITIONS

V_{DD}	Supply voltage	3 ... 15	V
V_I	Input voltage	0 ... V_{DD}	
T_A	Operating temperature	-40 ... +85	°C

CONNECTION DIAGRAM



BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The precision time base of the circuit is provided by connecting a 4 MHz quartz crystal and a RC network together with the on-chip CMOS inverter/amplifier. The inputs I_1 , I_2 disable the access of the signal generated by the internal oscillator to the dividing chain, by a pulse applied on I_1 or by a step applied on I_2 . The state after reset make access possible if I_2 is connected to V_{SS} . A low level on the $I_{R\bar{}}$ input resets to 0 the flip-flops of the circuit; Schmitt Trigger action on this input permits unlimited block rise and fall times.

For testing purposes, I_{TEST} input connected to V_{SS} allows a 1 MHz signal to be applied to the second section of the dividing chain instead of the 100 Hz signal in normal operation.

The circuit provides 25% duty cycle, 1 KHz frequency multiplexing signals, $Y_{S1} \dots Y_{S4}$, and a 4 KHz signal, Y_X , for timing purposes.

It also provides signals of period equal to .01 s, .1 s, 1 s, 1 min, that can be used as clock input for a timer. The circuit being mounted in 16-lead dual-in-line package, the .01 s output is not connected.

STATIC ELECTRICAL CHARACTERISTICS

PARAMETER			TEST CONDITIONS				VALUES						UNIT
			V _I (V)	V _O (V)	I _O (μA)	V _{DD} (V)	T _{LOW}		25°C		T _{HIGH}		
							min.	max.	min.	max.	min.	max.	
I _L Quiescent current	G, H types	0/ 5			5		20		20		600	μA	
		0/10			10		40		40		1200		
		0/15			15		80		80		2400		
		0/20			20		400		400		12000		
	E, F types	0/ 5			5		80		80		600		
		0/10			10		160		160		1200		
		0/15			15		320		320		2400		
V _{OH} Output low voltage		0/ 5		< 1	5	4.95		4.95		4.95		V	
		0/10		< 1	10	9.95		9.95		9.95			
		0/15		< 1	15	14.95		14.95		14.95			
V _{OL} Output low voltage		5 / 0		< 1	5		0.05		0.05		0.05	V	
		10/ 0		< 1	10		0.05		0.05		0.05		
		15/ 0		< 1	15		0.05		0.05		0.05		

STATIC ELECTRICAL CHARACTERISTICS (cont'd)

PARAMETER			TEST CONDITIONS				VALUES						UNIT
			V _I (V)	V _O (V)	I _O (μA)	V _{DD} (V)	T _{LOW}		25°C		T _{HIGH}		
							min.	max.	min.	max.	min.	max.	
V _{IH}	Input high voltage			0.5/4.5 1/9 1.5/13.5	< 1 < 1 < 1	5 10 15	4 8 12.5		4 8 12.5		4 8 12.5	V	
V _{IL}	Input low voltage			4.5/0.5 9/1 13.5/1.5	< 1 < 1 < 1	5 10 15		1.5 3.0 4.0		1.5 3.0 4.0	1.5 3.0 4.0	V	
I _{IH} I _{IL}	Input leakage current	G, H types	0/18			18				.1		1.0	μA
		E, F types	0/15			15		.3		.3		1.0	
I _{OH}	Output drive current	G, H types	0/ 5	2.5		5	-2.0		-1.6		-1.1		mA
			0/ 5	4.6		5	-0.6		-0.5		-0.3		
			0/10	9.5		10	-1.6		-1.3		-0.9		
			0/15	13.5		15	-4.2		-3.4		-2.4		
		E, F types	0/ 5	2.5		5	-1.5		-1.3		-1.1		
			0/ 5	4.6		5	-0.5		-0.4		-0.3		
			0/10	9.5		10	-1.3		-1.1		-0.9		
			0/15	13.5		15	-3.6		-3.0		-2.4		
I _{OL}	Output sink current	G, H types	0/ 5	0.4		5	0.6		0.5		0.3		mA
			0/10	0.5		10	1.6		1.3		0.9		
			0/16	1.5		15	4.2		3.4		2.4		
		E, F types	0/ 5	0.4		5	0.5		0.4		0.3		
			0/10	0.5		10	1.3		1.1		0.9		
			0/15	1.5		15	3.6		3.0		2.4		
C _I	Input capacitance		Any input							7.5		pF	

DYNAMIC ELECTRICAL CHARACTERISTICS

PARAMETER		TEST CONDITIONS V _{DD} (V)	VALUES		UNIT
			min.	max.	
t _{PLH} t _{PHL}	Propagation delay I-O	15		5	μ s
t _{TLH} t _{THL}	Transition delay	15		150	ns
f _{CK}	Clock frequency	5 15		5 15	MHz

