National Semiconductor

Electronic Data Processing

# MM5330 4½-Digit Panel Meter Logic Block

General Description

The MM5330 is a monolithic integrated circuit which provides the logic circuitry to implement a 4-1/2 digit panel meter. The MM5330 utilizes P-channel low threshold enhancement mode devices and ion-implanted depletion mode devices. All inputs and outputs are TTL compatible with BCD output for direct interface with various display drivers.
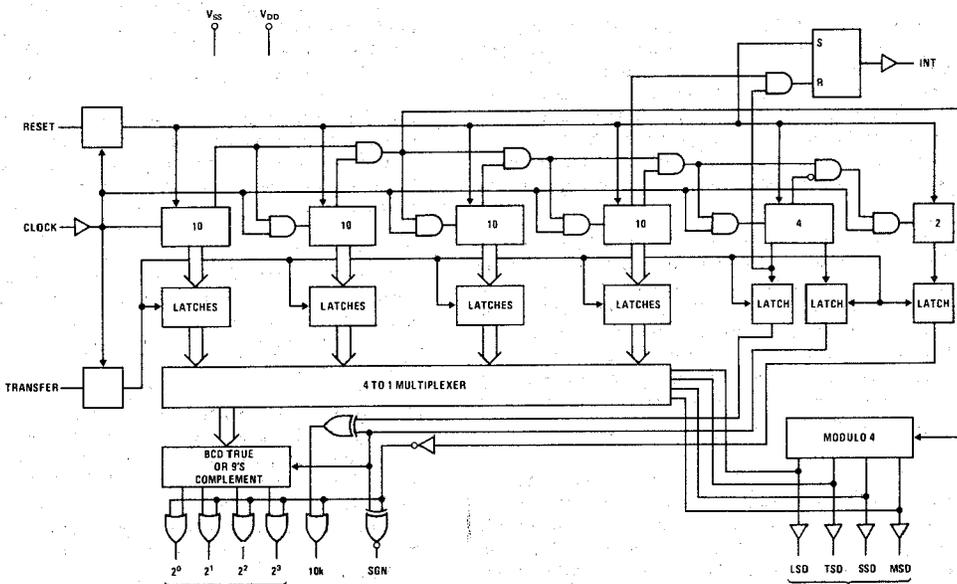
Features

- dc to 400 kHz operation
- TTL compatible inputs and outputs
- BCD output code
- Overrange blanking
- Valid sign bit during overrange
- Standard supply voltages; +5, −15V

Connection and Block Diagrams

Dual-In-Line Package
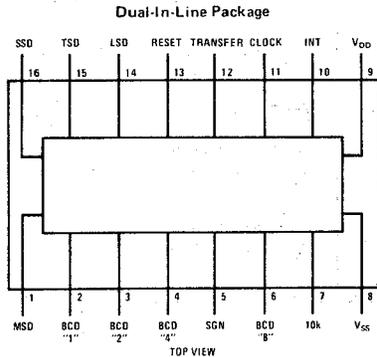
Order Number MM5330N
See Package 19

Absolute Maximum Ratings

Voltage at Any Pin $\quad\quad\quad\quad\quad\quad$ $V_{SS} + 0.3V$ to $V_{SS} - 25V$
Operating Temperature $\quad\quad\quad\quad\quad$ $0°C$ to $+75°C$
Storage Temperature $\quad\quad\quad\quad\quad\quad$ $-40°C$ to $+125°C$
Lead Temperature (Soldering, 10 seconds) $\quad$ $300°C$

Electrical Characteristics

T_A within operating range, $V_{SS} = 4.75V$ to $5.25V$, $V_{DD} = -16.5V$ to $-13.5V$ unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Voltage (V_{SS})		4.75	5	5.25	V
Power Supply Voltage (V_{DD})		-16.5	-15	-13.5	V
Power Supply Current (I_{SS})	No Load			30	mA
Input Frequency		dc		400	kHz
Reset or Transfer Pulse Width		200			ns
Input Voltage Levels	$V_{SS} = 5V$, $V_{DD} = -15V$				
Logic "1"	Inputs Driven by TTL or Square Waves	3		5	V
Logic "0"	Inputs Driven by TTL or Square Waves	-15		0.8	V
Clock Input Voltage Levels					
Logic "1"	Driven by Sinewave	$V_{SS}-0.5$		$V_{SS}+0.3$	V
Logic "0"	Driven by Sinewave	$V_{SS}-25$		$V_{SS}-4.5$	V
Output Current Levels	$V_{SS} = 5V$, $V_{DD} = -15V$				
Digit Output State					
Logic "1"	V_O Forced To 4.75V	100			μA
Logic "0"	V_O Forced To 4.5V	-5		-20	mA
All Other Outputs					
Logic "1"	V_O Forced To 3V	100			μA
Logic "0"	V_O Forced To 0.4V	-2			mA
Delay From Digit Output to BCD Output		0.1		5	μs

FUNCTIONAL DESCRIPTION

Counters: The MM5330 has four $\div 10$ counters, one $\div 4$ counter, and one $\div 2$ for a count of 80,000 clock pulses. A ripple carry is provided and all counter flip-flops are synchronous with the negative transition of the input clock. The last flip-flop in the divider chain ($\div 2$ in the block diagram) triggers with the "0" to "1" transition of the previous flip-flop. The count sequence is shown in the first column of the count diagram.

Reset: All counter stages are reset to "0" and the INT flip-flop (driving the INT output) is set to "1" on the first negative clock transition after a "0" is applied to the Reset input. The internal reset is removed on the first negative clock transition after the internal reset has occured and a "1" has been applied to the Reset input. This timing provides an on-chip reset at least one clock cycle wide and a one cycle delay to remove reset before counting begins.

Transfer: Data in the counters is transferred to the latches when the Transfer input is at "0." If the Transfer input is held low the state of the counters is continuously displayed (see count diagram). Data will cease to transfer to the latches on the first positive clock

transition after the first negative clock transition after a "1" is applied to the Transfer input. This provides a transfer pulse at least one half clock cycle wide and a half clock cycle delay to remove the transfer signal before the counters change state.

INT: The integrate output is used to set the charge time on a dual slope integrator. INT is "1" from reset to the 18,000th clock pulse, then "0" until the next reset. The dual slope integrator is the voltage monitoring part of the external circuitry needed for a DPM. It charges a capacitor at a rate proportional to the measured voltage while INT is "1," then discharges at a rate proportional to a fixed reference as shown in the dual slope diagram. When the output of the integrator reaches 0V a pulse is generated and fed into the Transfer input of the chip. As the dual slope diagram indicates, the number in the latches is proportional to the measured voltage.

Multiplexing: The modulo 4 multiplex counter is triggered by the carry from the second decade counter, making the multiplex rate one hundredth the counting rate (4 kHz for a 400 kHz clock). The LSD, TSD, SSD and MSD (least significant, third significant, second significant and most significant digits) outputs indicate by a low level which decade latch is displayed at the BCD outputs.

FUNCTIONAL DESCRIPTION (Continued)

Overrange Blanking and Sign: The data in the latch for the $\div 2$ counter is used to detect an out-of-range voltage. If this latch is "0" the BCD and 10k outputs are forced to all "1's" and the SGN output is inverted. When the data in the overrange latch and the sign bit latch are "1" the sign bit generates the 9's complement of the decade latches and the complement of the 10k latch at the respective outputs. When the overrange bit is "1" and the sign bit is "0" true BCD of the decade latches and the uncomplemented 10k latch appear at the outputs.

APPLICATIONS INFORMATION

The MM5330 is the display and control for a modified dual slope system. It contains the counters and latches, together with a multiplexing system to provide 4 digits of display with one decoder driver. It also provides a sign digit, either plus or minus, and a ten-thousand counts digit for full display of ±19999. By eliminating the right-most digits it may also be used as a 2-1/2 or 3-1/2 digit DVM chip.

The basic modified dual slope system for which the MM5330 is designed, is shown in *Figure 1.* The integrator is now used in a non-inverting mode and is biased to integrate negatively for all voltages below V_{MAX}. Thus if the maximum positive voltage at V_{IN} is 1.9999V, then V_{MAX} would be set at 2.200V. In this way, all voltages measured are below V_{MAX}. This eliminates the need for reference switching and provides automatic polarity with no additional components. Also, it can be shown that the amplifier input bias currents which cause errors in conventional dual slope systems are eliminated by merely zeroing the display. Thus low bias current op amps are not necessarily required unless a high input impedance is desired at V_{IN}.

Count Diagram

	INTERNAL STATES								OUTPUTS WITH TRANSFER LOW						
	OVERRANGE BIT COMPLEMENT	SIGN BIT	10k BIT	DECADE COUNTERS					INT (AFTER RESET)	SGN	10k	BCD DECADE OUTPUTS			
	0	0	0	0	0	0	0		1	1	1				
	0	0	0	0	0	0	1		1	1	1				
	0	0	0	0	0	0	2		1	1	1	•			
				•								•			
	0	0	0	9	9	9	9		1	1	1	•			
BLANKING ZONE	0	0	1	0	0	0	0		1	1	1		OUTPUT BLANKED		
				•								•			
	0	0	1	7	9	9	9		1	1	1	•			
	0	0	1	8	0	0	0	POSITIVE OVERRANGE	0	1	1	•			
				•								•			
	0	0	1	9	9	9	9		0	1	1	•			
	1	1	0	0	0	0	0		0	1	1	9	9	9	9
				•								•			
COMPLEMENT OUTPUT INTERVAL	1	1	0	9	9	9	9	POSITIVE VALUE	0	1	1	0	0	0	0
	1	1	1	0	0	0	0		0	1	0	9	9	9	9
				•								•			
	1	1	1	9	9	9	9	DISPLAY ZONE	0	1	0	0	0	0	0
	1	0	0	0	0	0	0		0	0	0	0	0	0	0
				•								•			
TRUE OUTPUT INTERVAL	1	0	0	9	9	9	9	NEGATIVE VALUE	0	0	0	9	9	9	9
	1	0	1	0	0	0	0		0	0	1	0	0	0	0
				•								•			
	1	0	1	9	9	9	9		0	0	1	9	9	9	9
BLANKING ZONE	0	1	0	0	0	0	0	NEGATIVE OVERRANGE	0	0	1	•			

CONTINUOUS COUNT

5

APPLICATIONS INFORMATION (Continued)

Secondly, the use of a conventional op amp for a comparator allows zeroing of all voltage offsets in both the op amp and comparator. This is achieved by zeroing the voltage on the capacitor through the use of the comparator as part of a negative feedback loop. During the zeroing period, the non-inverting input of the integrator is at V_{REF}. As this voltage is within the active common-mode range of the integrator the loop will respond by placing the integrator and comparator in the active region. The voltage on the capacitor is no longer equal to zero, but rather to a voltage which is the sum of both the op amp and comparator offset voltages. Because of the intrinsic nature of an integrator, this constant voltage remains throughout the integrating cycle and serves to eliminate even large offset voltages.

The waveforms at the output of the integrator are as shown. The voltage at A is the comparator threshold just discussed. Simultaneously, with the opening of switch A, V_{IN} is connected to the input of the integrator via switch B. The output then slews to V_{IN}. Integration then begins for the reference period, after which time the reference voltage is again applied to the input. The output again slews the difference between V_{REF} and V_{IN} and integrates for the unknown period until the comparator threshold is crossed. At this point, the accumulated counts are transferred from the counters to the latches and zeroing begins until the next conversion interval.

It may be obvious, however, that while we have eliminated several of the basic dual slope circuits disadvantages, we have created another—the number of counts are no longer proportional to V_{IN} but rather to $(V_{MAX}-V_{IN})$. In fact, when we short V_{IN} to ground we are actually measuring our own 2.2000 V_{MAX}.

What is done in the MM5330 is to code convert the number of counts as shown in the count diagram. This chart shows a code conversion starting at the time of a reset. The first 18,000 counts are the reference period after which time the integrator changes slope. If a com-

parator crossing is detected within the next 2000 counts, a plus overrange condition will occur at the display. This condition results in a lit "+" sign, a lit "1" and four blanked rightmost digits. A transfer at 20,000 however, will create a reading of +1.9999, at 20,001 a reading of 19.998 and so on, until at 39,999 a reading of +0000 would be displayed. A transfer occuring at 40,000 would cause a −0000 display and so on until 60,000 counts were entered at which time a −1 with four blanked digits would be displayed indicating a minus overrange condition.

A typical circuit for a low cost 4 1/2 digit DPM is shown in *Figure 2*. The display interface used is a TTL, 7-segment decoder driver and four P-type transistors. The ±1 digit is driven directly by CMOS. The clock-synchronous reset and transfer functions prevent any cyclic digit variations and present a blink-free, flicker-free display. CMOS analog switches are used as reference, zero, and input switches and used also in the comparator slew rate circuit.

A problem with all dual slope systems occurs when short integrating times and high clock frequencies are used. Because of the very slow rise time of the ramp into the comparator, the output of the comparator will normally ramp at approximately 1/10 of its actual slew rate. Thus, a significant number of extra counts are displayed due to the slow rate of rise of the comparator. A technique to improve this consists of capacitor C_S and analog switch four. An unstable positive loop is created by this capacitor when the comparator comes out of saturation. This causes the output to rise at its slew rate to the comparator threshold. As soon as this threshold is reached the analog switch opens and zeroing is initiated as previously discussed.

A simplified approach to performing the modified dual slope function combines the MM5330 and the LF11300 dual slope analog block as in *Figure 3*. The LF11300 provides the front analog circuitry required. This includes a FET input amplifier, analog switches, integrator and comparator. The LF11300 provides auto zero, > 1000 MΩ input impedance, and a ±10V analog range.
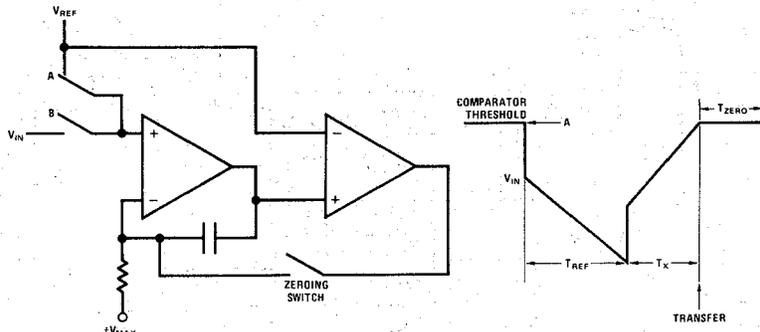
Dual Slope Diagram

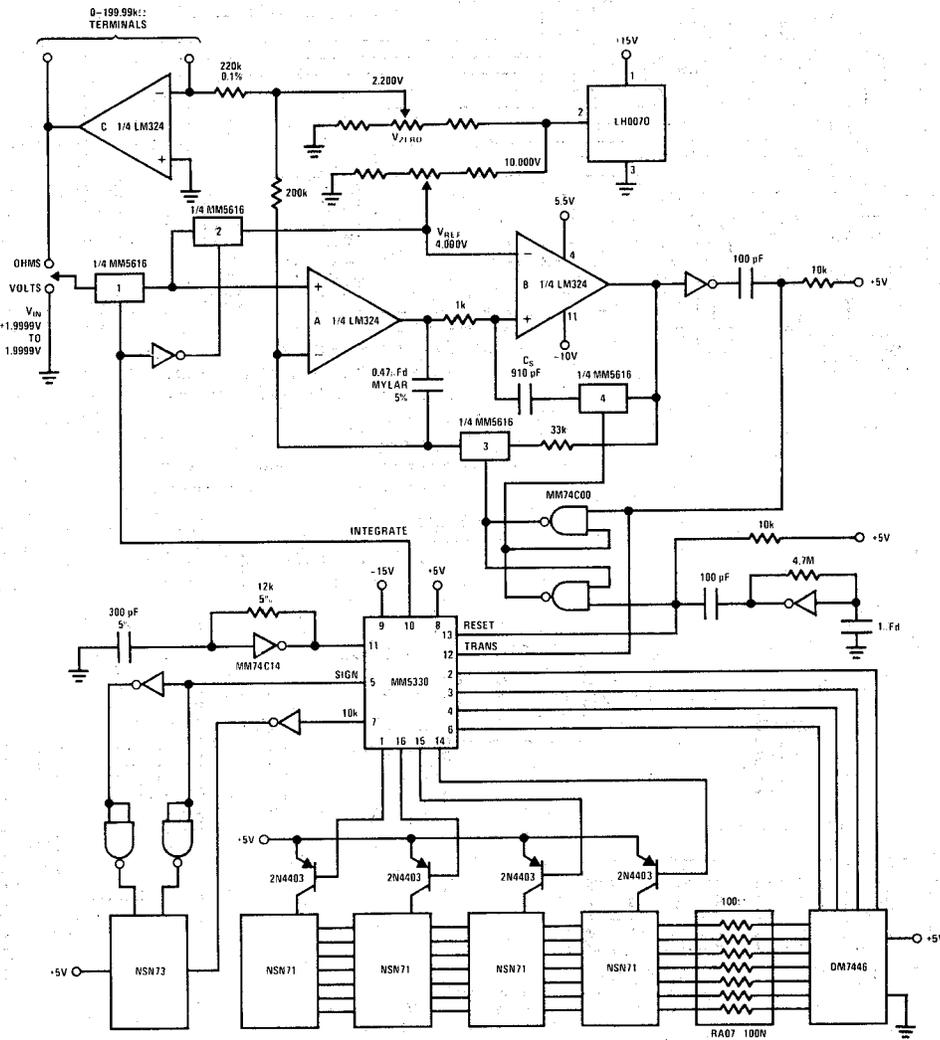
V_x is the analog voltage to be converted.
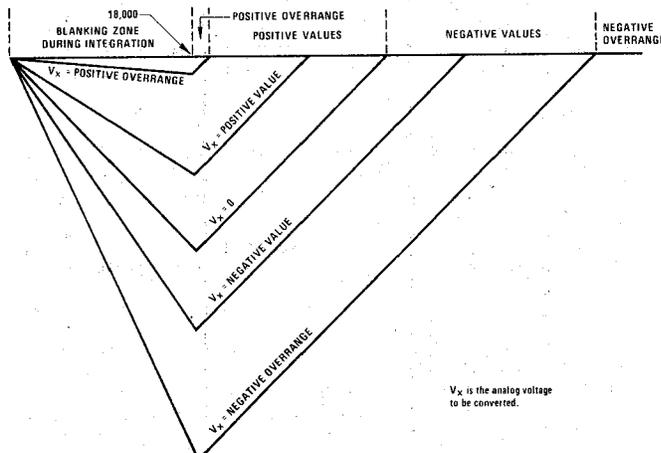
Typical Applications
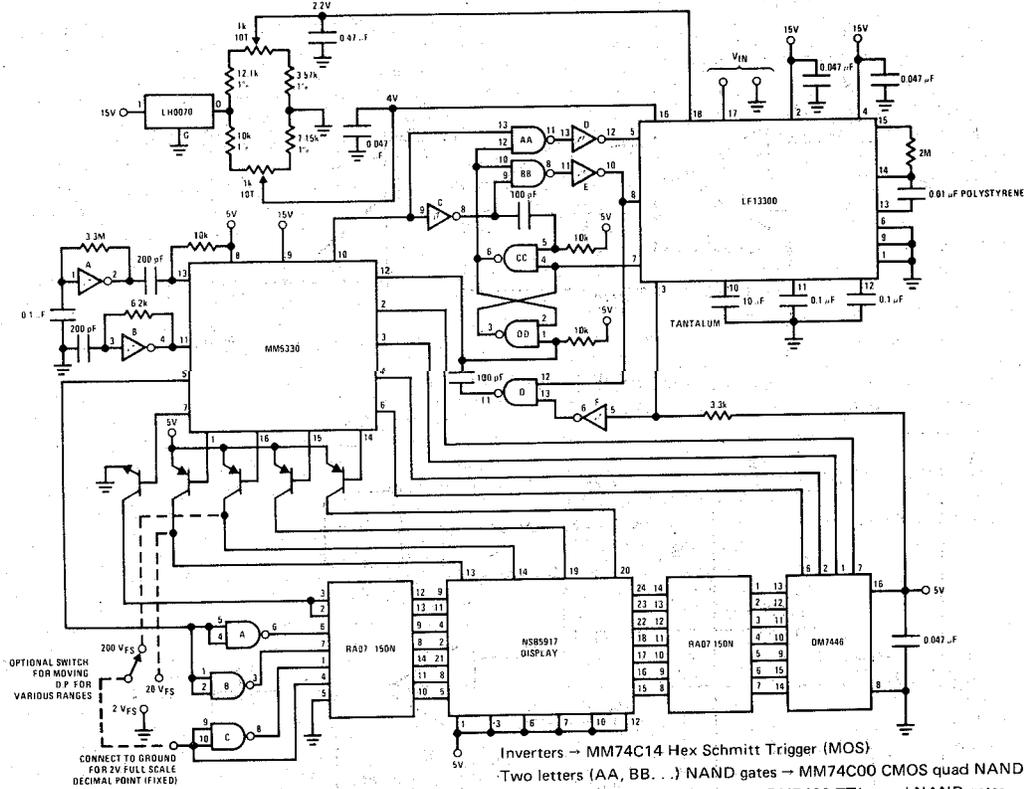

FIGURE 1. Modified Dual Slope

FIGURE 2. Typical Application Low Cost 4 1/2 Digit Volt-Ohm Meter

Typical Applications (Cont'd)

Inverters → MM74C14 Hex Schmitt Trigger (MOS)
Two letters (AA, BB. . .) NAND gates → MM74C00 CMOS quad NAND gates
One letter (A, B. . .) NAND gates → DM7400 TTL quad NAND gates
↓→ analog ground
→ digital ground
All resistors 1/4W, 5% unless otherwise noted.
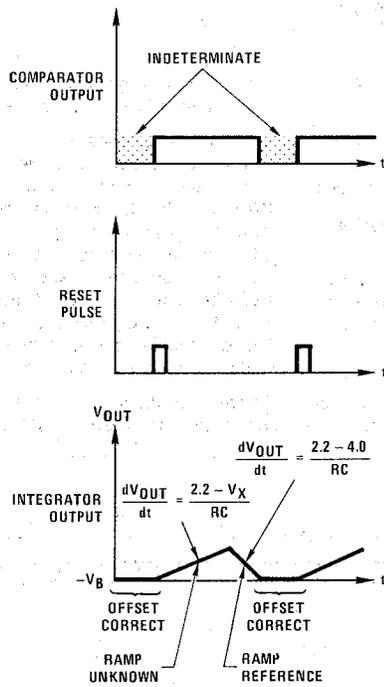All capacitor values in μF unless otherwise noted.

(Second letter code)

NSB5917 Display (Front View)
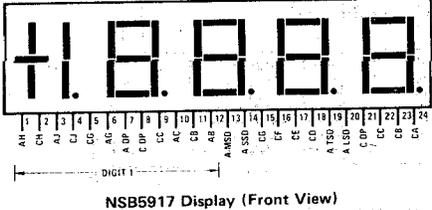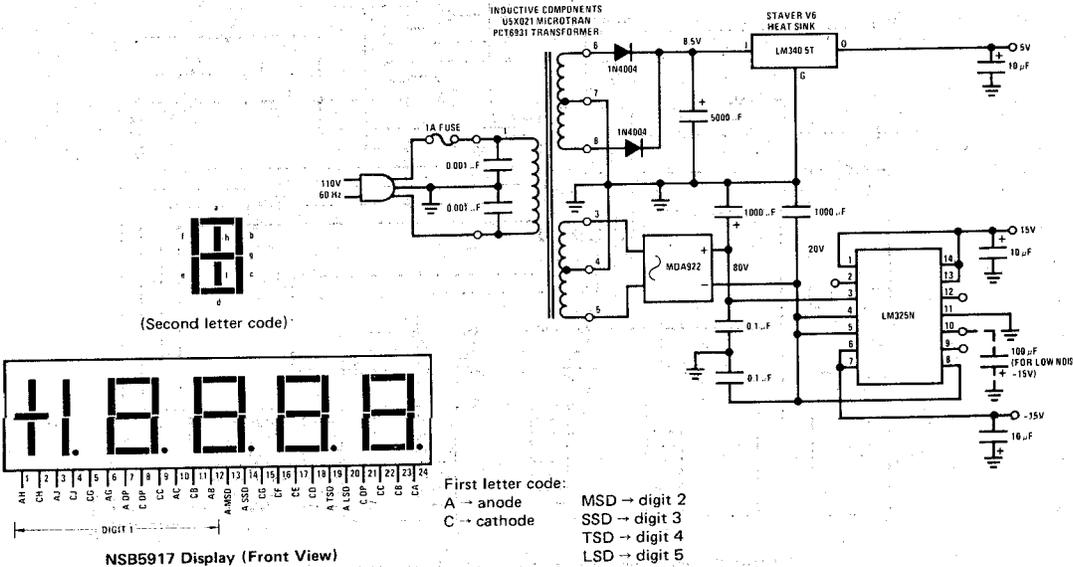
First letter code:
A → anode   MSD → digit 2
C → cathode   SSD → digit 3
                 TSD → digit 4
                 LSD → digit 5

FIGURE 3. 4 1/2-Digit DVM

Timing Diagrams

4 1/2-Digit DPM

COMPARATOR
OUTPUT

INDETERMINATE

t

RESET
PULSE

t

V_{OUT}

INTEGRATOR
OUTPUT

$$\frac{dV_{OUT}}{dt} = \frac{2.2 - V_X}{RC}$$

$$\frac{dV_{OUT}}{dt} = \frac{2.2 - 4.0}{RC}$$

$-V_B$

t

OFFSET
CORRECT

OFFSET
CORRECT

RAMP
UNKNOWN

RAMP
REFERENCE

Note. Here the LF13300 always operates
as an autozeroed, high input impedance
inverting integrator; bipolar input volt-
ages are handled by offsetting the analog
ground by 2.2V.

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