

32K x 8 Bit Static Random Access Memory

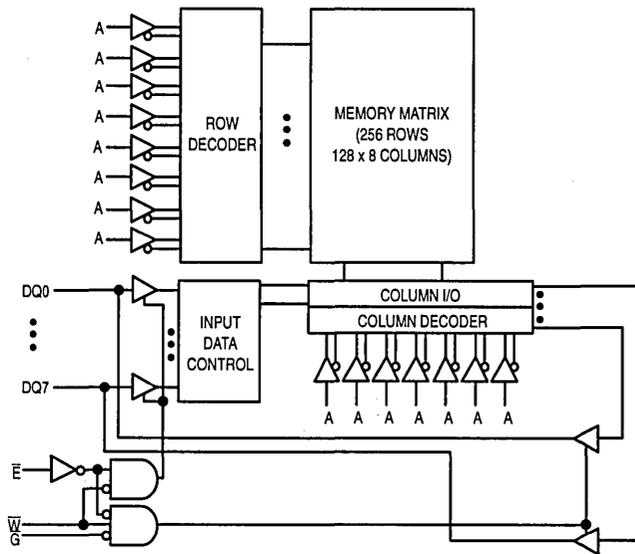
The MCM6706A is a 262,144 bit static random access memory organized as 32,768 words of 8 bits, fabricated using high performance silicon-gate BiCMOS technology. Static design eliminates the need for external clocks or timing strobes.

Output enable (\bar{G}) is a special control feature that provides increased system flexibility and eliminates bus contention problems.

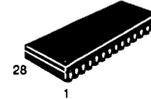
The MCM6706A is available in a 300 mil, 28-lead surface-mount SOJ package.

- Single 5.0 V \pm 10% Power Supply
- Fully Static — No Clock or Timing Strokes Necessary
- All Inputs and Outputs Are TTL Compatible
- Three State Outputs
- Fast Access Times: MCM6706A-8 = 8 ns
MCM6706A-10 = 10 ns
MCM6706A-12 = 12 ns

BLOCK DIAGRAM



MCM6706A



J PACKAGE
300 MIL SOJ
CASE 810B

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PIN ASSIGNMENT

A14	1	28	VCC
A12	2	27	\bar{W}
A7	3	26	A13
A6	4	25	A8
A5	5	24	A9
A4	6	23	A11
A3	7	22	\bar{G}
A2	8	21	A10
A1	9	20	E
A0	10	19	DQ7
DQ0	11	18	DQ6
DQ1	12	17	DQ5
DQ2	13	16	DQ4
VSS	14	15	DQ3

PIN NAMES

A0 - A14	Address Input
\bar{W}	Write Enable
E	Chip Enable
\bar{G}	Output Enable
DQ0 - DQ7	Data Input/Output
VCC	+ 5.0 V Power Supply
VSS	Ground

TRUTH TABLE (X = Don't Care)

\bar{E}	\bar{G}	\bar{W}	Mode	I/O Pin	Cycle
H	X	X	Not Selected	High-Z	—
L	H	H	Read	High-Z	—
L	L	H	Read	D _{out}	Read Cycle
L	X	L	Write	D _{in}	Write Cycle

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V _{CC}	- 0.5 to + 7.0	V
Voltage Relative to V _{SS} for Any Pin Except V _{CC}	V _{in} , V _{out}	- 0.5 to V _{CC} + 0.5	V
Output Current	I _{out}	± 30	mA
Power Dissipation	P _D	2.0	W
Temperature Under Bias	T _{bias}	- 10 to + 85	°C
Operating Temperature	T _A	0 to + 70	°C
Storage Temperature — Plastic	T _{stg}	- 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V _{CC}	4.5	5.0	5.5	V
Input High Voltage	V _{IH}	2.2	—	V _{CC} + 0.3*	V
Input Low Voltage	V _{IL}	- 0.5**	—	0.8	V

*V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 2.0 ns) or I ≤ 30.0 mA.

**V_{IL} (min) = - 0.5 V dc @ 30.0 mA; V_{IL} (min) = - 2.0 V ac (pulse width ≤ 2.0 ns) or I ≤ 30.0 mA.

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V _{in} = 0 to V _{CC})	I _{kg(I)}	—	± 1.0	μA
Output Leakage Current (\bar{E} = V _{IH} or \bar{G} = V _{IH} , V _{out} = 0 to V _{CC})	I _{kg(O)}	—	± 1.0	μA
Output High Voltage (I _{OH} = - 4.0 mA)	V _{OH}	2.4	—	V
Output Low Voltage (I _{OL} = + 8.0 mA)	V _{OL}	—	0.4	V

POWER SUPPLY CURRENTS

Parameter	Symbol	6706A-8	6706A-10	6706A-12	Unit
AC Active Supply Current (I _{out} = 0 mA, V _{CC} = max, f = f _{max})	I _{CCA}	195	185	175	mA
AC Standby Current (\bar{E} = V _{IH} , V _{CC} = max, f = f _{max})	I _{SB1}	130	120	115	mA
CMOS Standby Current (V _{CC} = max, f = 0 MHz, $\bar{E} \geq V_{CC} - 0.2$ V, V _{in} ≤ V _{SS} , or ≥ V _{CC} - 0.2 V)	I _{SB2}	50	50	50	mA

CAPACITANCE ($f = 1.0 \text{ MHz}$, $dV = 3.0 \text{ V}$, $T_A = 25^\circ\text{C}$, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Max	Unit
Address Input Capacitance	C_{in}	5	pF
Control Pin Input Capacitance (\bar{E} , \bar{G} , \bar{W})	C_{in}	6	pF
I/O Capacitance	C_{out}	6	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

($V_{CC} = 5.0 \text{ V} \pm 10\%$, $T_A = 0 \text{ to } +70^\circ\text{C}$, Unless Otherwise Noted)

Input Timing Measurement Reference Level 1.5 V Output Timing Measurement Reference Level 1.5 V
 Input Pulse Levels 0 to 3.0 V Output Load See Figure 1A
 Input Rise/Fall Time 2 ns

READ CYCLE (See Notes 1 and 2)

Parameter	Symbol		MCM6706A-8		MCM6706A-10		MCM6706A-12		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	8	—	10	—	12	—	ns	3
Address Access Time	t_{AVQV}	t_{AA}	—	8	—	10	—	12	ns	
Chip Enable Access Time	t_{ELQV}	t_{ACS}	—	8	—	10	—	12	ns	
Output Enable Access Time	t_{GLQV}	t_{OE}	—	4	—	5	—	6	ns	
Output Hold from Address Change	t_{AXQX}	t_{OH}	3	—	3	—	3	—	ns	
Chip Enable Low to Output Active	t_{ELQX}	t_{LZ}	1	—	1	—	1	—	ns	4, 5, 6
Chip Enable High to Output High-Z	t_{EHQZ}	t_{HZ}	0	4.5	0	5	0	6	ns	4, 5, 6
Output Enable Low to Output Active	t_{GLQX}	t_{LZ}	0	—	0	—	0	—	ns	4, 5, 6
Output Enable High to Output High-Z	t_{GHQZ}	t_{HZ}	0	4	0	5	0	6	ns	4, 5, 6

NOTES:

- \bar{W} is high for read cycle.
- Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
- All read cycle timing is referenced from the last valid address to the first transitioning address.
- At any given voltage and temperature, $t_{EHQZ} \text{ max} < t_{ELQX} \text{ min}$, and $t_{GHQZ} \text{ max} < t_{GLQX} \text{ min}$, both for a given device and from device to device.
- Transition is measured 200 mV from steady-state voltage with load of Figure 1B.
- This parameter is sampled and not 100% tested.
- Device is continuously selected ($\bar{E} = V_{IL}$, $\bar{G} = V_{IL}$).
- Addresses valid prior to or coincident with \bar{E} going low.

AC TEST LOADS

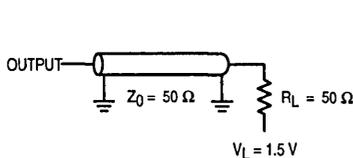


Figure 1A

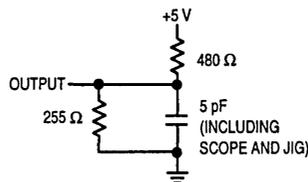


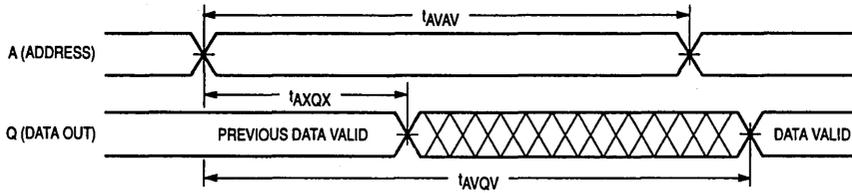
Figure 1B

TIMING LIMITS

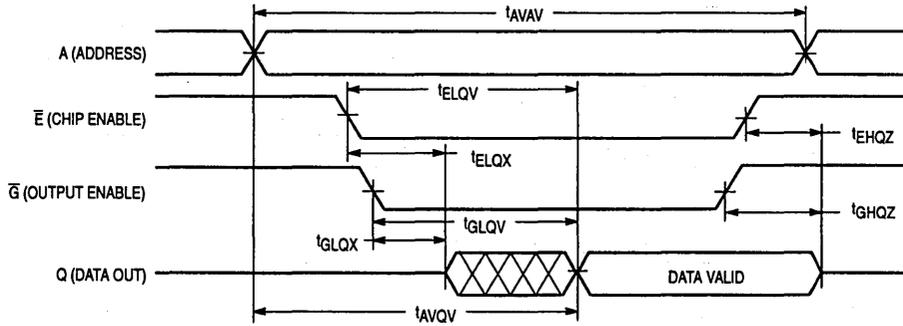
The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

NOTE: For information on output I-V characteristics, see Chapter 8, Section 1.

READ CYCLE 1 (See Note 7)



READ CYCLE 2 (See Note 8)

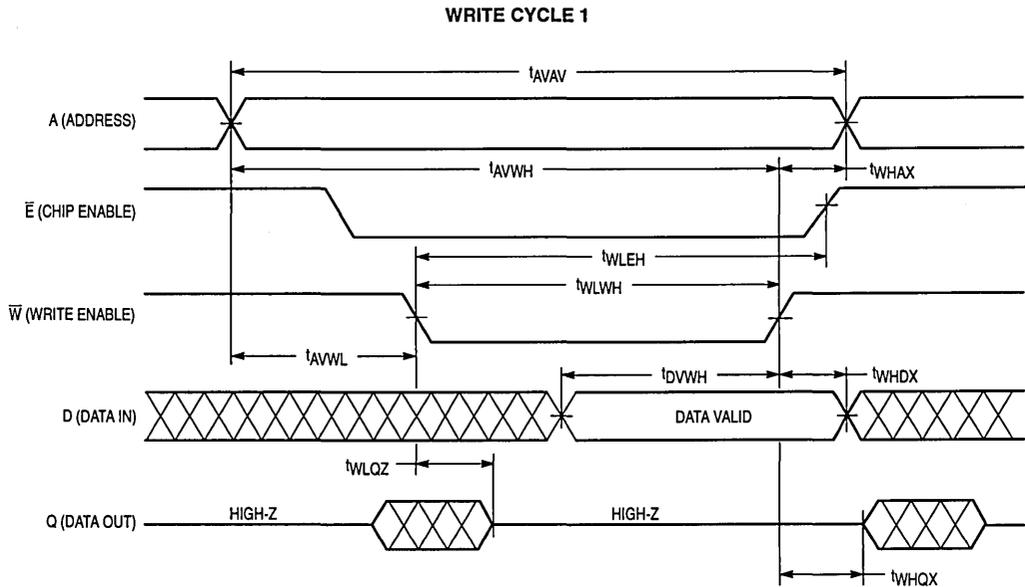


WRITE CYCLE 1 (\bar{W} Controlled, See Notes 1 and 2)

Parameter	Symbol		MCM6706A-8		MCM6706A-10		MCM6706A-12		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	8	—	10	—	12	—	ns	3
Address Setup Time	t_{AVWL}	t_{AS}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	t_{AW}	8	—	9	—	10	—	ns	
Write Pulse Width	t_{WLWH} , t_{WLEH}	t_{WP}	8	—	9	—	10	—	ns	
Data Valid to End of Write	t_{DVWH}	t_{DW}	4	—	5	—	6	—	ns	
Data Hold Time	t_{WHDX}	t_{DH}	0	—	0	—	0	—	ns	
Write Low to Data High-Z	t_{WLQZ}	t_{WZ}	0	4	0	5	0	6	ns	4, 5, 6
Write High to Output Active	t_{WHQX}	t_{OW}	3	—	3	—	3	—	ns	4, 5, 6
Write Recovery Time	t_{WHAX}	t_{WR}	0	—	0	—	0	—	ns	

NOTES:

1. A write occurs during the overlap of \bar{E} low and \bar{W} low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. Transition is measured 200 mV from steady-state voltage with load of Figure 1B.
5. Parameter is sampled and not 100% tested.
6. At any given voltage and temperature, t_{WLQZ} max is < t_{WHQX} min both for a given device and from device to device.



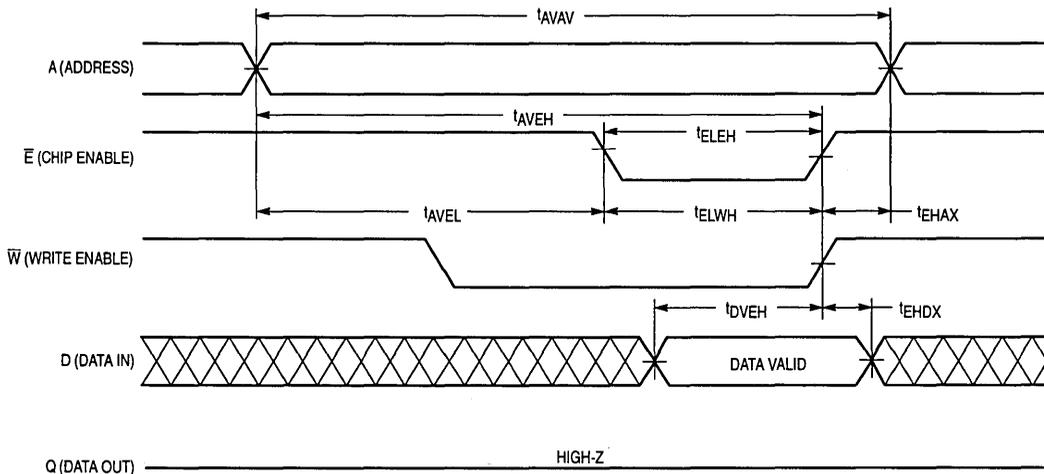
WRITE CYCLE 2 (\bar{E} Controlled, See Notes 1 and 2)

Parameter	Symbol		MCM6706A-8		MCM6706A-10		MCM6706A-12		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	8	—	10	—	12	—	ns	3
Address Setup Time	t_{AVEL}	t_{AS}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	t_{AW}	8	—	9	—	10	—	ns	
Chip Enable to End of Write	t_{ELWH} , t_{ELEH}	t_{CW}	7	—	8	—	9	—	ns	4,5
Data Valid to End of Write	t_{DVEH}	t_{DW}	4	—	5	—	6	—	ns	
Data Hold Time	t_{EHDX}	t_{DH}	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	t_{WR}	0	—	0	—	0	—	ns	

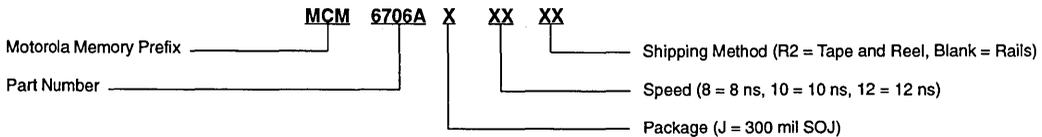
NOTES:

1. A write occurs during the overlap of \bar{E} low and \bar{W} low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All write cycle timing is referenced from the last valid address to the first transitioning address.
4. If \bar{E} goes low coincident with or after \bar{W} goes low, the output will remain in a high impedance condition.
5. If \bar{E} goes high coincident with or before \bar{W} goes high, the output will remain in a high impedance condition.

WRITE CYCLE 2



ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers — MCM6706AJ8 MCM6706AJ8R2
MCM6706AJ10 MCM6706AJ10R2
MCM6706AJ12 MCM6706AJ12R2