

MCM6726A

Product Preview

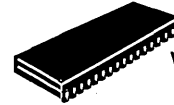
128K x 8 Bit Fast Static Random Access Memory

The MCM6726A is a 1,048,576 bit static random access memory organized as 131,072 words of 8 bits. This device is fabricated using high performance silicon-gate BiCMOS technology. Static design eliminates the need for external clocks or timing strobes.

Output enable (\bar{G}) is a special control feature that provides increased system flexibility and eliminates bus contention problems.

This device meets JEDEC standards for functionality and revolutionary pinout, and is available in a 400 mil plastic small-outline J-leaded package.

- Single 5 V \pm 10% Power Supply
- Fully Static — No Clock or Timing Strokes Necessary
- All Inputs and Outputs Are TTL Compatible
- Three State Outputs
- Fast Access Times: 8, 10, 12, 15 ns
- Center Power and I/O Pins for Reduced Noise

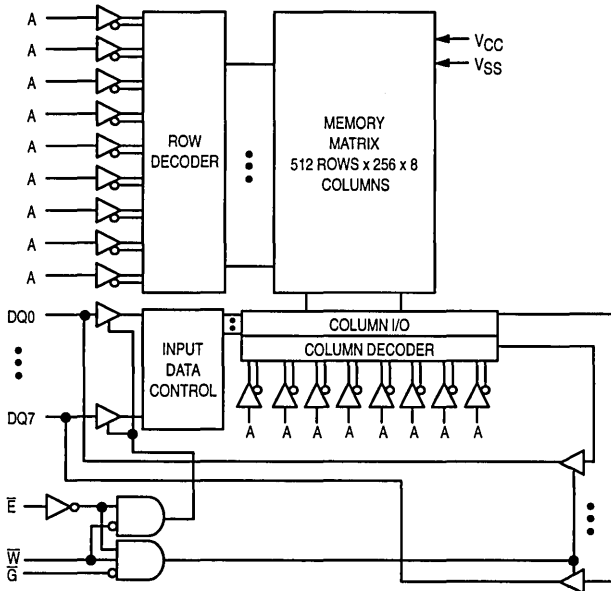


WJ PACKAGE
 400 MIL SOJ
 CASE 857A

PIN ASSIGNMENT

A	1	32	A
A	2	31	A
A	3	30	A
A	4	29	A
\bar{E}	5	28	\bar{G}
DQ0	6	27	DQ7
DQ1	7	26	DQ6
VCC	8	25	VSS
VSS	9	24	VCC
DQ2	10	23	DQ5
DQ3	11	22	DQ4
\bar{W}	12	21	A
A	13	20	A
A	14	19	A
A	15	18	A
A	16	17	A

BLOCK DIAGRAM



PIN NAMES

A0 - A16	Address Input
\bar{E}	Chip Enable
\bar{W}	Write Enable
\bar{G}	Output Enable
DQ0 - DQ7	Data Input/Output
VCC	+ 5 V Power Supply
VSS	Ground

This document contains information on a new product under development. Motorola reserves the right to change or discontinue this product without notice.

TRUTH TABLE (X = Don't Care)

\bar{E}	\bar{G}	\bar{W}	Mode	V _{CC} Current	Output	Cycle
H	X	X	Not Selected	I _{SB1} , I _{SB2}	High-Z	—
L	H	H	Output Disabled	I _{CCA}	High-Z	—
L	L	H	Read	I _{CCA}	D _{out}	Read Cycle
L	X	L	Write	I _{CCA}	High-Z	Write Cycle

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V _{CC}	- 0.5 to + 7.0	V
Voltage Relative to V _{SS} for Any Pin Except V _{CC}	V _{in} , V _{out}	- 0.5 to V _{CC} + 0.5	V
Output Current	I _{out}	± 30	mA
Power Dissipation	P _D	1.2	W
Temperature Under Bias	T _{bias}	- 10 to + 85	°C
Operating Temperature	T _A	0 to + 70	°C
Storage Temperature — Plastic	T _{stg}	- 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high-impedance circuits.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V _{CC}	4.5	5.0	5.5	V
Input High Voltage	V _{IH}	2.2	—	V _{CC} + 0.3**	V
Input Low Voltage	V _{IL}	- 0.5*	—	0.8	V

* V_{IL} (min) = -0.5 V dc; V_{IL} (min) = -2.0 V ac (pulse width ≤ 2.0 ns) for I ≤ 20.0 mA.

** V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2 V ac (pulse width ≤ 2.0 ns) for I ≤ 20.0 mA.

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V _{in} = 0 to V _{CC})	I _{kg(I)}	—	± 1.0	μA
Output Leakage Current (\bar{E} = V _{IH} , V _{out} = 0 to V _{CC})	I _{kg(O)}	—	± 1.0	μA
Output Low Voltage (I _{OL} = + 8.0 mA)	V _{OL}	—	0.4	V
Output High Voltage (I _{OH} = - 4.0 mA)	V _{OH}	2.4	—	V

POWER SUPPLY CURRENTS

Parameter	Symbol	6726A-8	6726A-10	6726A-12	6726A-15	Unit
AC Active Supply Current (I _{out} = 0 mA) (V _{CC} = max, f = f _{max})	I _{CCA}	185	175	165	155	mA
Active Quiescent Current (\bar{E} = V _{IL} , V _{CC} = max, f = 0 MHz)	I _{CC2}	100	100	100	100	mA
AC Standby Current (\bar{E} = V _{IH} , V _{CC} = max, f = f _{max})	I _{SB1}	60	60	60	60	mA
CMOS Standby Current (V _{CC} = max, f = 0 MHz, \bar{E} ≥ V _{CC} - 0.2 V, V _{in} ≤ V _{SS} + 0.2 V, or ≥ V _{CC} - 0.2 V)	I _{SB2}	20	20	20	20	mA

CAPACITANCE ($f = 1.0 \text{ MHz}$, $dV = 3.0 \text{ V}$, $T_A = 25^\circ\text{C}$, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit
Address Input Capacitance	C_{in}	—	6	pF
Control Pin Input Capacitance	C_{in}	—	6	pF
Input/Output Capacitance	$C_{I/O}$	—	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

($V_{CC} = 5.0 \text{ V} \pm 10\%$, $T_A = 0 \text{ to } +70^\circ\text{C}$, Unless Otherwise Noted)

Input Timing Measurement Reference Level	1.5 V	Output Timing Measurement Reference Level	1.5 V
Input Pulse Levels	0 to 3.0 V	Output Load	See Figure 1A
Input Rise/Fall Time	2 ns		

READ CYCLE TIMING (See Notes 1 and 2)

Parameter	Symbol		6726A-8		6726A-10		6726A-12		6726A-15		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	8	—	10	—	12	—	15	—	ns	3
Address Access Time	t_{AVQV}	t_{AA}	—	8	—	10	—	12	—	15	ns	
Enable Access Time	t_{ELQV}	t_{ACS}	—	8	—	10	—	12	—	15	ns	
Output Enable Access Time	t_{GLQV}	t_{OE}	—	4	—	5	—	6	—	7	ns	
Output Hold from Address Change	t_{AXQX}	t_{OH}	3	—	3	—	3	—	3	—	ns	
Enable Low to Output Active	t_{ELQX}	t_{CLZ}	3	—	3	—	3	—	3	—	ns	4,5,6
Output Enable Low to Output Active	t_{GLQX}	t_{OLZ}	0	—	0	—	0	—	0	—	ns	4,5,6
Enable High to Output High-Z	t_{EHQZ}	t_{CHZ}	—	4	0	5	0	6	0	7	ns	4,5,6
Output Enable High to Output High-Z	t_{GHQZ}	t_{OHZ}	—	4	0	5	0	6	0	7	ns	4,5,6

NOTES:

1. W is high for read cycle.
2. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.
3. All read cycle timings are referenced from the last valid address to the first transitioning address.
4. At any given voltage and temperature, $t_{EHQZ} \text{ max} < t_{ELQX} \text{ min}$, and $t_{GHQZ} \text{ max} < t_{GLQX} \text{ min}$, both for a given device and from device to device.
5. Transition is measured 200 mV from steady-state voltage with load of Figure 1B.
6. This parameter is sampled and not 100% tested.
7. Device is continuously selected ($\bar{E} = V_{IL}$, $\bar{G} = V_{IL}$).
8. Addresses valid prior to or coincident with \bar{E} going low.

AC TEST LOADS

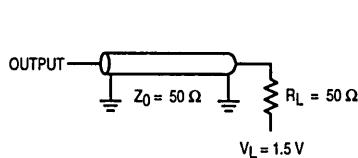


Figure 1A

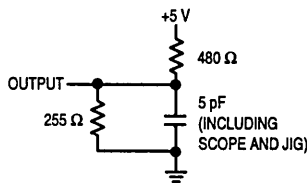


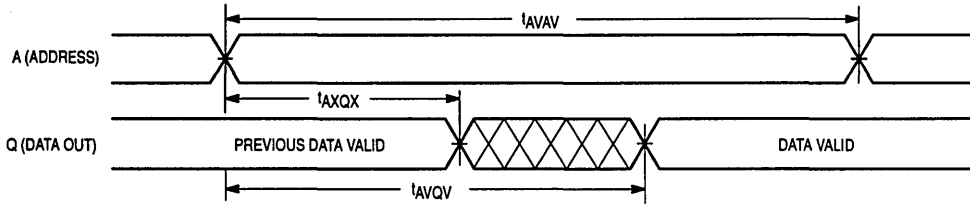
Figure 1B

TIMING LIMITS

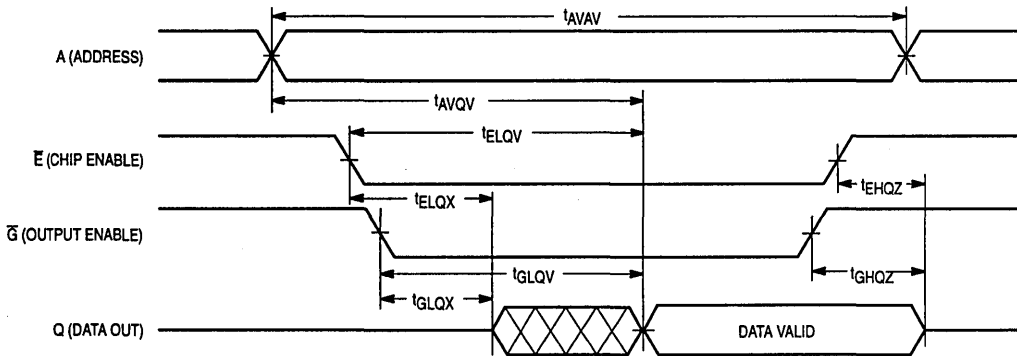
The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

NOTE: For information on output I-V characteristics, see Chapter 8, Section 1.

READ CYCLE 1 (See Note 7)



READ CYCLE 2 (See Note 8)

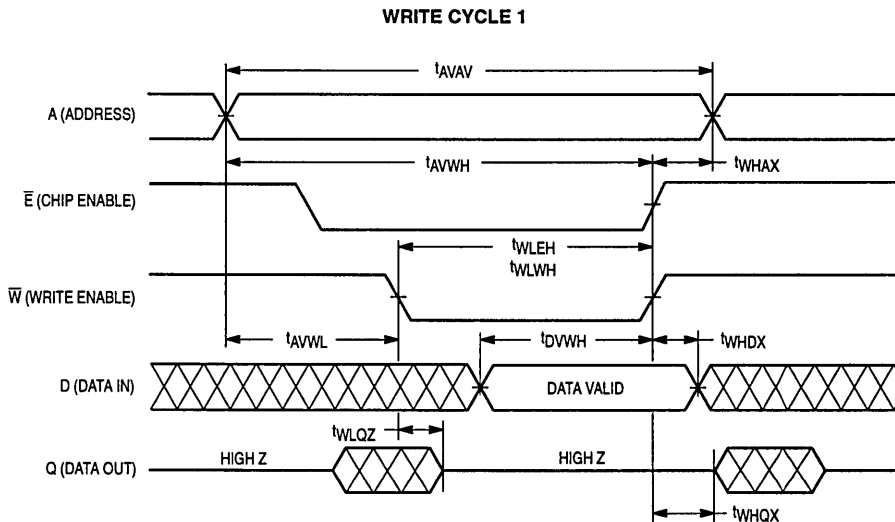


WRITE CYCLE 1 (\overline{W} Controlled, See Notes 1 and 2)

Parameter	Symbol		6726A-8		6726A-10		6726A-12		6726A-15		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	8	—	10	—	12	—	15	—	ns	3
Address Setup Time	t_{AVWL}	t_{AS}	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	t_{AW}	8	—	9	—	10	—	12	—	ns	
Address Valid to End of Write, \overline{G} High	t_{AVWH}	t_{AW}	7	—	8	—	9	—	10	—	ns	
Write Pulse Width	t_{WLWH}	t_{WP}	8	—	9	—	10	—	12	—	ns	
Write Pulse Width, \overline{G} High	t_{WLWH} t_{WLEH}	t_{WP} t_{WP}	7	—	8	—	9	—	10	—	ns	
Data Valid to End of Write	t_{DVWH}	t_{DW}	4	—	5	—	6	—	7	—	ns	
Data Hold Time	t_{WHDX}	t_{DH}	0	—	0	—	0	—	0	—	ns	
Write Low to Data High-Z	t_{WLQZ}	t_{WZ}	0	4	0	5	0	6	0	7	ns	4,5,6
Write High to Output Active	t_{WHQX}	t_{OW}	3	—	3	—	3	—	3	—	ns	4,5,6
Write Recovery Time	t_{WHAX}	t_{WR}	0	—	0	—	0	—	0	—	ns	

NOTES:

1. A write occurs during the overlap of \overline{E} low and \overline{W} low.
2. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. Transition is measured 200 mV from steady-state voltage with load of Figure 1B.
5. This parameter is sampled and not 100% tested.
6. At any given voltage and temperature, t_{WLQZ} max < t_{WHQX} min both for a given device and from device to device.



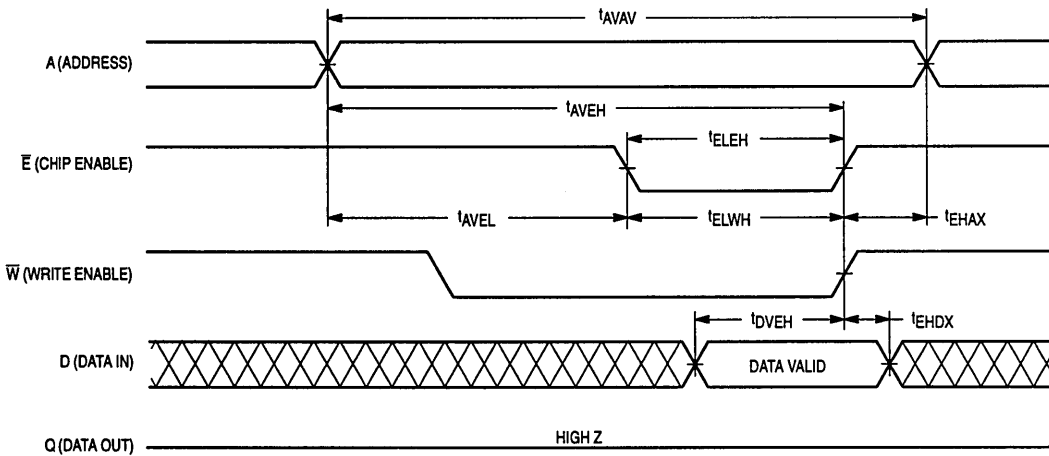
WRITE CYCLE 2 (\bar{E} Controlled, See Notes 1 and 2)

Parameter	Symbol		6726A-8		6726A-10		6726A-12		6726A-15		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	8	—	10	—	12	—	15	—	ns	3
Address Setup Time	t_{AVEL}	t_{AS}	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	t_{AW}	7	—	8	—	9	—	10	—	ns	
Enable to End of Write	t_{ELEH} t_{ELWH}	t_{CW} t_{CW}	7	—	8	—	9	—	10	—	ns	4,5
Data Valid to End of Write	t_{DVEH}	t_{DW}	4	—	5	—	6	—	7	—	ns	
Data Hold Time	t_{EHDX}	t_{DH}	0	—	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	t_{WR}	0	—	0	—	0	—	0	—	ns	

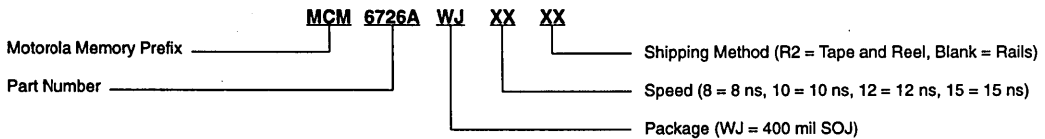
NOTES:

1. A write occurs during the overlap of \bar{E} low and \bar{W} low.
2. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. If \bar{E} goes low coincident with or after \bar{W} goes low, the output will remain in a high impedance condition.
5. If \bar{E} goes high coincident with or before \bar{W} goes high, the output will remain in a high impedance condition.

WRITE CYCLE 2



ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers — MCM6726AWJ8 MCM6726AWJ10 MCM6726AWJ12 MCM6726AWJ15
 MCM6726AWJ8R2 MCM6726AWJ10R2 MCM6726AWJ12R2 MCM6726AWJ15R2