

Product Preview

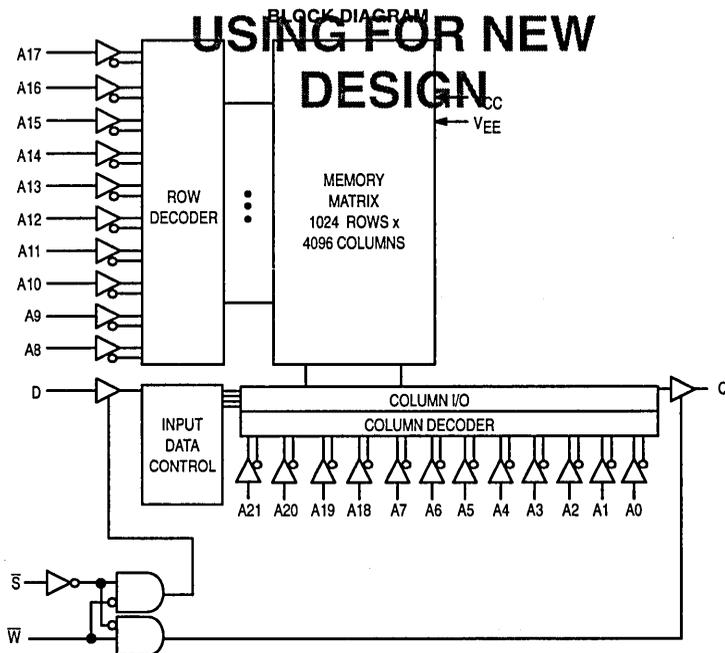
4M x 1 Bit Fast Static Random Access Memory with ECL I/O

The MCM101520 is a 4,194,304 bit static random access memory organized as 4,194,304 words of 1 bit. This circuit is fabricated using high performance silicon-gate BiCMOS technology. Asynchronous design eliminates the need for external clocks or timing strobes. This device operates across a supply voltage range of -4.94 V to -5.46 V. Inputs and outputs are voltage and temperature 100K ECL compensated.

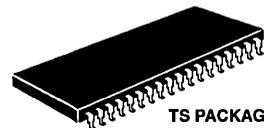
The MCM101520 meets JEDEC standards for functionality and revolutionary pin-out. It is available in 400 mil, 36 lead surface mount TSOP package as well as 36 lead TAB.

- Fast Access Times: 10, 12, 15 ns
- Equal Address and Chip Select Access Time
- Power Operation - 200 mA Maximum Quiescent Current

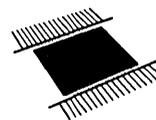
**PLEASE CONSULT
 FACTORY BEFORE
 USING FOR NEW
 DESIGN**



MCM101520



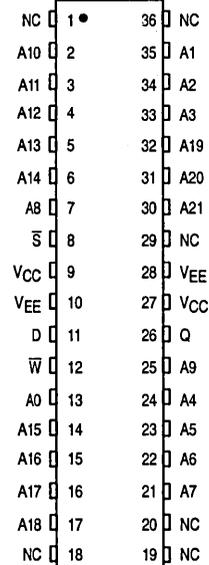
TS PACKAGE
 400 MIL TSOP
 CASE TBD



TB PACKAGE
 400 MIL TAB
 CASE TBD

2

PIN ASSIGNMENT



PIN NAMES

A0 - A21	Address Inputs	W	Write Enable
S	Chip Select	D	Data Input
Q	Data Output	NC	No Connection
VEE	Power Supply	VCC	Ground

This document contains information on a new product under development. Motorola reserves the right to change or discontinue this product without notice.

TRUTH TABLE (X = Don't Care)

\bar{S}	\bar{W}	Data	Current	Output	Cycle
H	X	X	I _{EE}	L	Not Enabled
L	H	X	I _{EE}	Q	Read Cycle
L	L	X	I _{EE}	L	Write Cycle

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
V _{EE} Pin Potential (to Ground)	V _{EE}	- 7.0 to + 0.5	V
Voltage Relative to V _{CC} for Any Pin Except V _{EE}	V _{in} , V _{out}	V _{EE} - 0.5 to + 0.5	V
Output Current (per I/O)	I _{out}	- 50	mA
Power Dissipation	P _D	2.0	W
Temperature Under Bias	T _{bias}	- 30 to + 85	°C
Operating Temperature	T _A	0 to + 70	°C
Storage Temperature — Plastic	T _{stg}	- 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high impedance circuits.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 0 V, V_{EE} = - 5.2 V ±5%, T_A = 0 to + 70°C, Unless Otherwise Noted)

DC OPERATING CONDITIONS AND SUPPLY CURRENTS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V _{EE}	- 5.46	- 5.2	- 4.94	V
Input High Voltage	V _{IH}	- 1165	—	- 880	mV
Input Low Voltage	V _{IL}	- 1810	—	- 1475	mV
Output High Voltage	V _{OH}	- 1025	—	- 880	mV
Output Low Voltage	V _{OL}	- 1810	—	- 1620	mV
Output High Corner Voltage	V _{OHc}	- 1035	—	—	mV
Output Low Corner Voltage	V _{OLc}	—	—	- 1610	mV
Input Low Current	I _{IL}	- 50	—	—	μA
Input High Current	I _{IH}	—	—	220	μA
Chip Select Input Low Current	I _{IL(CS)}	0.5	—	170	μA
Operating Power Supply Current (AVAV = 20 ns, All Outputs Open)	I _{EE}	—	—	- 195	mA
Quiescent Power Supply Current (f _o = 0 MHz (All Inputs and Outputs Open))	I _{EEQ}	—	—	- 150	mA
Voltage Compensation (V _{OH})	ΔV _{OH} /ΔV _{EE}	± 35 mV/V @ - 4.94 to - 5.46			
Voltage Compensation (V _{OL})	ΔV _{OL} /ΔV _{EE}	± 60 mV/V @ - 4.94 to - 5.46			

RISE/FALL TIME REQUIREMENTS

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Rise Time	t _r	20% to 80%	0.5	1.0	1.5	ns
Output Fall Time	t _f	20% to 80%	0.5	1.0	1.5	ns

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit	
Input Capacitance	Address and Data	C _{in}	3.5	7	pF
	S, \bar{W}	C _{ck}	4	7	
Output Capacitance	Q	C _{out}	4	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{EE} = -5.2 V ± 5%, V_{CC} = 0 V, T_A = 0 to +70°C, Unless Otherwise Noted)

Input Pulse Levels -1.7 V to -0.9 V (See Figure 1)
 Input Rise/Fall Time 1 ns
 Input Timing Measurement Reference Level 50%

Output Timing Measurement Reference Level ... V_{OH} = -1165 mV
 V_{OL} = -1475 mV
 Output Load (AC Test Circuit) See Figure 2

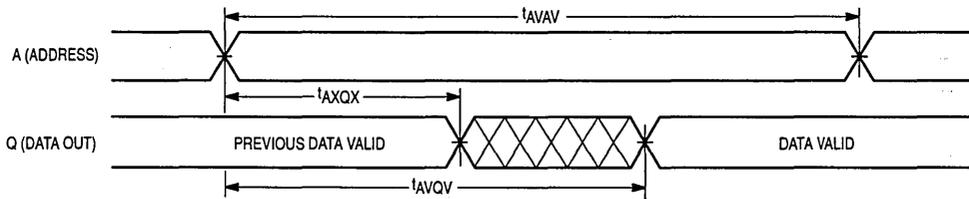
READ CYCLE TIMING (See Notes 1 and 2)

Parameter	Symbol		MCM101520-10		MCM101520-12		MCM101520-15		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t _{AVAV}	t _{RC}	10	—	12	—	15	—	ns	2, 3
Address Access Time	t _{AVQV}	t _{AA}	—	10	—	12	—	15	ns	
Chip Select Access Time	t _{SLQV}	t _{ACS}	—	10	—	12	—	15	ns	6
Select High to Output Low	t _{SHQL}	t _{RCS}	0	7	0	8	0	9	ns	
Output Hold from Address Change	t _{AXQX}	t _{OH}	4	—	4	—	4	—	ns	
Power Up Time	t _{SLIEEH}	t _{PU}	0	—	0	—	0	—	ns	4
Power Down Time	t _{SHIEEL}	t _{PD}	—	10	—	12	—	15	ns	4

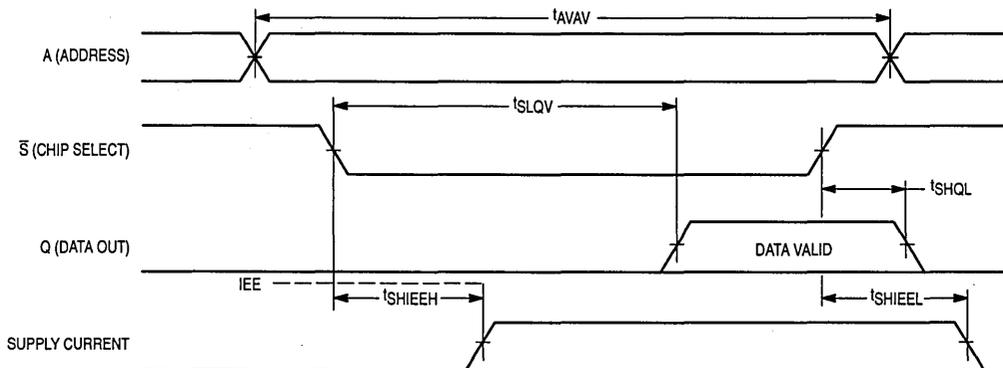
NOTES:

1. \bar{W} is high for read cycle.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies during read and write cycles.
3. All read cycle timings are referenced from the last valid address to the first transitioning address.
4. This parameter is sampled and not 100% tested.
5. Device is continuously selected ($\bar{S} \leq V_{IL}$).
6. Addresses valid prior to or coincident with \bar{S} going low.

READ CYCLE 1 (See Notes 1, 2, and 5)



READ CYCLE 2 (See Note 6)



AC TEST CONDITIONS

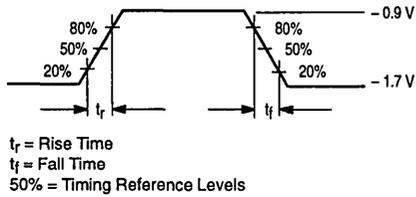


Figure 1. Input Levels

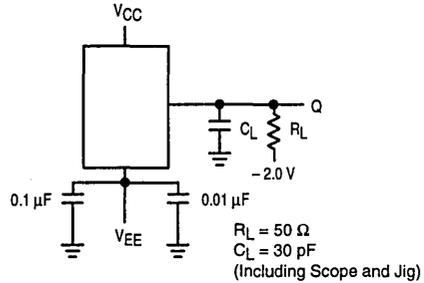


Figure 2. AC Test Circuit

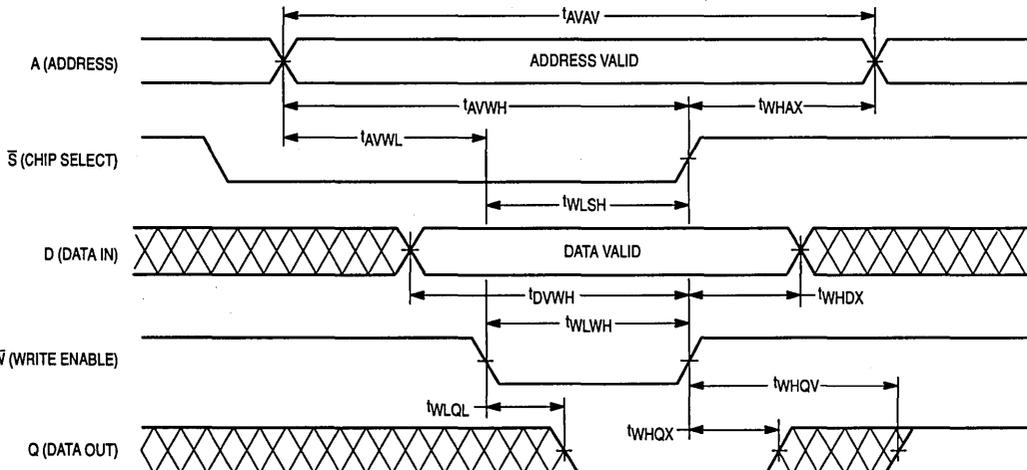
WRITE CYCLE 1 (\bar{W} Controlled, See Notes 1 and 2)

Parameter	Symbol		MCM101520-10		MCM101520-12		MCM101520-15		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	10	—	12	—	15	—	ns	3
Address Setup Time	t_{AVWL}	t_{AS}	1	—	1	—	1	—	ns	
Address Valid to End of Write	t_{AVWH}	t_{AW}	7	—	8	—	9	—	ns	
Write Pulse Width	t_{WLWH} t_{WLSH}	t_{WP}	7	—	8	—	9	—	ns	
Data Valid to End of Write	t_{DVWH}	t_{DW}	7	—	8	—	9	—	ns	
Data Hold Time	t_{WHDX}	t_{DH}	1	—	1	—	1	—	ns	
Write High to Output Active	t_{WHQX}	t_{OW}	4	—	4	—	4	—	ns	4
Write High to Output Valid	t_{WHQV}	t_{AW}	—	11	—	13	—	16	ns	
Write Recovery Time	t_{WHAX}	t_{WR}	1	—	1	—	1	—	ns	
Write Low to Output Low	t_{WLQL}	t_{WS}	0	7	0	8	0	9	ns	

NOTES:

1. A write occurs during the overlap of \bar{S} low and \bar{W} low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies during read and write cycles.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. This parameter is sampled and not 100% tested.

WRITE CYCLE 1 (\bar{W} Controlled, See Notes 1, 2, and 3)



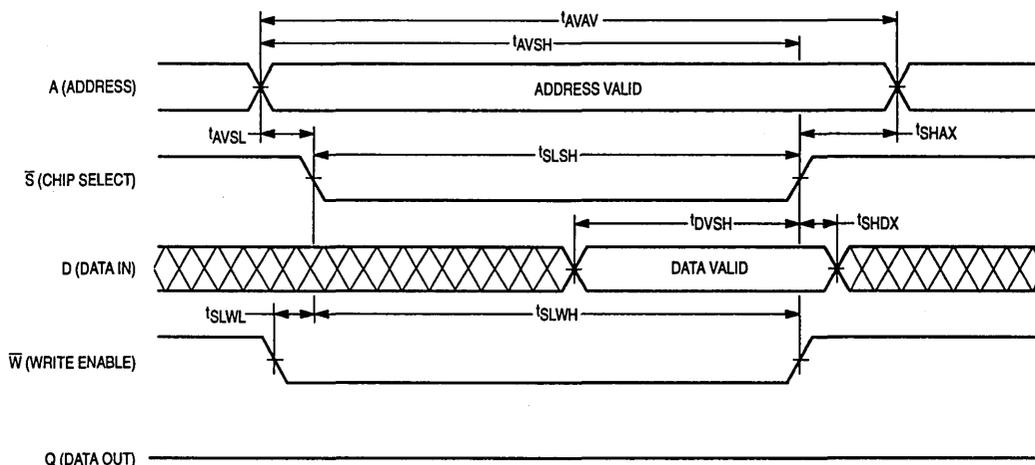
WRITE CYCLE 2 (\bar{S} Controlled, See Notes 1 and 2)

Parameter	Symbol		MCM101520-10		MCM101520-12		MCM101520-15		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	10	—	12	—	15	—	ns	3
Address Setup Time	t_{AVSL}	t_{AS}	1	—	1	—	1	—	ns	
Address Valid to End of Write	t_{AVSH}	t_{AW}	7	—	8	—	9	—	ns	
Write Pulse Width	t_{SLSH} t_{SLWH}	t_{CW}	7	—	8	—	9	—	ns	
Data Valid to End of Write	t_{DVSH}	t_{DW}	7	—	8	—	9	—	ns	
Chip Select Set-Up Time	t_{SLWL}	t_{CS}	0	—	0	—	0	—	ns	
Data Hold Time	t_{SHDX}	t_{DH}	1	—	1	—	1	—	ns	
Write Recovery Time	t_{SHAX}	t_{WR}	1	—	1	—	1	—	ns	

NOTES:

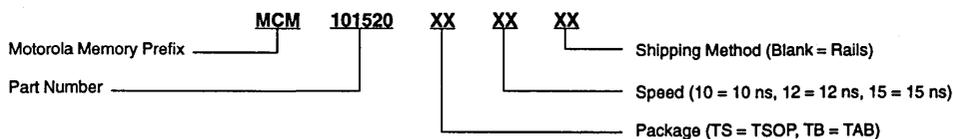
1. A write occurs during the overlap of \bar{S} low and \bar{W} low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies during read and write cycles.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.

WRITE CYCLE 2 (\bar{S} Controlled, See Notes 1 and 2)



ORDERING INFORMATION

(Order by Full Part Number)



Full Part Numbers — MCM101520TS10 MCM101520TB10
MCM101520TS12 MCM101520TB12
MCM101520TS15 MCM101520TB15