

*Product Preview*  
**256K x 4 Bit Static Random Access Memory**

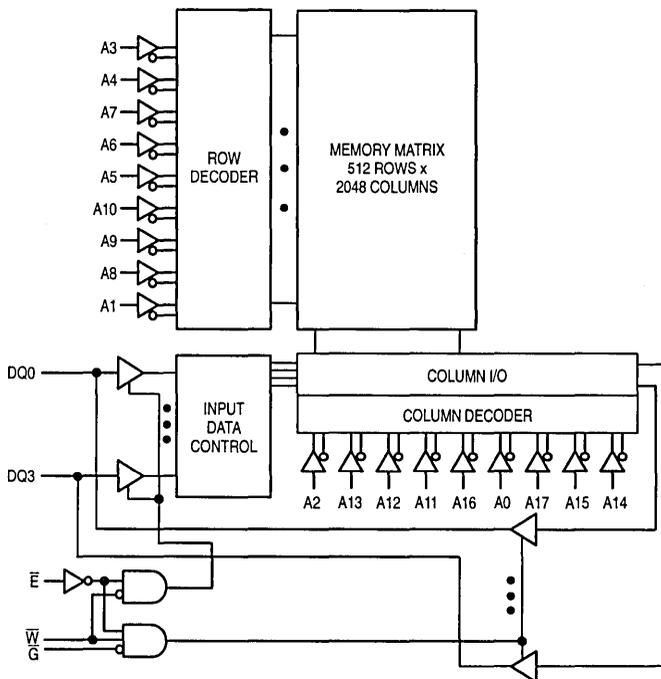
The MCM6229B is a 1,048,576 bit static random access memory organized as 262,144 words of 4 bits, fabricated using high-performance silicon-gate CMOS technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides for greater reliability.

The MCM6229B is equipped with both chip enable ( $\bar{E}$ ) and output enable ( $\bar{G}$ ) pins, allowing for greater system flexibility and eliminating bus contention problems. Either input, when high, will force the outputs to high impedance.

The MCM6229B is available in 300 mil and 400 mil, 28-lead surface-mount SOJ packages.

- Single 5 V  $\pm$  10% Power Supply
- Fast Access Times: 15/17/20/25/35 ns
- Equal Address and Chip Enable Access Times
- All Inputs and Outputs are TTL Compatible
- Three-State Outputs
- Low Power Operation: 120/115/110/105/100 mA Maximum, Active AC

**BLOCK DIAGRAM**



This document contains information on a new product under development. Motorola reserves the right to change or discontinue this product without notice.

**MCM6229B**



J PACKAGE  
 300 MIL SOJ  
 CASE 810B

WJ PACKAGE  
 400 MIL SOJ  
 CASE 810

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**PIN ASSIGNMENT**

A0	1	28	VCC
A1	2	27	A17
A2	3	26	A16
A3	4	25	A15
A4	5	24	A14
A5	6	23	A13
A6	7	22	A12
A7	8	21	A11
A8	9	20	NC*
A9	10	19	DQ3
A10	11	18	DQ2
$\bar{E}$	12	17	DQ1
$\bar{G}$	13	16	DQ0
VSS	14	15	$\bar{W}$

**PIN NAMES**

A0 - A17	Address Inputs
$\bar{W}$	Write Enable
$\bar{G}$	Output Enable
$\bar{E}$	Chip Enable
DQ0 - DQ3	Data Inputs/Outputs
VCC	+ 5 V Power Supply
VSS	Ground
NC	No Connection

\*If not used for no connect, then do not exceed voltages of - 0.5 to VCC + 0.5 V. This pin is used for manufacturing diagnostics.

### TRUTH TABLE

$\bar{E}$	$\bar{G}$	$\bar{W}$	Mode	I/O Pin	Cycle	Current
H	X	X	Not Selected	High-Z	—	$I_{SB1}$ , $I_{SB2}$
L	H	H	Output Disabled	High-Z	—	$I_{CCA}$
L	L	H	Read	$D_{out}$	Read	$I_{CCA}$
L	X	L	Write	$D_{in}$	Write	$I_{CCA}$

H = High, L = Low, X = Don't Care

### ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage Relative to $V_{SS}$	$V_{CC}$	- 0.5 to 7.0	V
Voltage Relative to $V_{SS}$ for Any Pin Except $V_{CC}$	$V_{in}$ , $V_{out}$	- 0.5 to $V_{CC} + 0.5$	V
Output Current (per I/O)	$I_{out}$	$\pm 20$	mA
Power Dissipation	$P_D$	1.1	W
Temperature Under Bias	$T_{bias}$	- 10 to + 85	$^{\circ}C$
Operating Temperature	$T_A$	0 to + 70	$^{\circ}C$
Storage Temperature	$T_{stg}$	- 55 to + 150	$^{\circ}C$

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

### DC OPERATING CONDITIONS AND CHARACTERISTICS

( $V_{CC} = 5.0 V \pm 10\%$ ,  $T_A = 0$  to  $70^{\circ}C$ , Unless Otherwise Noted)

#### RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	$V_{CC}$	4.5	5.5	V
Input High Voltage	$V_{IH}$	2.2	$V_{CC} + 0.3^{**}$	V
Input Low Voltage	$V_{IL}$	- 0.5*	0.8	V

\* $V_{IL}$  (min) = - 0.5 V dc;  $V_{IL}$  (min) = - 2.0 V ac (pulse width  $\leq 20$  ns).

\*\* $V_{IH}$  (max) =  $V_{CC} + 0.3$  V dc;  $V_{IH}$  (max) =  $V_{CC} + 2$  V ac (pulse width  $\leq 20$  ns).

#### DC CHARACTERISTICS AND SUPPLY CURRENTS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, $V_{in} = 0$ to $V_{CC}$ )	$I_{kg(I)}$	—	$\pm 1$	$\mu A$
Output Leakage Current ( $\bar{E} = V_{IH}$ , $V_{out} = 0$ to $V_{CC}$ )	$I_{kg(O)}$	—	$\pm 1$	$\mu A$
AC Active Supply Current ( $I_{out} = 0$ mA, $V_{CC} = \max$ )	$I_{CCA}$	—	120 115 110 100 95	mA
AC Standby Current ( $V_{CC} = \max$ , $\bar{E} = V_{IH}$ , $f = f_{max}$ )	$I_{SB1}$	—	35 35 30 25 20	mA
CMOS Standby Current ( $\bar{E} \geq V_{CC} - 0.2$ V, $V_{in} \leq V_{SS} + 0.2$ V or $\geq V_{CC} - 0.2$ V, $V_{CC} = \max$ , $f = 0$ MHz)	$I_{SB2}$	—	15	mA
Output Low Voltage ( $I_{OL} = + 8.0$ mA)	$V_{OL}$	—	0.4	V
Output High Voltage ( $I_{OH} = - 4.0$ mA)	$V_{OH}$	2.4	—	V

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high-impedance circuits.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

**CAPACITANCE** (f = 1.0 MHz, dV = 3.0 V, T<sub>A</sub> = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Typ	Max	Unit	
Input Capacitance	All Inputs except Clocks & DQs	C <sub>in</sub>	4	6	pF
	E, $\bar{G}$ , and W	C <sub>ck</sub>	5	8	
Input/Output Capacitance	DQ	C <sub>I/O</sub>	5	8	pF

**AC OPERATING CONDITIONS AND CHARACTERISTICS**

(V<sub>CC</sub> = 5.0 V ± 10%, T<sub>A</sub> = 0 to + 70°C, Unless Otherwise Noted)

Input Pulse Levels	0 to 3.0 V	Output Timing Measurement Reference Level	1.5 V
Input Rise/Fall Time	2 ns	Output Load	See Figure 1A
Input Timing Measurement Reference Level	1.5 V		

**READ CYCLE TIMING** (See Notes 1 and 2)

Parameter	Symbol		6229B-15		6229B-17		6229B-20		6229B-25		6229B-35		Unit	Notes
	Std	Alt	Min	Max										
Read Cycle Time	t <sub>AVAV</sub>	t <sub>RC</sub>	15	—	17	—	20	—	25	—	35	—	ns	2, 3
Address Access Time	t <sub>AVQV</sub>	t <sub>AA</sub>	—	15	—	17	—	20	—	25	—	35	ns	
Enable Access Time	t <sub>ELQV</sub>	t <sub>ACS</sub>	—	15	—	17	—	20	—	25	—	35	ns	4
Output Enable Access Time	t <sub>GLQV</sub>	t <sub>OE</sub>	—	6	—	7	—	7	—	8	—	8	ns	
Output Hold from Address Change	t <sub>AXQX</sub>	t <sub>OH</sub>	5	—	5	—	5	—	5	—	5	—	ns	
Enable Low to Output Active	t <sub>ELQX</sub>	t <sub>ELZ</sub>	5	—	5	—	5	—	5	—	5	—	ns	5, 6, 7
Output Enable Low to Output Active	t <sub>GLQX</sub>	t <sub>GLZ</sub>	0	—	0	—	0	—	0	—	0	—	ns	5, 6, 7
Enable High to Output High-Z	t <sub>EHQZ</sub>	t <sub>EHZ</sub>	0	6	0	7	0	7	0	8	0	8	ns	5, 6, 7
Output Enable High to Output High-Z	t <sub>GHQZ</sub>	t <sub>ELZ</sub>	0	6	0	7	0	7	0	8	0	8	ns	5, 6, 7

**NOTES:**

1.  $\bar{W}$  is high for read cycle.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All timings are referenced from the last valid address to the first transitioning address.
4. Addresses valid prior to or coincident with  $\bar{E}$  going low.
5. At any given voltage and temperature, t<sub>EHQZ</sub> max is less than t<sub>ELQX</sub> min, and t<sub>GHQZ</sub> max is less than t<sub>GLQX</sub> min, both for a given device and from device to device.
6. Transition is measured ± 500 mV from steady-state voltage with load of Figure 1B.
7. This parameter is sampled and not 100% tested.
8. Device is continuously selected ( $\bar{E} \leq V_{IL}$ ,  $\bar{G} \leq V_{IL}$ ).

**AC TEST LOADS**

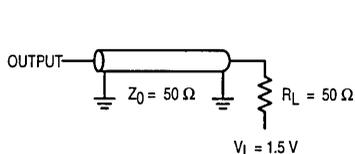


Figure 1A

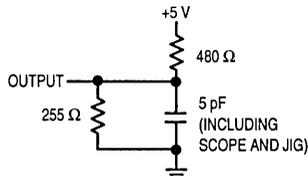
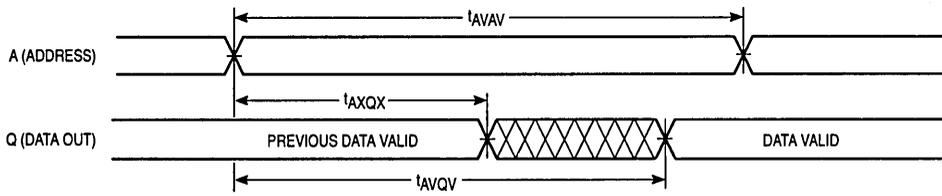


Figure 1B

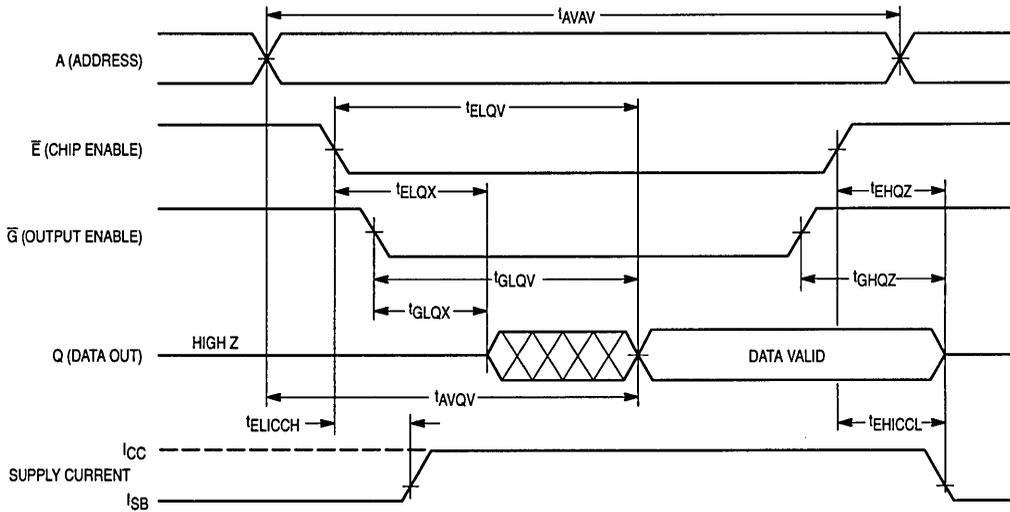
**TIMING LIMITS**

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

**READ CYCLE 1** (See Notes 1, 2, and 8)



**READ CYCLE 2** (See Note 8)



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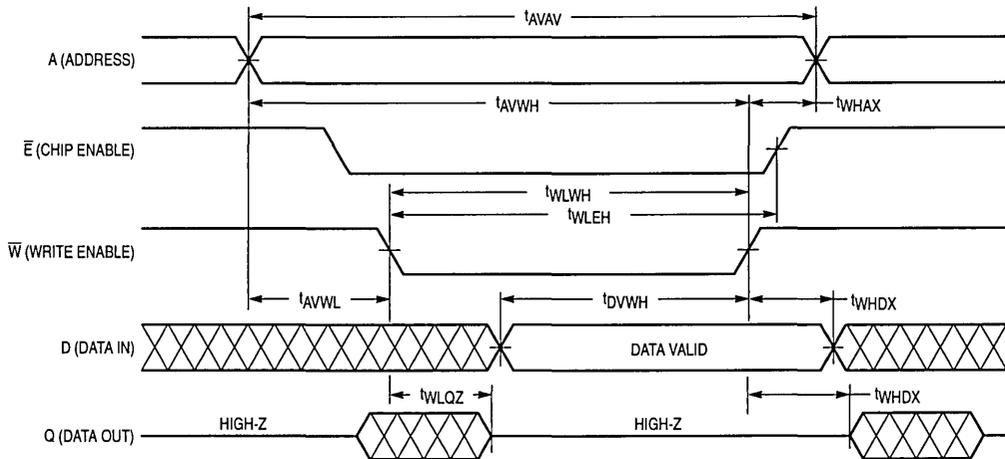
**WRITE CYCLE 1** ( $\overline{W}$  Controlled, See Notes 1, 2, and 3)

Parameter	Symbol		6229B-15		6229B-17		6229B-20		6229B-25		6229B-35		Unit	Notes
	Std	Alt	Min	Max										
Write Cycle Time	$t_{AVAV}$	$t_{WC}$	15	—	17	—	20	—	25	—	35	—	ns	4
Address Setup Time	$t_{AVWL}$	$t_{AS}$	0	—	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	$t_{AVWH}$	$t_{AW}$	12	—	14	—	15	—	17	—	20	—	ns	
Write Pulse Width	$t_{WLWH}$	$t_{WP}$	12	—	14	—	15	—	17	—	20	—	ns	
Data Valid to End of Write	$t_{DVWH}$	$t_{DW}$	7	—	8	—	8	—	10	—	11	—	ns	
Data Hold Time	$t_{WHDX}$	$t_{DH}$	0	—	0	—	0	—	0	—	0	—	ns	
Write Low to Data High-Z	$t_{WLQZ}$	$t_{WZ}$	0	6	0	7	0	7	0	8	0	8	ns	5, 6, 7
Write High to Output Active	$t_{WHQX}$	$t_{OW}$	5	—	5	—	5	—	5	—	5	—	ns	5, 6, 7
Write Recovery Time	$t_{WHAX}$	$t_{WR}$	0	—	0	—	0	—	0	—	0	—	ns	

**NOTES:**

1. A write occurs during the overlap of  $\overline{E}$  low and  $\overline{W}$  low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. If  $\overline{G}$  goes low coincident with or after  $\overline{W}$  goes low, the output will remain in a high-impedance state.
4. All timings are referenced from the last valid address to the first transitioning address.
5. Transition is measured  $\pm 500$  mV from steady-state voltage with load of Figure 1B.
6. This parameter is sampled and not 100% tested.
7. At any given voltage and temperature,  $t_{WLQZ}$  max is less than  $t_{WHQX}$  min both for a given device and from device to device.

**WRITE CYCLE 1** ( $\overline{W}$  Controlled See Notes 1, 2, and 3)



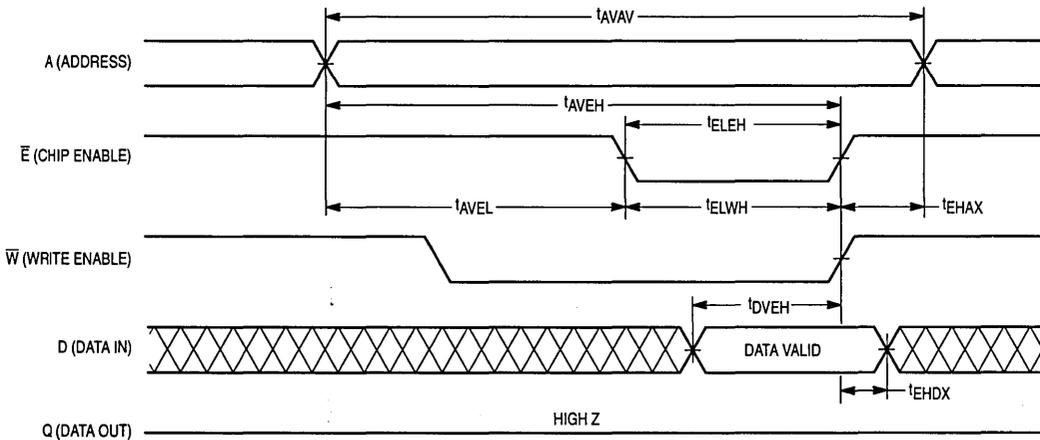
**WRITE CYCLE 2** ( $\bar{E}$  Controlled, See Notes 1, 2, and 3)

Parameter	Symbol		6229B-15		6229B-17		6229B-20		6229B-25		6229B-35		Unit	Notes
	Std	Alt	Min	Max										
Write Cycle Time	t <sub>AVAV</sub>	t <sub>WC</sub>	15	—	17	—	20	—	25	—	35	—	ns	4
Address Setup Time	t <sub>AVEL</sub>	t <sub>AS</sub>	0	—	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t <sub>AVEH</sub>	t <sub>AW</sub>	12	—	14	—	15	—	17	—	20	—	ns	
Enable to End of Write	t <sub>ELEH</sub>	t <sub>CW</sub>	10	—	11	—	12	—	15	—	20	—	ns	5, 6
Enable to End of Write	t <sub>ELWH</sub>	t <sub>CW</sub>	10	—	11	—	12	—	15	—	20	—	ns	
Data Valid to End of Write	t <sub>DVEH</sub>	t <sub>DW</sub>	7	—	8	—	8	—	10	—	11	—	ns	
Data Hold Time	t <sub>EHDX</sub>	t <sub>DH</sub>	0	—	0	—	0	—	0	—	0	—	ns	
Write Recovery Time	t <sub>EHAX</sub>	t <sub>WR</sub>	0	—	0	—	0	—	0	—	0	—	ns	

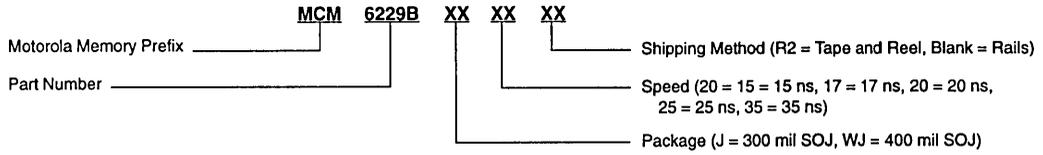
**NOTES:**

1. A write occurs during the overlap of  $\bar{E}$  low and  $\bar{W}$  low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. If  $\bar{G}$  goes low coincident with or after  $\bar{W}$  goes low, the output will remain in a high-impedance state.
4. All timings are referenced from the last valid address to the first transitioning address.
5. If  $\bar{E}$  goes low coincident with or after  $\bar{W}$  goes low, the output will remain in a high-impedance state.
6. If  $\bar{E}$  goes high coincident with or before  $\bar{W}$  goes high, the output will remain in a high-impedance state.

**WRITE CYCLE 2** ( $\bar{E}$  Controlled See Notes 1, 2, and 3)



**ORDERING INFORMATION**  
(Order by Full Part Number)



Full Part Numbers —

MCM6229BJ15	MCM6229BJ15R2
MCM6229BJ17	MCM6229BJ17R2
MCM6229BJ20	MCM6229BJ20R2
MCM6229BJ25	MCM6229BJ25R2
MCM6229BJ35	MCM6229BJ35R2
MCM6229BWJ15	MCM6229BWJ15R2
MCM6229BWJ17	MCM6229BWJ17R2
MCM6229BWJ20	MCM6229BWJ20R2
MCM6229BWJ25	MCM6229BWJ25R2
MCM6229BWJ35	MCM6229BWJ35R2