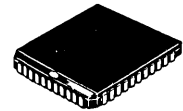


**MCM62940B**

*Advance Information*

**32K x 9 Bit BurstRAM™**  
**Synchronous Static RAM**  
**With Burst Counter and Self-Timed Write**



**FN PACKAGE**  
**44-LEAD PLCC**  
**CASE 777**

The MCM62940B is a 294,912 bit synchronous static random access memory designed to provide a burstable, high-performance, secondary cache for the MC68040 and PowerPC™ microprocessors. It is organized as 32,768 words of 9 bits, fabricated using Motorola's high-performance silicon-gate CMOS technology. The device integrates input registers, a 2-bit counter, high speed SRAM, and high drive capability outputs onto a single monolithic circuit for reduced parts count implementation of cache data RAM applications. Synchronous design allows precise cycle control with the use of an external clock (K). CMOS circuitry reduces the overall power consumption of the integrated functions for greater reliability.

Addresses (A0 – A14), data inputs (DQ0 – DQ8), and all control signals, except output enable ( $\bar{G}$ ), are clock (K) controlled through positive-edge-triggered noninverting registers.

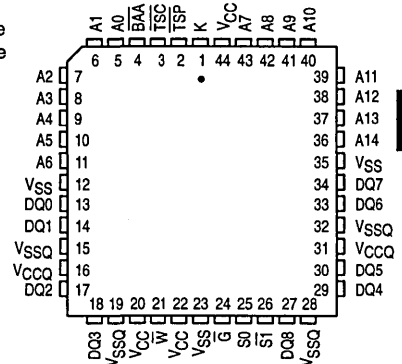
Bursts can be initiated with either transfer start processor ( $\bar{TSP}$ ) or transfer start cache controller ( $\bar{TSC}$ ) input pins. Subsequent burst addresses are generated internally by the MCM62940B (burst sequence imitates that of the MC68040 and PowerPC) and controlled by the burst address advance ( $\bar{BAA}$ ) input pin. The following pages provide more detailed information on burst controls.

Write cycles are internally self-timed and are initiated by the rising edge of the clock (K) input. This feature eliminates complex off-chip write pulse generation and provides increased flexibility for incoming signals.

The MCM62940B is packaged in a 44-pin plastic-leaded chip carrier (PLCC). Multiple power and ground pins have been utilized to minimize effects induced by output noise. Separate power and ground pins have been employed for DQ0 – DQ8 to allow user-controlled output levels of 5 volts or 3.3 volts.

- Single 5 V ± 10% Power Supply
- Choice of 5 V or 3.3 V ± 10% Power Supplies for Output Level Compatibility
- Fast Access Times: 11/12/14/19/24 ns Max, Cycle Times: 15/20/20/25/30 ns Min
- Internal Input Registers (Address, Data, Control)
- Internally Self-Timed Write Cycle
- $\bar{TSP}$ ,  $\bar{TSC}$ , and  $\bar{BAA}$  Burst Control Pins
- Asynchronous Output Enable Controlled Three-State Outputs
- Common Data Inputs and Data Outputs
- High Output Drive Capability: 85 pF per I/O
- High Board Density PLCC Package
- Fully TTL-Compatible
- Active High and Low Chip Select Inputs for Easy Depth Expansion

**PIN ASSIGNMENT**



**4**

**PIN NAMES**

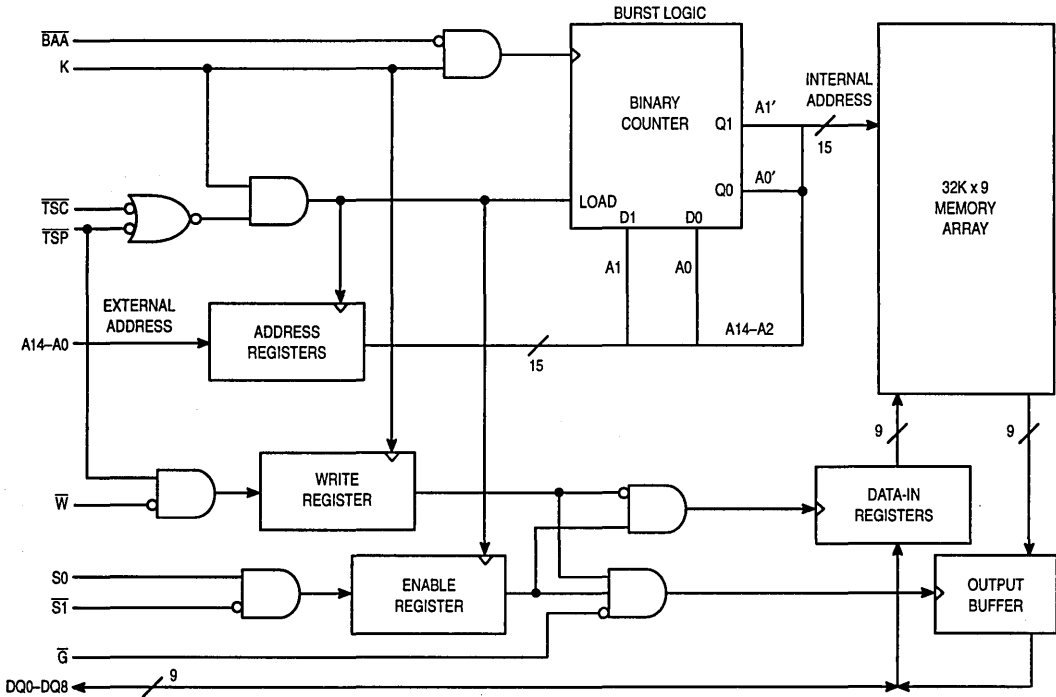
A0 – A14	Address Inputs
K	Clock
$\bar{W}$	Synchronous Write
$\bar{G}$	Output Enable
S0, $\bar{S}1$	Chip Selects
$\bar{BAA}$	Burst Address Advance
$\bar{TSP}$ , $\bar{TSC}$	Transfer Start
DQ0 – DQ8	Data Input/Output
VCC	+ 5 V Power Supply
VCCQ	Output Buffer Power Supply
VSS	Ground
VSSQ	Output Buffer Ground

All power supply and ground pins must be connected for proper operation of the device.  $V_{CC} \geq V_{CCQ}$  at all times including power up.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

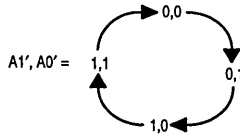
BurstRAM is a trademark of Motorola, Inc.  
 PowerPC is a trademark of IBM Corp.

**BLOCK DIAGRAM** (See Note)



**NOTE:** All registers are positive-edge triggered. The  $\overline{TSC}$  or  $\overline{TSP}$  signals control the duration of the burst and the start of the next burst. When  $\overline{TSP}$  is sampled low, any ongoing burst is interrupted and a read (independent of  $\overline{W}$  and  $\overline{TSC}$ ) is performed using the new external address. When  $\overline{TSC}$  is sampled low (and  $\overline{TSP}$  is sampled high), any ongoing burst is interrupted and a read or write (dependent on  $\overline{W}$ ) is performed using the next external address. Chip selects ( $S_0$ ,  $\overline{S_1}$ ) are sampled only when a new base address is loaded. After the first cycle of the burst,  $\overline{BAA}$  controls subsequent burst cycles. When  $\overline{BAA}$  is sampled low, the internal address is advanced prior to the operation. When  $\overline{BAA}$  is sampled high, the internal address is not advanced, thus inserting a wait state into the burst sequence accesses. Upon completion of a burst, the address will wrap around to its initial state. See **BURST SEQUENCE GRAPH**.

**BURST SEQUENCE GRAPH** (See Note)



**NOTE:** The external two values for A1 and A0 provide the starting point for the burst sequence graph. The burst logic advances A1 and A0 as shown above.

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**SYNCHRONOUS TRUTH TABLE** (See Notes 1, 2, 3, and 4)

S	TSP	TSC	BAA	W	K	Address	Operation
F	L	X	X	X	L-H	N/A	Deselected
F	X	L	X	X	L-H	N/A	Deselected
T	L	X	X	X	L-H	External Address	Read Cycle, Begin Burst
T	H	L	X	L	L-H	External Address	Write Cycle, Begin Burst
T	H	L	X	H	L-H	External Address	Read Cycle, Begin Burst
X	H	H	L	L	L-H	Next Address	Write Cycle, Continue Burst
X	H	H	L	H	L-H	Next Address	Read Cycle, Continue Burst
X	H	H	H	L	L-H	Current Address	Write Cycle, Suspend Burst
X	H	H	H	H	L-H	Current Address	Read Cycle, Suspend Burst

**NOTES:**

1. X means Don't Care.
2. All inputs except  $\bar{G}$  must meet setup and hold times for the low-to-high transition of clock (K).
3. S represents S0 and ST. T implies S0 = H and ST = L; F implies S0 = L or ST = H.
4. Wait states are inserted by suspending burst.

**ASYNCHRONOUS TRUTH TABLE** (See Notes 1 and 2)

Operation	$\bar{G}$	I/O Status
Read	L	Data Out (DQ0-DQ8)
Read	H	High-Z
Write	X	High-Z — Data In (DQ0-DQ8)
Deselected	X	High-Z

**NOTES:**

1. X means Don't Care.
2. For a write operation following a read operation,  $\bar{G}$  must be high before the input data require setup time and held high throughout the input data hold time.

**ABSOLUTE MAXIMUM RATINGS** (Voltages referenced to  $V_{SS} = 0$ )

Rating	Symbol	Value	Unit
Power Supply Voltage	$V_{CC}$	-0.5 to 7.0	V
Output Power Supply Voltage	$V_{CCQ}$	-0.5 to $V_{CC}$	V
Voltage Relative to $V_{SS}$	$V_{in}, V_{out}$	-0.5 to $V_{CC} + 0.5$	V
Output Current (per I/O)	$I_{out}$	$\pm 20$	mA
Power Dissipation	$P_D$	1.0	W
Temperature Under Bias	$T_{bias}$	-10 to +85	°C
Operating Temperature	$T_A$	0 to +70	°C
Storage Temperature	$T_{stg}$	-55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

## DC OPERATING CONDITIONS AND CHARACTERISTICS

( $V_{CC} = 5.0\text{ V} \pm 10\%$ ,  $V_{CCQ} = 5.0\text{ V}$  or  $3.3\text{ V} \pm 10\%$ ,  $T_A = 0$  to  $+70^\circ\text{C}$ , Unless Otherwise Noted)

### RECOMMENDED OPERATING CONDITIONS (Voltages referenced to $V_{SS} = 0\text{ V}$ )

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	$V_{CC}$	4.5	5.0	5.5	V
Output Buffer Supply Voltage (5.0 V TTL Compatible) (3.3 V 50 $\Omega$ Compatible)	$V_{CCQ}$	4.5 3.0	5.0 3.3	5.5 3.6	V
Input High Voltage	$V_{IH}$	2.2	—	$V_{CC} + 0.3$	V
Input Low Voltage	$V_{IL}$	-0.5*	—	0.8	V

\*  $V_{IL}$  (min) = -3.0 V ac (pulse width  $\leq 20\text{ ns}$ )

### DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, $V_{in} = 0$ to $V_{CC}$ )	$I_{kg}(I)$	—	$\pm 1.0$	$\mu\text{A}$
Output Leakage Current ( $\bar{G}, \bar{S1} = V_{IH}, S0 = V_{IL}, V_{out} = 0$ to $V_{CCQ}$ )	$I_{kg}(O)$	—	$\pm 1.0$	$\mu\text{A}$
AC Supply Current ( $\bar{G}, \bar{S1} = V_{IL}, S0 = V_{IH}$ , All Inputs = $V_{IL} = 0\text{ V}$ and $V_{IH} \geq 3.0\text{ V}$ , $I_{out} = 0\text{ mA}$ , Cycle Time $\geq t_{KHKH}$ min)	$I_{CCA}$	—	150	mA
Standby Current ( $\bar{S1} = V_{IH}, S0 = V_{IL}$ , All Inputs = $V_{IL}$ and $V_{IH}$ , Cycle Time $\geq t_{KHKH}$ min)	$I_{SB1}$	—	40	mA
CMOS Standby Current ( $\bar{S1} \geq V_{CC} - 0.2\text{ V}, S0 \leq 0.2\text{ V}$ , All Inputs $\geq V_{CC} - 0.2\text{ V}$ or $\leq 0.2\text{ V}$ , Cycle Time $\geq t_{KHKH}$ min)	$I_{SB2}$	—	20	mA
Output Low Voltage ( $I_{OL} = +8.0\text{ mA}$ )	$V_{OL}$	—	0.4	V
Output High Voltage ( $I_{OH} = -4.0\text{ mA}$ )	$V_{OH}$	2.4	—	V

NOTE: Good decoupling of the local power supply should always be used. DC characteristics are guaranteed for all possible MC68040 bus cycles.

### CAPACITANCE ( $f = 1.0\text{ MHz}$ , $dV = 3.0\text{ V}$ , $T_A = 25^\circ\text{C}$ , Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance (All Pins Except DQ0 - DQ8)	$C_{in}$	2	3	pF
Input/Output Capacitance (DQ0 - DQ8)	$C_{I/O}$	7	8	pF

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## AC OPERATING CONDITIONS AND CHARACTERISTICS

( $V_{CC} = 5.0\text{ V} \pm 10\%$ ,  $V_{CCQ} = 5.0\text{ V}$  or  $3.3\text{ V} \pm 10\%$ ,  $T_A = 0$  to  $+70^\circ\text{C}$ , Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V  
 Input Pulse Levels ..... 0 to 3.0 V  
 Input Rise/Fall Time ..... 3 ns

Output Timing Reference Level ..... 1.5 V  
 Output Load ..... See Figure 1A Unless Otherwise Noted

### READ/WRITE CYCLE TIMING (See Notes 1, 2, and 3)

Parameter	Symbol		62940B-11		62940B-12		62940B-14		62940B-19		62940B-24		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Cycle Time	t <sub>KHKH</sub>	t <sub>CYC</sub>	15	—	20	—	20	—	25	—	30	—	ns	
Clock Access Time	t <sub>KHQV</sub>	t <sub>CD</sub>	—	11	—	12	—	14	—	19	—	24	ns	4
Output Enable to Output Valid	t <sub>GLQV</sub>	t <sub>OE</sub>	—	5	—	5	—	6	—	7	—	7	ns	
Clock High to Output Active	t <sub>KHQX1</sub>	t <sub>DC1</sub>	6	—	6	—	6	—	6	—	6	—	ns	
Clock High to Output Change	t <sub>KHQX2</sub>	t <sub>DC2</sub>	3	—	3	—	5	—	5	—	5	—	ns	
Output Enable to Output Active	t <sub>GLQX</sub>	t <sub>OLZ</sub>	0	—	0	—	0	—	0	—	0	—	ns	
Output Disable to Q High-Z	t <sub>GHQZ</sub>	t <sub>OHZ</sub>	—	6	—	6	—	6	—	7	—	7	ns	5
Clock High to Q High-Z	t <sub>KHQZ</sub>	t <sub>CZ</sub>	—	6	—	6	—	6	—	6	—	6	ns	5
Clock High Pulse Width	t <sub>KHKL</sub>	t <sub>CH</sub>	5.5	—	7	—	8	—	9	—	11	—	ns	
Clock Low Pulse Width	t <sub>KLKH</sub>	t <sub>CL</sub>	5.5	—	7	—	8	—	9	—	11	—	ns	
Setup Times:	Address	t <sub>AVKH</sub>	2	—	2	—	3	—	3	—	3	—	ns	6
	Address Status	t <sub>TSVKH</sub>												
	Data In	t <sub>DPVKH</sub>												
	Write	t <sub>WVKH</sub>												
	Address Advance	t <sub>BAVKH</sub>												
	Chip Select	t <sub>SOVKH</sub>												
		t <sub>SIVKH</sub>												
Hold Times:	Address	t <sub>KHAX</sub>	2	—	2	—	2	—	2	—	2	—	ns	6
	Address Status	t <sub>KHTSX</sub>												
	Data In	t <sub>KHDX</sub>												
	Write	t <sub>KHWX</sub>												
	Address Advance	t <sub>KHBAX</sub>												
	Chip Select	t <sub>KHS0X</sub>												
		t <sub>KHS1X</sub>												

#### NOTES:

1. A read cycle is defined by  $\bar{W}$  high or  $\bar{TSP}$  low for the setup and hold times. A write cycle is defined by  $\bar{W}$  low and  $\bar{TSP}$  high for the setup and hold times.
2. All read and write cycle timings are referenced from K or  $\bar{G}$ .
3.  $\bar{G}$  is a don't care when W is sampled low.
4. Maximum access times are guaranteed for all possible MC68040 external bus cycles.
5. Transition is measured  $\pm 500\text{ mV}$  from steady-state voltage with load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t<sub>KHQZ</sub> max is less than t<sub>KHQX1</sub> min for a given device and from device to device.
6. This is a synchronous device. All addresses must meet the specified setup and hold times for **ALL** rising edges of clock (K) whenever  $\bar{TSP}$  or  $\bar{TSC}$  are low and the chip is selected. All other synchronous inputs must meet the specified setup and hold times for **ALL** rising edges of K when the chip is selected. Chip select must be true ( $\bar{S1}$  low and  $\bar{S0}$  high) at each rising edge of clock for the device (when  $\bar{TSP}$  or  $\bar{TSC}$  is low) to remain enabled. Timings for  $\bar{S1}$  and  $\bar{S0}$  are similar.

### AC TEST LOADS

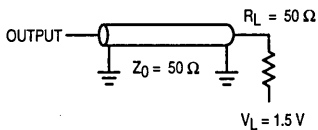


Figure 1A

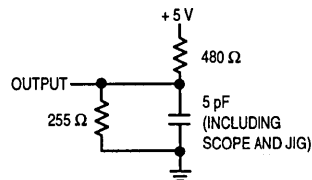
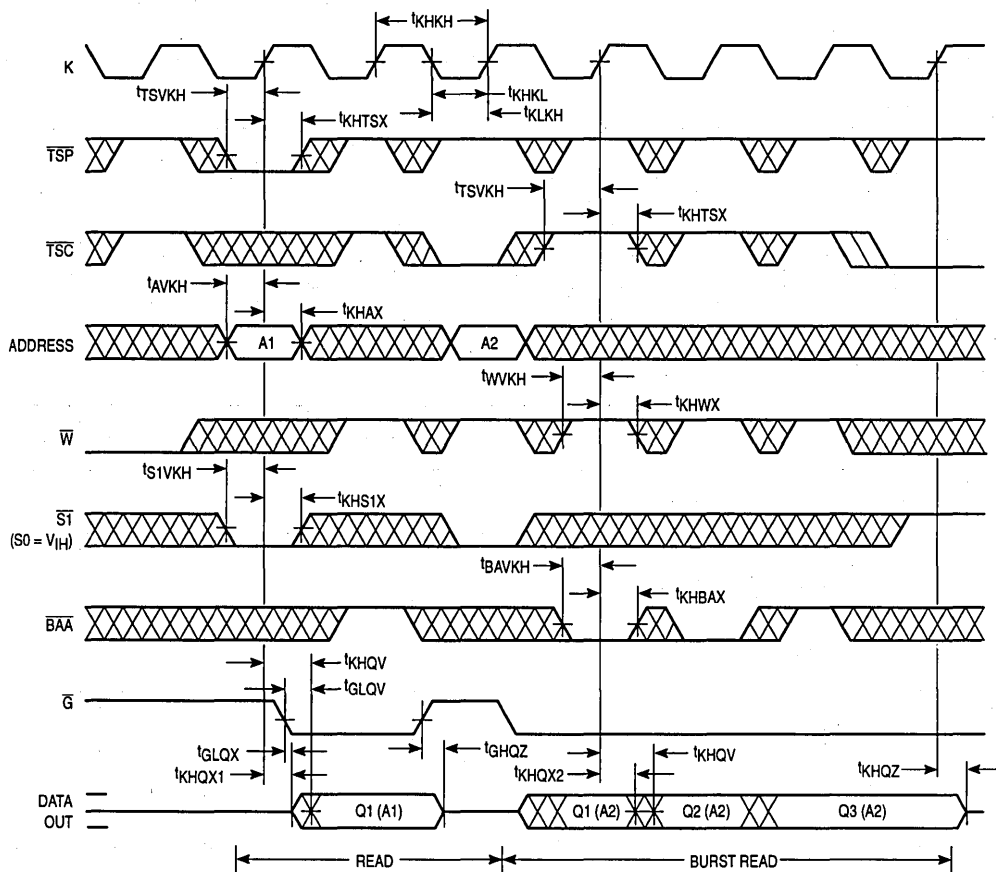


Figure 1B

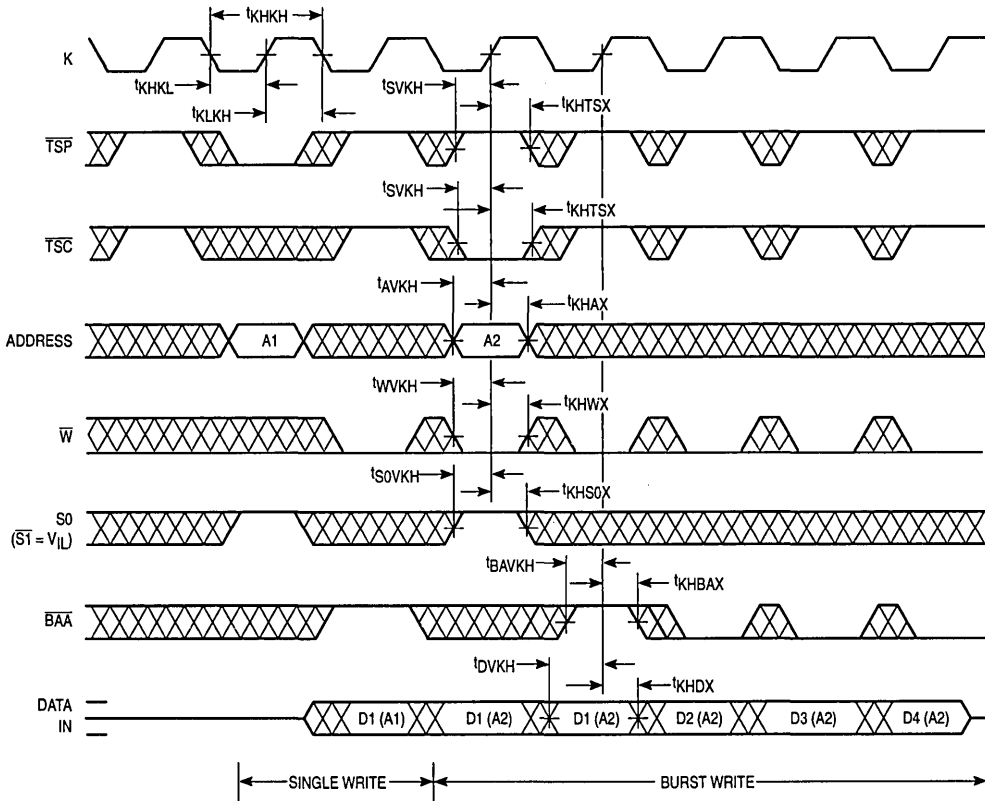
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### READ-WRITE CYCLE



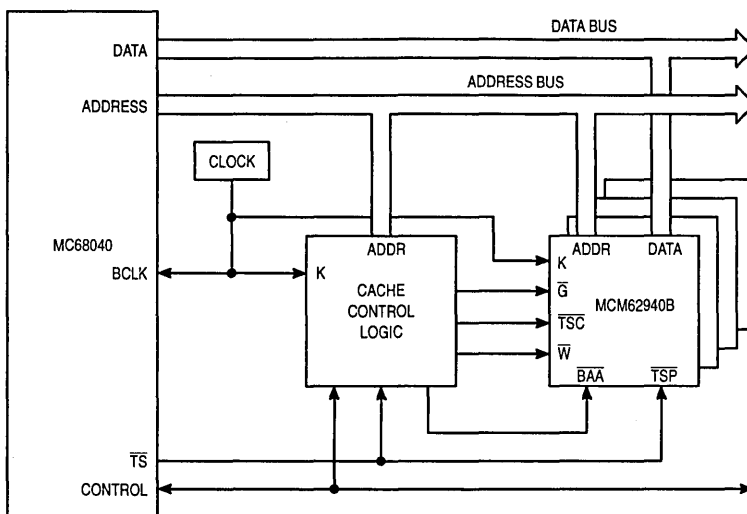
NOTE: Q1 (A2) represents the first output from the external address A2; Q2 (A2) represents the next output data in the burst sequence with A2 as the base address.

### WRITE CYCLE



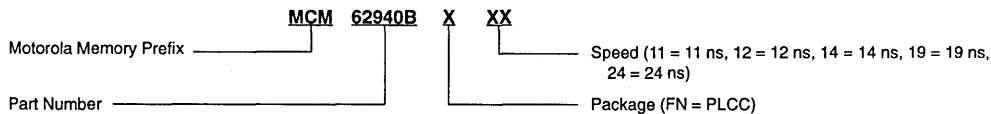
NOTE:  $\overline{G} = V_{IH}$ .

## APPLICATION EXAMPLE



128K Byte Burstable, Secondary Cache  
Using Four MCM62940BFN24s with a 33 MHz MC68040

## ORDERING INFORMATION (Order by Full Part Number)



Full Part Numbers — MCM62940BFN11 MCM62940BFN12 MCM62940BFN14 MCM62940BFN19 MCM62940BFN24