

CD4000UB, CD4001UB, CD4002UB, CD4025UB Types

CMOS NOR Gates

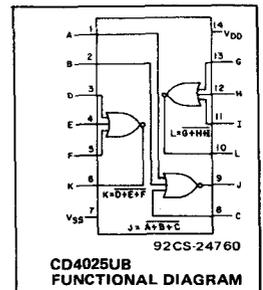
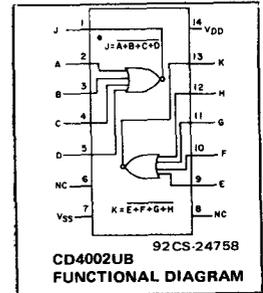
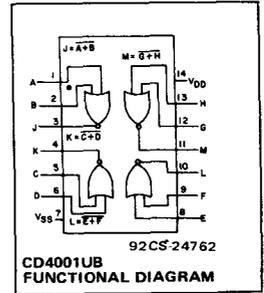
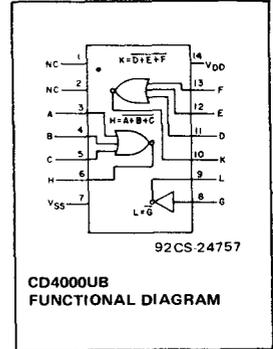
High-Voltage Types (20-Volt Rating)
Dual 3 Input
plus Inverter—CD4000UB
Quad 2 Input—CD4001UB
Dual 4 Input—CD4002UB
Triple 3 Input—CD4025UB

RCA-CD4000UB, CD4001UB, CD4002UB, and CD4025UB NOR gates provide the system designer with direct implementation of the NOR function and supplement the existing family of CMOS gates.

The CD4000UB, CD4001UB, CD4002UB, and CD4025UB types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic packages (E suffix), 14-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

- Propagation delay time = 30 ns (typ.) at $C_L = 50$ pF, $V_{DD} = 10$ V
- Standardized symmetrical output characteristics
- 100% tested for maximum quiescent current at 20 V
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"
- Maximum input current of $1 \mu\text{A}$ at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- 5-V, 10-V, and 15-V parametric ratings



STATIC ELECTRICAL CHARACTERISTICS

CHARACTER- ISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
	V_D (V)	V_{IN} (V)	V_{DD} (V)	Values at -55, +25, +125 Apply to D, F, K, H Packages Values at -40, +25, +85 Apply to E Package							
				-55	-40	+85	+125	+25			
				Min.	Typ.	Max.					
Quiescent Device Current, I_{DD} Max.	-	0.5	5	0.25	0.25	7.5	7.5	-	0.01	0.25	μA
	-	0.10	10	0.5	0.5	15	15	-	0.01	0.5	
	-	0.15	15	1	1	30	30	-	0.01	1	
	-	0.20	20	5	5	150	150	-	0.02	5	
Output Low (Sink) Current I_{OL} Min.	0.4	0.5	5	0.64	0.61	0.42	0.36	0.51	1	-	mA
	0.5	0.10	10	1.6	1.5	1.1	0.9	1.3	2.6	-	
	1.5	0.15	15	4.2	4	2.8	2.4	3.4	6.8	-	
Output High (Source) Current, I_{OH} Min.	4.6	0.5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	-	mA
	2.5	0.5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	-	
	9.5	0.10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	-	
	13.5	0.15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8	-	
Output Voltage: Low-Level, V_{OL} Max.	-	0.5	5	0.05			-	0	0.05	V	
	-	0.10	10	0.05			-	0	0.05		
	-	0.15	15	0.05			-	0	0.05		
Output Voltage: High-Level, V_{OH} Min.	-	0.5	5	4.95			4.95	5	-	V	
	-	0.10	10	9.95			9.95	10	-		
	-	0.15	15	14.95			14.95	15	-		
Input Low Voltage, V_{IL} Max.	0.5, 4.5	-	5	1			-	-	1	V	
	1, 9	-	10	2			-	-	2		
	1.5, 13.5	-	15	2.5			-	-	2.5		
Input High Voltage, V_{IH} Min.	0.5	-	5	4			4	-	-	V	
	1	-	10	8			8	-	-		
	1.5	-	15	12.5			12.5	-	-		
Input Current I_{IN} Max.	-	0.18	18	± 0.1	± 0.1	± 1	± 1	-	$\pm 10^{-5}$	± 0.1	μA

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RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range)	3	18	V

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD}) (Voltages referenced to V_{SS} Terminal)	-0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS	-0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT	± 10 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = -40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
For T_A = -55 to +100°C (PACKAGE TYPES D, F, K)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPES D, F, K, H	-55 to +125°C
PACKAGE TYPE E	-40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg})	-65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 \pm 1/32 inch (1.59 \pm 0.79 mm) from case for 10 s max.	+265°C

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ\text{C}$, Input $t_r, t_f = 20$ ns, and $C_L = 50$ pF, $R_L = 200$ K Ω

CHARACTERISTIC	TEST CONDITIONS	ALL TYPES LIMITS		UNITS	
		V_{DD} Volts	TYP.		MAX.
Propagation Delay Time, t_{PHL}, t_{PLH}		5	60	120	ns
		10	30	60	
		15	25	50	
Transition Time, t_{THL}, t_{TLH}		5	100	200	ns
		10	50	100	
		15	40	80	
Input Capacitance, C_{IN}	Any Input	10	15	pF	

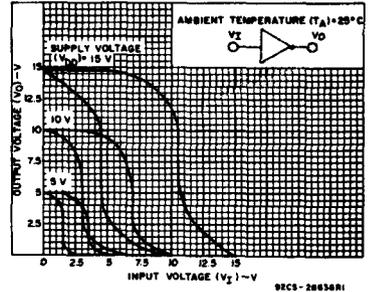


Fig. 1 - Minimum and maximum voltage transfer characteristics.

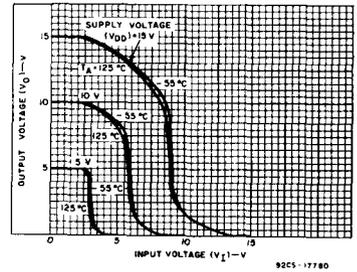


Fig. 2 - Typical voltage transfer characteristics as a function of temperature.

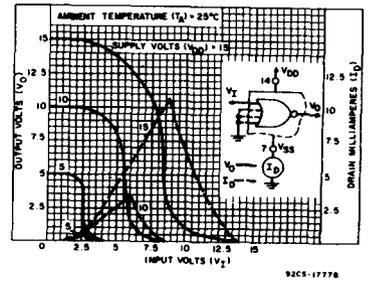


Fig. 3 - Typical current & voltage transfer characteristics.

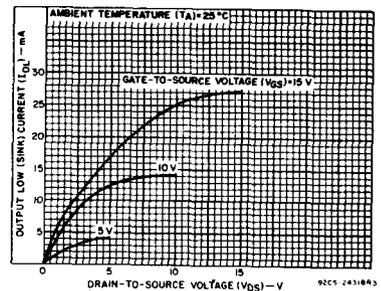


Fig. 5 - Typical output low (sink) current characteristics.

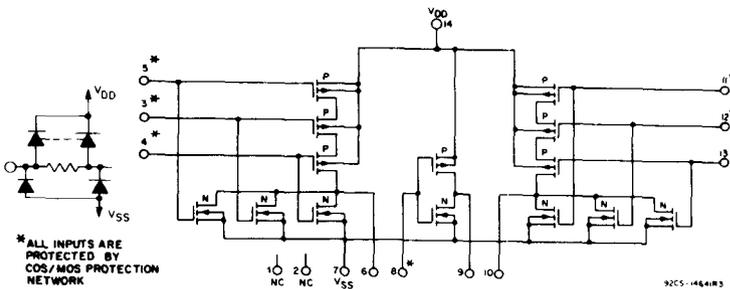


Fig. 4 - Schematic diagram for type CD4000UB.

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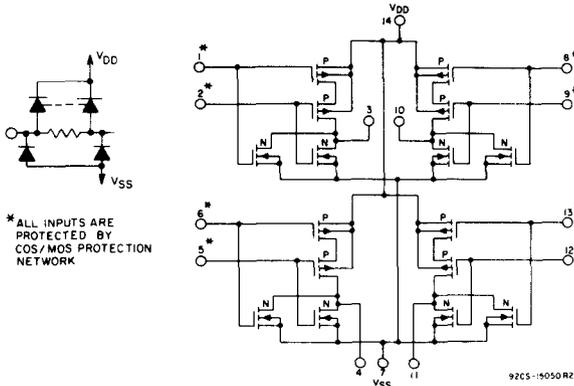


Fig. 6 - Schematic diagram for type CD4001UB.

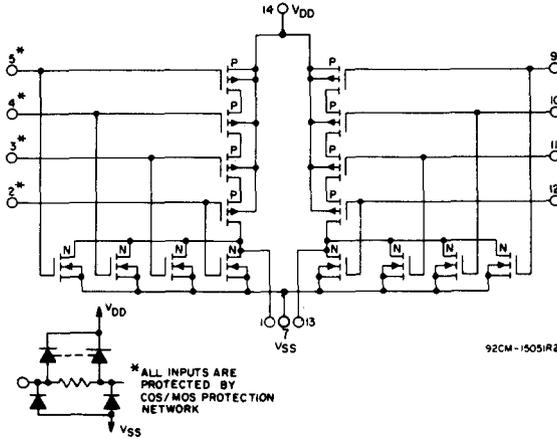


Fig. 7 - Schematic diagram for type CD4002UB.

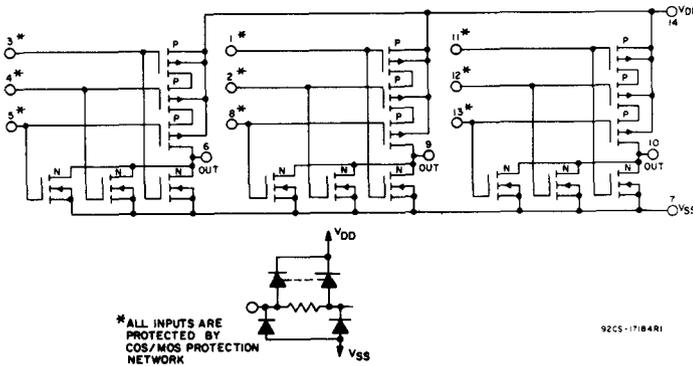


Fig. 8 - Schematic diagram for type CD4025UB.

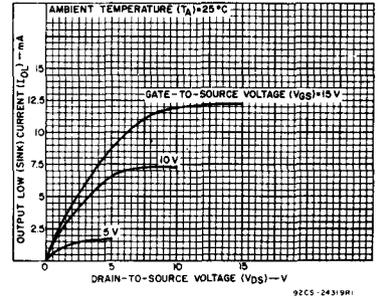


Fig. 9 - Minimum output low (sink) current characteristics.

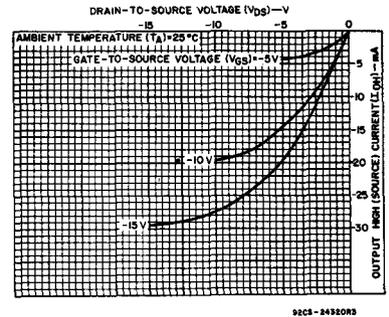


Fig. 10 - Typical output high (source) current characteristics.

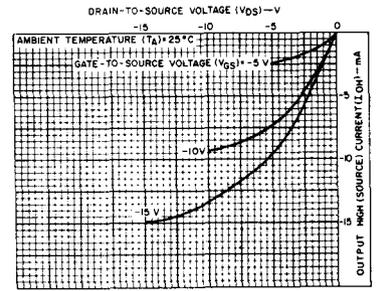


Fig. 11 - Minimum output high (source) current characteristics.

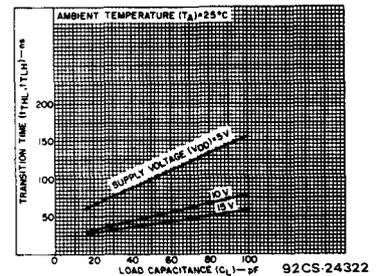


Fig. 12 - Typical transition time vs. load capacitance.

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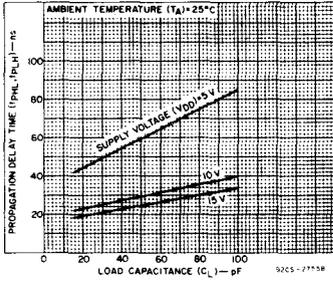


Fig. 13 - Typical propagation delay time vs. load capacitance.

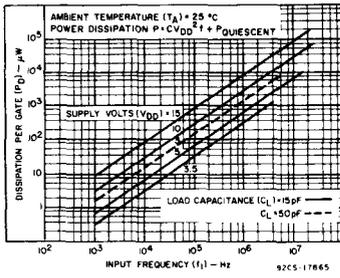


Fig. 14 - Typical power dissipation vs. frequency.

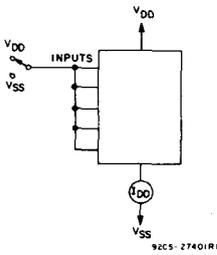


Fig. 15 - Quiescent device current test circuit.

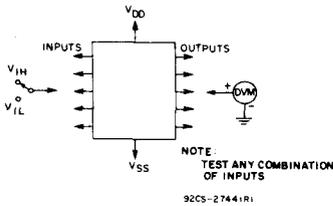


Fig. 16 - Input voltage test circuit.

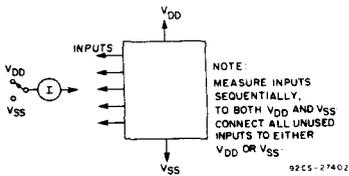
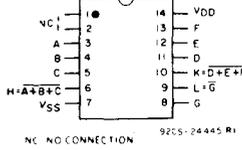
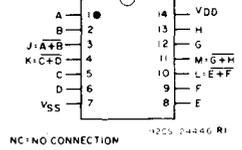


Fig. 17 - Input leakage current test circuit.

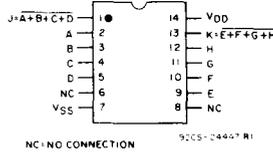
TERMINAL ASSIGNMENTS



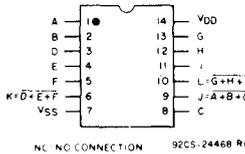
CD4000UB



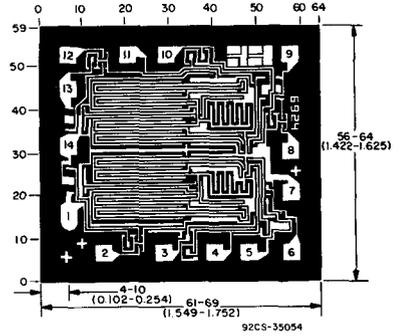
CD4001UB



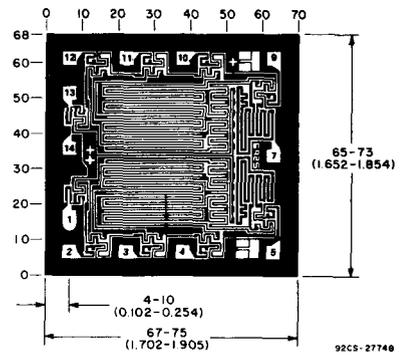
CD4002UB



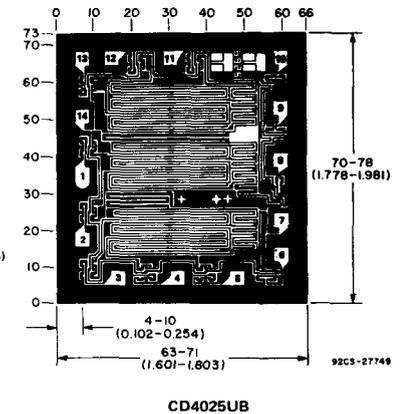
CD4025UB



CD4001UB

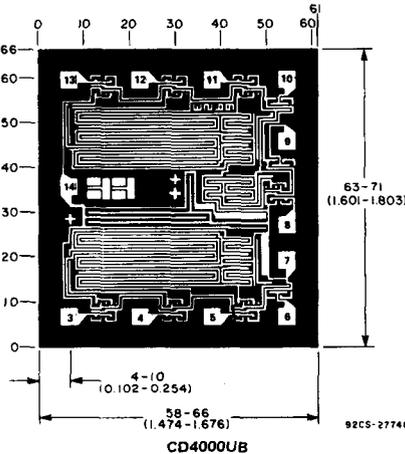


CD4002UB



CD4000UB

CHIP PHOTOGRAPHS Dimensions and Pad Layouts



CD4000UB

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each CMOS chip represent a chip when it is part of the wafer. When the wafer is separated into individual chips, the angle of cleavage may vary with respect to the chip face for different chips. The actual dimensions of the isolated chip, therefore, may differ slightly from the nominal dimensions shown. The user should consider a tolerance of ± 9 mils to ± 16 mils applicable to the nominal dimensions shown.