



4 GByte NANDrive SST85LD1004T

Fact Sheet

The SST85LD1004T NANDrive™ solid-state (SSD) drive combines a NAND controller and 4 GBytes of NAND flash in a multi-chip package. It provides complete ATA/IDE hard disk drive functionality in a small package for easy, space-saving mounting to a system motherboard. This makes the SST85LD1004T NANDrive SSD the ideal data storage solution for mobile and embedded electronic products that require smaller and more reliable storage.

Features

- **Industry Standard ATA/IDE Bus Interface**
 - Host Interface: 16-bit access
 - Supports up to PIO Mode-6
 - Supports up to Multi-word DMA Mode-4
 - Supports up to Ultra DMA Mode-4
- **Low Power, 3.3V Power Supply**
- **5.0V or 3.3V Host Interface Through V_{DDQ} Pins**
- **Low Current Operation:**
 - Active mode: 220 mA Maximum
 - Sleep mode: 120 μ A Typical
- **Power Management Unit**
 - Immediate disabling of unused circuitry without host intervention
 - Zero wake-up latency
- **Expanded Data Protection**
 - WP#/PD# pin configurable by firmware for prevention of data overwrites
 - Data security through user-selectable protection zones with advanced NAND management technology
- **20-byte Unique ID for Enhanced Security**
 - Factory Pre-programmed 10-byte Unique ID
 - User-Programmable 10-byte ID
- **Integrated Voltage Detector**
 - Prevents data loss due to unexpected power-down or brownout.
- **Endurance**
 - 100 Million write cycles with advanced NAND management technology
- **Data Retention**
 - 10 years
- **Pre-programmed Embedded Firmware**
 - Executes industry standard ATA/IDE commands
 - Implements advanced wear-leveling algorithms to substantially increase the longevity of flash media
 - Embedded Flash File System
- **Robust Built-in ECC**
- **Multi-tasking Technology Enables Fast Sustained Write Performance (Host-to-Flash)**
 - Up to 20 MByte/sec
- **Fast Sustained Read Performance (Flash-to-Host)**
 - Up to 20 MByte/sec
- **Industrial Temperature Range**
 - -40°C to +85°C for industrial operation
- **LBGA package**
 - 12mm x 24mm
- **All Devices are RoHS Compliant**



Product Description

The SST85LD1004T NANDrive™ solid-state drive (SSD) is a high-performance, fully-integrated, embedded flash solid state drive. It combines an integrated ATA Controller and 4GByte of NAND Flash in a multi-chip package. This product is ideal for solid state mass storage applications offering new and expanded functionality while enabling cost effective designs.

ATA-based solid state mass storage technology is widely used in portable and desktop computers, digital cameras, music players, handheld data collection scanners, cellular phones, PCS phones, PDAs, handy terminals, personal communicators, robotics, audio recorders, monitoring devices, and set-top boxes.

SST NANDrive is a single device, solid state drive designed for embedded ATA/IDE protocol systems and supports standard ATA/IDE protocol with up to PIO Mode-6, Multi-word DMA Mode-4 and Ultra DMA Mode-4 interface. The built in microcontroller and file management firmware communicates with ATA standard interfaces; thereby eliminating the need for additional or proprietary software such as Flash File System (FFS) and Memory Technology Driver (MTD) software.

The SST85LD1004T NANDrive provides complete IDE Hard Disk Drive functionality and compatibility in a 12mm x 24mm BGA package for easy, space saving mounting to a system motherboard. It is a perfect solution for portable, consumer electronic products requiring smaller and more reliable data storage.

The NANDrive provides a WP#/PD# pin to protect critical information stored in the flash media from unauthorized overwrites.

The NANDrive is pre-programmed with a 10-byte unique serial ID. For even greater system security, the user has the option of programming an additional 10 Bytes of ID space to create a unique, 20-byte ID.

NANDrive SSD is available with advanced NAND management technology, a NAND memory management technology that enhances data security, significantly improves endurance, and accurately predicts the minimum life span of NAND flash devices. Advanced NAND management technology combines NAND controller hardware error correction, advanced wear leveling algorithms, and bad block management to extend the life of the product.



General Description

Each NANDrive contains an integrated ATA Controller and one or more NAND Flash dice in a LBGA package. Refer to Figure 1 for the NANDrive block diagram.

Performance-optimized NANDrive

The heart of the NANDrive is the ATA Flash Disk Controller which translates standard ATA signals into flash media data and control signals. The following components contribute to the NANDrive's operation.

Microcontroller Unit (MCU)

The MCU translates ATA/IDE commands into data and control signals required for flash media operation.

Internal Direct Memory Access (DMA)

The NANDrive uses internal DMA allowing instant data transfer from buffer to flash media. This implementation eliminates microcontroller overhead associated with the traditional, firmware-based approach, thereby increasing the data transfer rate.

Power Management Unit (PMU)

The power management unit controls the power consumption of the NANDrive. The PMU dramatically reduces the power consumption of the NANDrive by putting the part of the circuitry that is not in operation into sleep mode.

The Flash File System handles inadvertent power interrupts and has auto-recovery capability to insure NANDrive firmware integrity. For regular power management, the Host must send an Idle_Immediate command and wait for command ready before powering down the NANDrive.

SRAM Buffer

A key contributor to the NANDrive performance is an SRAM buffer. The buffer optimizes the host's data transfer to and from the flash media.

Embedded Flash File System

The embedded flash file system is an integral part of the NANDrive. It contains MCU firmware that performs the following tasks:

1. Translates host side signals into flash media writes and reads.
2. Provides flash media wear leveling to spread the flash writes across all memory address space to increase the longevity of flash media.
3. Keeps track of data file structures.

Error Correction Code (ECC)

High performance is achieved through optimized hardware error detection and correction.

Serial Communication Interface (SCI)

The Serial Communication Interface (SCI) is designed for manufacturing error reporting. Always provide access to the SCI interface in the PCB design to aid in design validation.



Multi-tasking Interface

The multi-tasking interface enables fast, sustained write performance by allowing concurrent Read, Program, and Erase operations to multiple flash media devices.

Advanced NAND Management Technology

Advanced NAND management technology balances the wear on erased blocks with an advanced wear-leveling scheme which provides a minimum of 100 million product write cycles. Advanced NAND management technology tracks the number of program/erase cycles within a group. When the host updates data, higher priority is given to the less frequently written erase blocks; thereby, evenly distributing host writes within a wear-leveling group.

Advanced NAND management technology enhances NANDrive security with password protection and four independent protection zones which can be set to Read-only or Hidden.

Functional Blocks

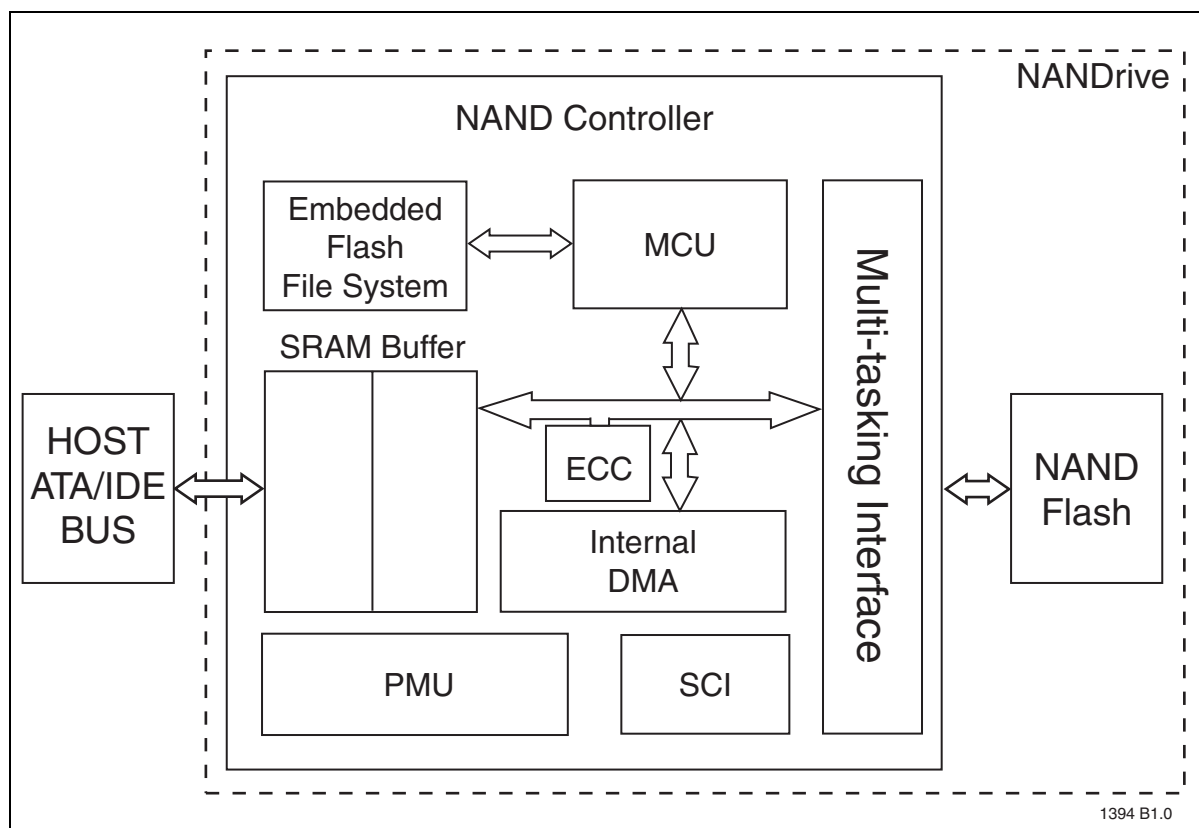


Figure 1: NANDrive Block Diagram



Pin Assignments

The signal/pin assignments are listed in Figure 2. Low active signals have a “#” suffix. Pin types are Input, Output, or Input/Output. Signals whose source is the host are designated as inputs while signals that the NANDrive sources are outputs.

The NANDrive functions in ATA mode, which is compatible with IDE hard disk drives.

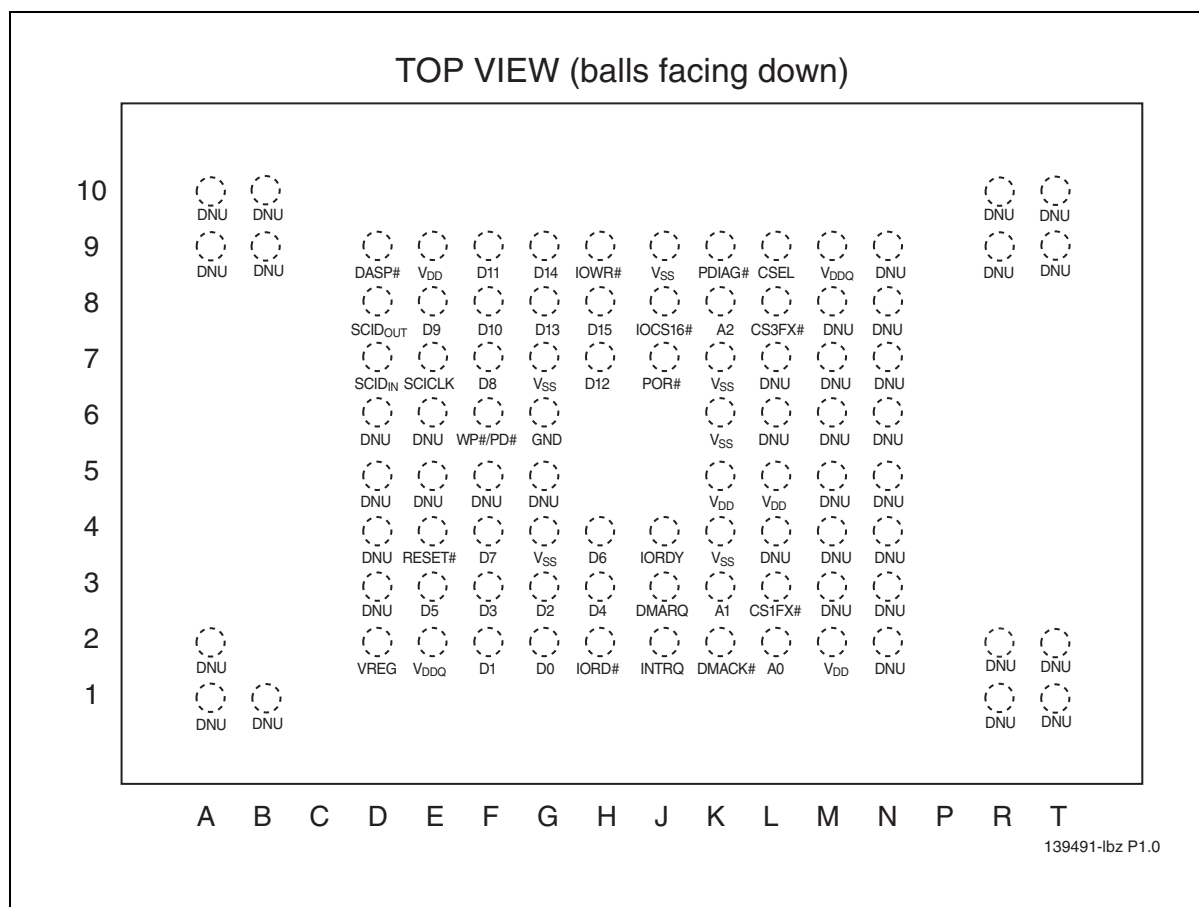


Figure 2: Pin Assignments for 91-Ball LBGA



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Table 1: Pin Assignments (1 of 3)

Symbol	Pin No. 91-LBGA	Pin Type	I/O Type	Name and Functions
Host Side Interface				
A2	K8	I	I1Z	A[2:0] are used to select one of eight registers in the Task File.
A1	K3			
A0	L2			
D15	H8	I/O	I1Z/O2	D[15:0] Data bus
D14	G9			
D13	G8			
D12	H7			
D11	F9			
D10	F8			
D9	E8			
D8	F7			
D7	F4			
D6	H4			
D5	E3			
D4	H3			
D3	F3			
D2	G3			
D1	F2			
D0	G2			
DMACK#	K2	I	I2U	DMA Acknowledge - input from host
DMARQ	J3	O	O1	DMA Request to host
CS1FX#	L3	I	I2Z	CS1FX# is the chip select for the task file registers
CS3FX#	L8			CS3FX# is used to select the alternate status register and the Device Control register.
CSEL	L9	I	I1U	This internally pulled-up signal is used to configure this device as a Master or a Slave. When this pin is grounded, this device is configured as a Master. When the pin is open, this device is configured as a Slave. The pin setting should remain the same from Power-on to Power-down.
IORD#	H2	I	I2Z	IORD#: This is an I/O Read Strobe generated by the host. When Ultra DMA mode is not active, this signal gates I/O data from the device.
				HDMARDY#: In Ultra DMA mode when DMA Read is active, this signal is asserted by the host to indicate that the host is ready to receive Ultra DMA data-in bursts. The host may negate HDMARDY# to pause an Ultra DMA transfer.
				HSTROBE: When DMA Write is active, this signal is the data-out strobe generated by the host. Both the rising and falling edges of HSTROBE cause data to be latched by the device. The host may stop generating HSTROBE edges to pause an Ultra DMA data-out burst.



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Table 1: Pin Assignments (Continued) (2 of 3)

Symbol	Pin No. 91-LBGA	Pin Type	I/O Type	Name and Functions
IOWR#	H9	I	I2Z	IOWR#: This is an I/O Write Strobe generated by the host. When Ultra DMA mode is not active, this signal is used to clock I/O data into the device. STOP: When Ultra DMA mode protocol is active, the assertion of this signal causes the termination of the Ultra DMA burst
IORDY	J4	O	I2Z	IORDY: When Ultra DMA mode DMA Write is not active and the device is not ready to respond to a data transfer request, this signal is negated to extend the Host transfer cycle. However, it is never negated by this controller. DDMARDY#: When Ultra DMA mode DMA Write is active, this signal is asserted by the host to indicate that the device is ready to receive Ultra DMA data-in bursts. The device may negate DDMARDY# to pause an Ultra DMA transfer. DSTROBE: When Ultra DMA mode DMA Read is active, this signal is the data-out strobe generated by the device. Both the rising and falling edges of DSTROBE cause data to be latched by the host. The device may stop generating DSTROBE edges to pause an Ultra DMA data-out burst.
IOCS16#	J8	O	O2	This output signal is asserted low when the device is indicating a word data transfer cycle.
INTRQ	J2	O	O1	This signal is the active high Interrupt Request to the host.
PDIAG#	K9	I/O	I1U/O1	The Pass Diagnostic signal in the Master/Slave handshake protocol.
DASP#	D9	I/O	I1U/O6	The Drive Active/Slave Present signal in the Master/Slave handshake protocol.
RESET#	E4	I	I2U	This input pin is the active low hardware reset from the host.
WP#/PD#	F6	I	I3U	The WP#/PD# pin can be used for either the Write Protect mode or Power-down mode, but only one mode is active at any time. The Write Protect or Power-down modes can be selected through the host command. The Write Protect mode is the factory default setting.
Serial Communication Interface (SCI)				
SCID _{OUT}	D8	O	O4	SCI interface data output
SCID _{IN}	D7	I	I3U	SCI interface data input
SCICLK	E7	I	I3U	SCI interface clock
Miscellaneous				
V _{SS}	G4, G6, G7, K4, K6, K7, J9	PWR		Ground
V _{DD}	E9, K5, L5, M2	PWR		V _{DD} (3.3V)
V _{DDQ}	E2, M9	PWR		V _{DDQ} (5V/3.3V) for Host interface
POR#	J7	I	Analog Input ¹	Power-on Reset (POR). Active Low
V _{REG}	D2	O		External capacitor pin



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Table 1: Pin Assignments (Continued) (3 of 3)

Symbol	Pin No.	Pin Type	I/O Type	Name and Functions
	91-LBGA			
DNU	A1, A2, A9, A10, B1, B9, B10, D3, D4, D5, D6, E5, E6, F5, G5, L4, L6, L7, M3, M4, M5, M6, M7, M8, N2, N3, N4, N5, N6, N7, N8, N9, R1, R2, R9, R10, T1, T2, T9, T10			Do not use.

T1.4 1394(01)

1. Analog input for supply voltage detection



Capacity Specification

Table 2 shows the default capacity and specific settings for heads, sectors, and cylinders. Users can change the default settings in the drive ID table using the Identity-Drive command. If the total number of bytes is less than the default, the remaining space could be used as spares to increase the flash drive endurance. It should also be noted that if the total flash drive capacity exceeds the total default number of bytes, the flash drive endurance will be reduced.

Table 2: Default NANDrive Settings

Capacity	Total Bytes	Cylinders	Heads	Sectors	Max LBA
4 GByte	4,096,253,952	7937	16	63	8,000,496

T2.6 1394(01)

Table 3: Sustained Performance

Write Performance	Read Performance
Up to 20 MByte/sec	Up to 20 MByte/sec

T3.6 1394(01)

Table 4: Supported ATA Modes

PIO	MWDMA	UltraDMA
Up to Mode-6	Up to Mode-4	Up to Mode-4

T4.1394(01)

Table 5: Advanced NAND Management Technology Write Cycles

Write Cycles per Group	No. of Groups per Product	Wear-leveling Group Size	Cluster Size ¹
100M	4	1 GByte	16 KByte

T5.1394(01)

1. Optimized host cluster size setting.



Configurable Write Protect/Power-down Modes

The WP#/PD# pin can be used for either Write Protect mode or Power-down mode, but only one mode is active at any time. Either mode can be selected through the host command, Set-WP#/PD#-Mode.

Once the mode is set with this command, the device will stay in the configured mode until the next time this command is issued. Power-off or reset will not change the configured mode.

Write Protect Mode

When the device is configured in the Write Protect mode, the WP#/PD# pin offers extended data protection. This feature can be either selected through a jumper or host logic to protect the stored data from inadvertent system writes or erases, and viruses. The Write Protect feature protects the full address space of the data stored on the flash media.

In the Write Protect mode, the WP#/PD# pin should be asserted prior to issuing the destructive commands: Erase-Sector, Format-Track, Write-DMA, Write-Multiple, Write-Multiple-without-Erase, Write-Sector(s), Write-Sector-without-Erase, or Write-Verify. This will force the NANDrive to reject any destructive commands from the ATA interface. All destructive commands will return 51H in the Status register and 04H in the Error register signifying an invalid command. All non-destructive commands will be executed normally.

Power-down Mode

When the device is configured in the Power-down mode, if the WP#/PD# pin is asserted during a command, the NANDrive completes the current command and returns to the standby mode immediately to save power. Afterwards, the device will not accept any other commands. Only a Power-on Reset (POR) or hardware reset will bring the device to normal operation with the WP#/PD# pin de-asserted.

Power-on Initialization

NANDrive is self-initialized during the first power-up. As soon as the power is applied to the NANDrive it reports busy for typically up to five seconds while performing bad blocks search and low level format. This initialization is a one time event.

During the first self-initialization, the NANDrive firmware scans all connected flash media devices and reads their device ID. If the device ID matches the listed flash media devices, the NANDrive performs drive recognition based on the algorithm provided by the flash media suppliers, including setting up the bad block table, executing all the necessary handshaking routines for flash media support, and, finally, performing the low-level format.

If the drive initialization fails, and a visual inspection is unable to determine the problem, SST provides a comprehensive interface for manufacturing flow debug. This interface not only allows debug of the failure and manual reset of the initialization process, but also allows customization of user definable options.

ATA/IDE Interface

The ATA interface can be used for NANDrive manufacturing support. SST provides an example of a DOS-based solution (an executable routine) for manufacturing debug and rework.



Serial Communication Interface (SCI)

For additional manufacturing flexibility, the SCI bus can be used for manufacturing error reporting. The SCI consists of 3 active signals: SCIDOUT, SCIDIN, and SCICLK. Always provide access to the SCI interface in the PCB design to aid in design validation.

Lifetime Expectancy

NANDrive with advanced NAND management technology significantly extends the life of a product with its extensive ECC, advanced wear-leveling, and data scan and Refresh (DSR) algorithms. Each NANDrive device is partitioned into four wear-leveling groups. See Table 5 for the group size of each product.

Each NANDrive wear-leveling group can receive at least 100 million write cycles from the host. With four wear-leveling groups in each product, 400 million write cycles per product is possible when host writes are evenly distributed across groups.

For applications where data security is essential, NANDrive with advanced NAND management technology offers two additional protection features—protection zones and password protections.

Protection zones - Up to four independent protection zones can be enabled as either Read-only or Hidden (Read/Write protected). If the zones are not enabled, the data is unprotected (default configuration).

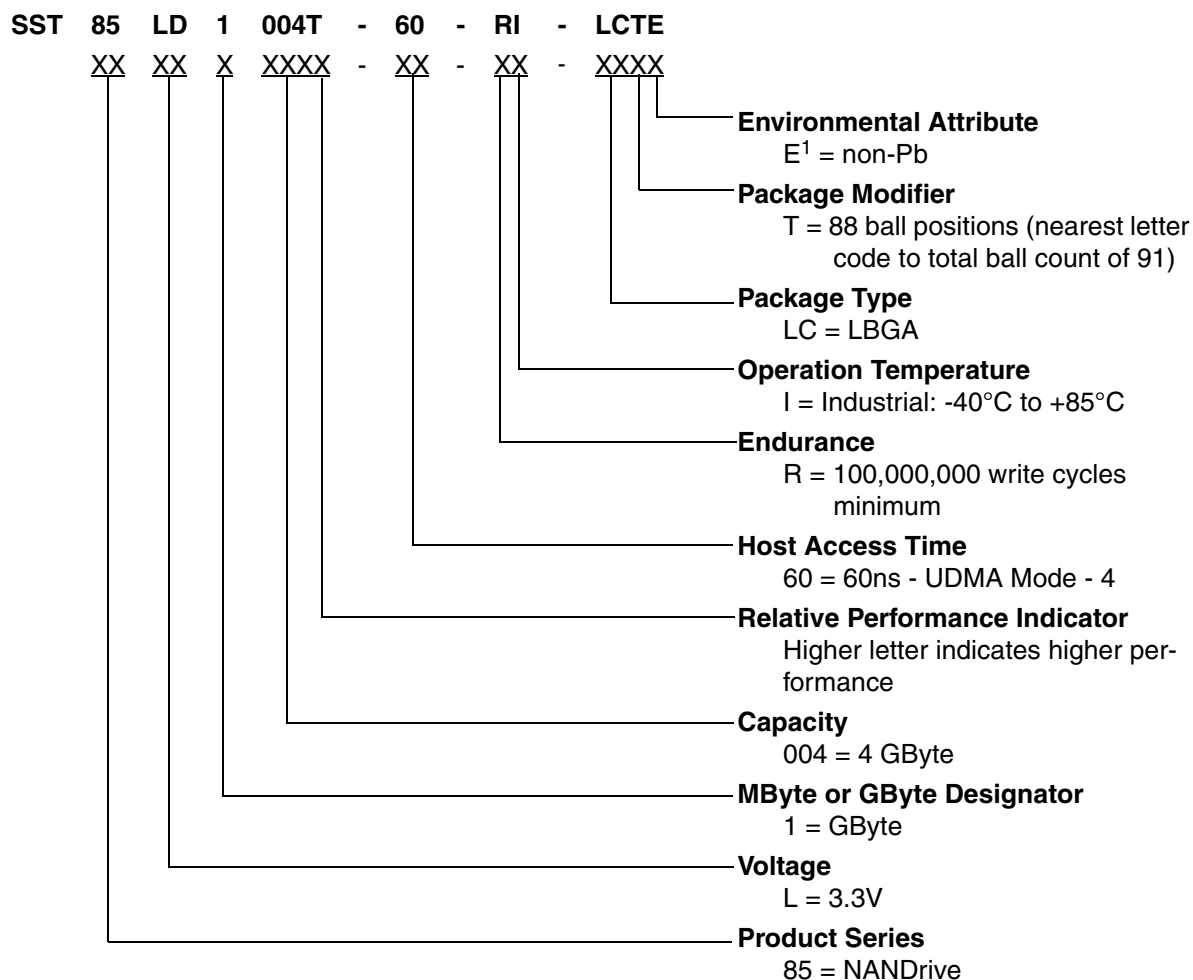
Password Protection - Requires a customer-unique password to access information within the protected zones.



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Product Ordering Information



1. Environmental suffix "E" denotes non-Pb solder. SST non-Pb solder devices are "RoHS Compliant".

Valid Combinations

SST85LD1004T-60-RI-LCTE

Note: Valid combinations are those products in mass production or will be in mass production. Consult your SST sales representative to confirm availability of valid combinations and to determine availability of new combinations.



Packaging Diagram

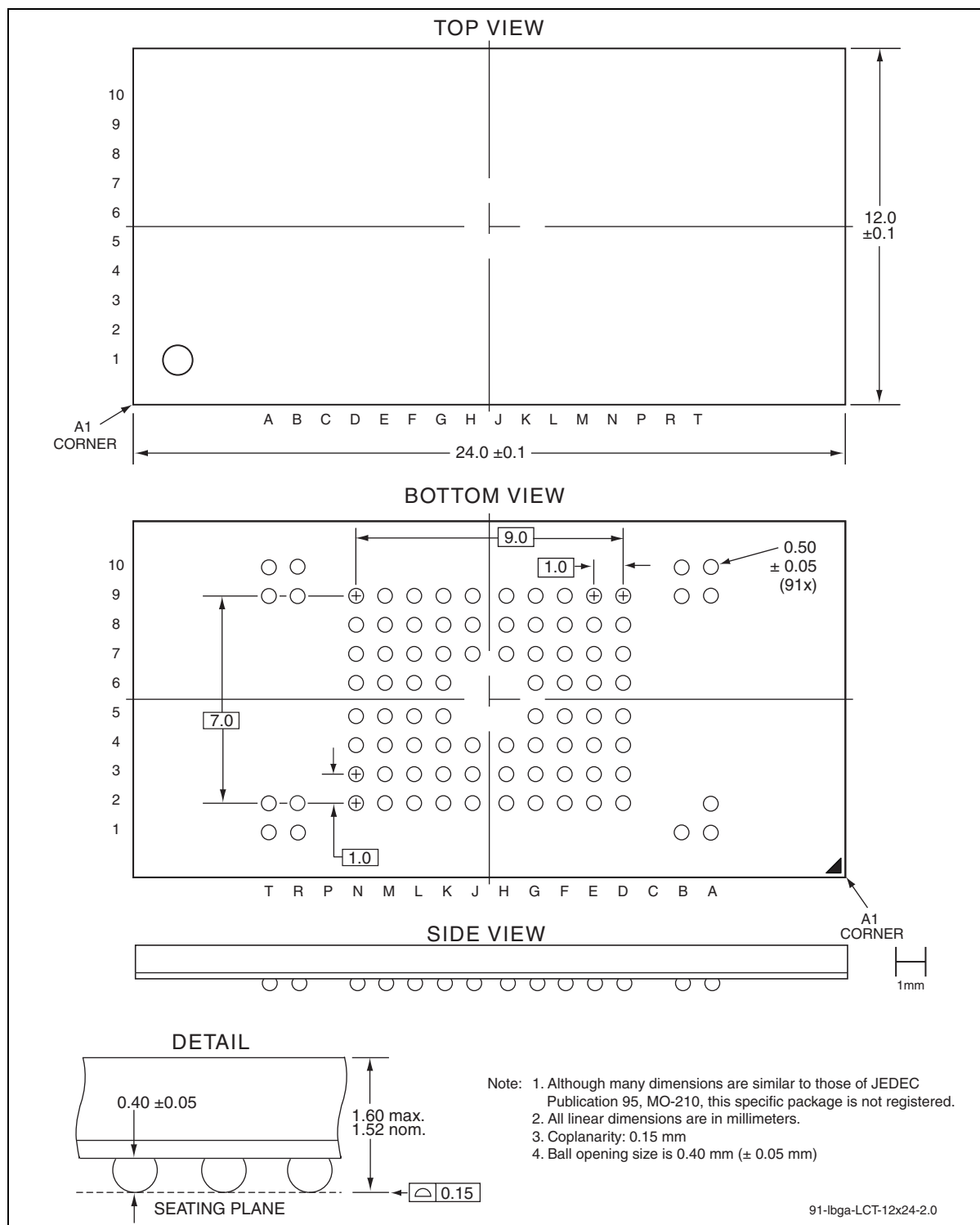


Figure 3: mini-NANDrive 91-Ball Low Profile Ball Grid Array (LBGA)
SST Package Code: LCT



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Table 6: Revision History

Number	Description	Date
00	• Initial release of Fact Sheet for SST85LD1004T	Sep 2008
01	• Updated "Product Ordering Information" on page 12 and Figure 3 to change the package code from LBT to LCT.	Feb 2009
02	• Applied new document format	Oct 2009

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Memory sizes denote raw storage capacity; actual usable capacity may be less.

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