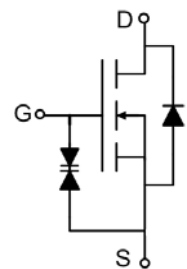


Main Product Characteristics:

V_{DS}	900V
$R_{DS(on)}$	1.2 Ω (typ.)
I_D	9A


TO-247

Marking and pin Assignment

Schematic diagram
Features and Benefits:

- Advanced MOSFET process technology
- Special designed for PWM, load switching and general purpose applications
- Ultra low on-resistance with low gate charge
- Fast switching and reverse body recovery
- 150°C operating temperature
- ESD Rating(HBM) :4KV


Description:

It utilizes the latest processing techniques to achieve the high cell density and reduces the on-resistance with high repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in power switching application and a wide variety of other applications.

Absolute max Rating:

Symbol	Parameter	Max.	Units
I_D @ TC = 25°C	Continuous Drain Current, V_{GS} @ 10V①	9	A
I_D @ TC = 100°C	Continuous Drain Current, V_{GS} @ 10V①	5.8	
I_{DM}	Pulsed Drain Current②	36	
P_D @TC = 25°C	Power Dissipation③	160	W
	Linear Derating Factor	1.3	W/°C
V_{DS}	Drain-Source Voltage	900	V
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy @ L=25mH	500	mJ
I_{AS}	Avalanche Current @ L=25mH	6.4	A
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	°C

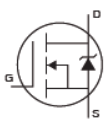
Thermal Resistance

Symbol	Characterizes	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-case ^③	—	0.78	°C/W
$R_{\theta JA}$	Junction-to-ambient ($t \leq 10s$) ^④	—	50	°C/W

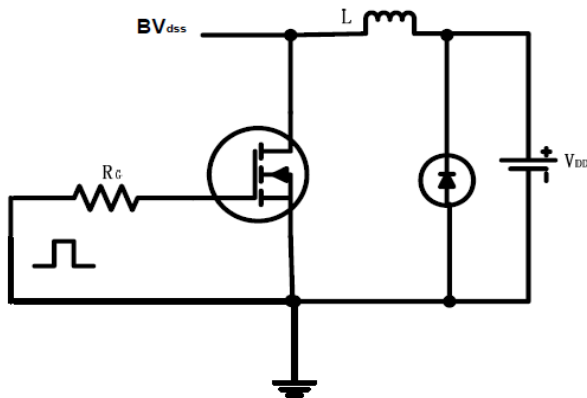
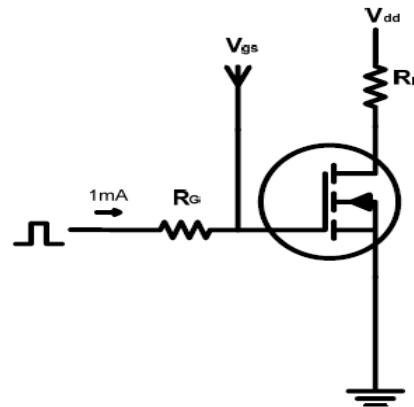
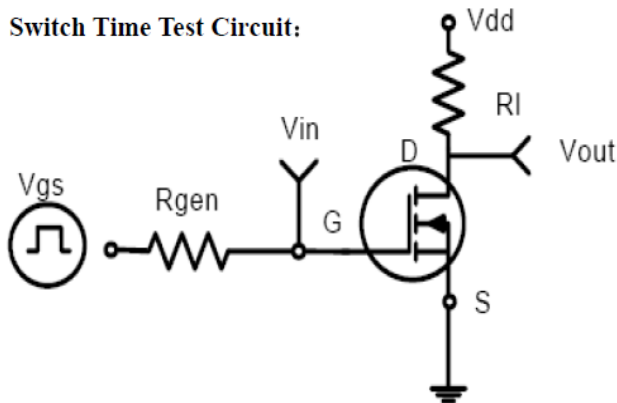
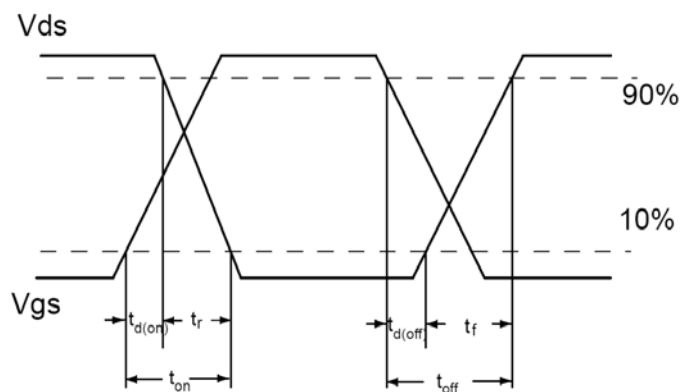
Electrical Characterizes @ $T_A=25^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source breakdown voltage	900	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$R_{DS(on)}$	Static Drain-to-Source on-resistance	—	1.2	1.4	Ω	$V_{GS}=10V, I_D = 3.5A$
$V_{GS(th)}$	Gate threshold voltage	2	—	4	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
I_{DSS}	Drain-to-Source leakage current	—	—	1	μA	$V_{DS} = 900V, V_{GS} = 0V$
		—	—	50		$T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source forward leakage	—	—	10	μA	$V_{GS} = 20V$
		—	—	-10		$V_{GS} = -20V$
g_{fs}	Forward Transconductance	—	10	—	S	$V_{DS} > 2I_D \cdot R_{DS(on).max.}$ $I_D = 9A$
Q_g	Total gate charge	—	47	—	nC	$I_D = 9A,$ $V_{DS} = 400V,$ $V_{GS} = 10V$
Q_{gs}	Gate-to-Source charge	—	10	—		
Q_{gd}	Gate-to-Drain("Miller") charge	—	17	—		
$t_{d(on)}$	Turn-on delay time	—	16	—	ns	$V_{GS}=10V, V_{DS}=450V,$ $R_{GEN}=4.7\Omega$ $I_D=4A$
t_r	Rise time	—	10	—		
$t_{d(off)}$	Turn-Off delay time	—	50	—		
t_f	Fall time	—	23	—		
C_{iss}	Input capacitance	—	2100	—	pF	$V_{GS} = 0V$ $V_{DS} = 25V$ $f = 1MHz$
C_{oss}	Output capacitance	—	152	—		
C_{rss}	Reverse transfer capacitance	—	12	—		

Source-Drain Ratings and Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	9	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode)	—	—	36	A	
V_{SD}	Diode Forward Voltage	—	—	1.5	V	$I_S=9A, V_{GS}=0V$
t_{rr}	Reverse Recovery Time	—	305	—	ns	$T_J = 25^\circ\text{C}, I_F = 9A, di/dt = 100A/\mu s$
Q_{rr}	Reverse Recovery Charge	—	2200	—	nC	

Test circuits and Waveforms

EAS test circuits:

Gate charge test circuit:

Switch Time Test Circuit:

Switch Waveforms:


Notes:

- ①The maximum current rating is limited by bond-wires.
- ②Repetitive rating; pulse width limited by max. junction temperature.
- ③The power dissipation PD is based on max. junction temperature, using junction-to-case thermal resistance.
- ④The value of $R_{\theta JA}$ is measured with the device mounted on 1in 2 FR-4 board with 2oz. Copper, in a still air environment with $T_A = 25^\circ\text{C}$

Typical electrical and thermal characteristics

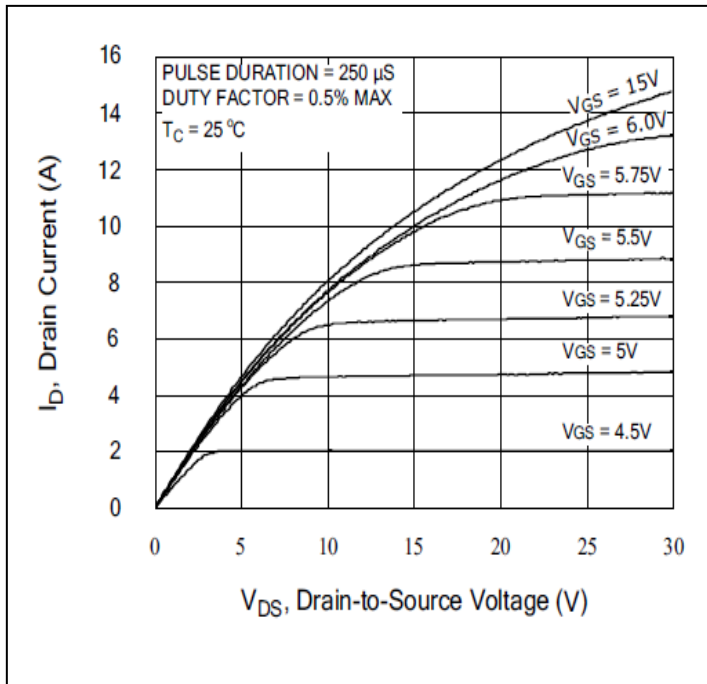


Figure 1: Typical Output Characteristics

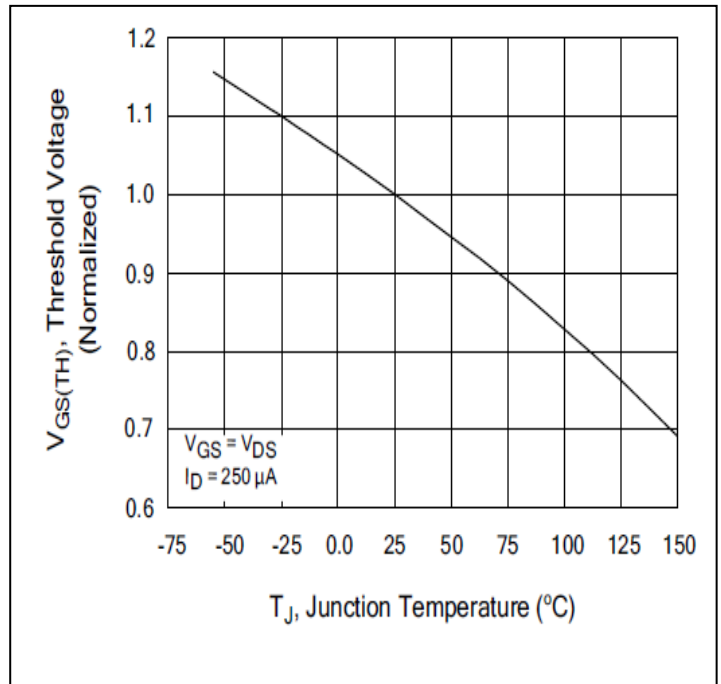


Figure 2: Gate to source cut-off voltage

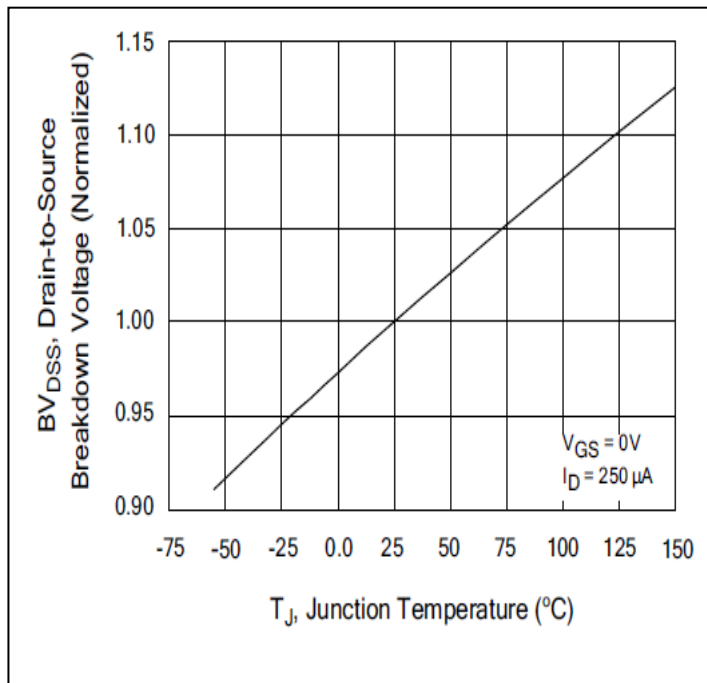


Figure 3: Drain-to-Source Breakdown Voltage Vs. Case Temperature

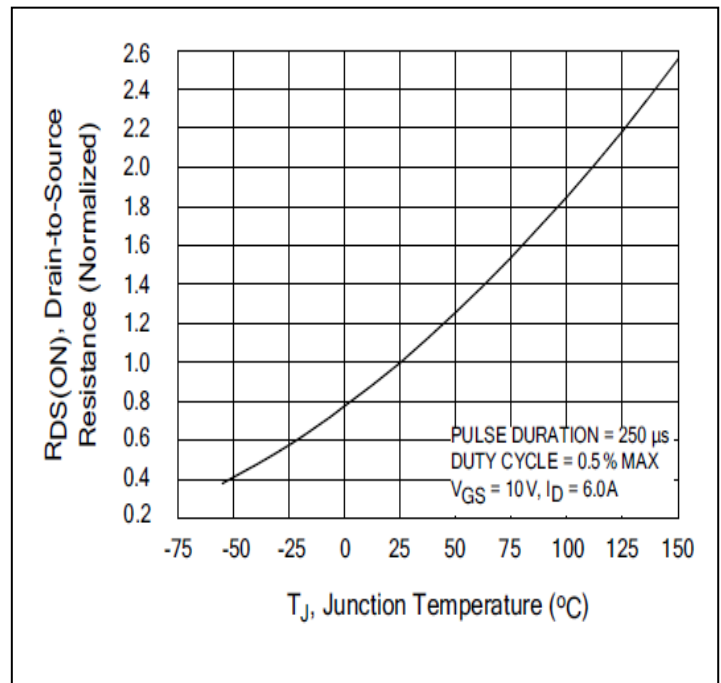


Figure 4: Normalized On-Resistance Vs. Case Temperature

Typical electrical and thermal characteristics

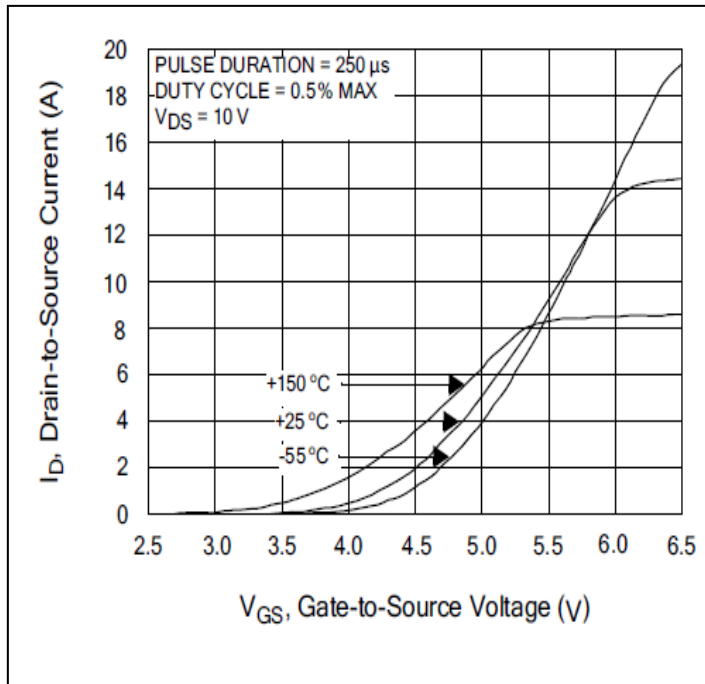


Figure 5: Typical Transfer Characteristics

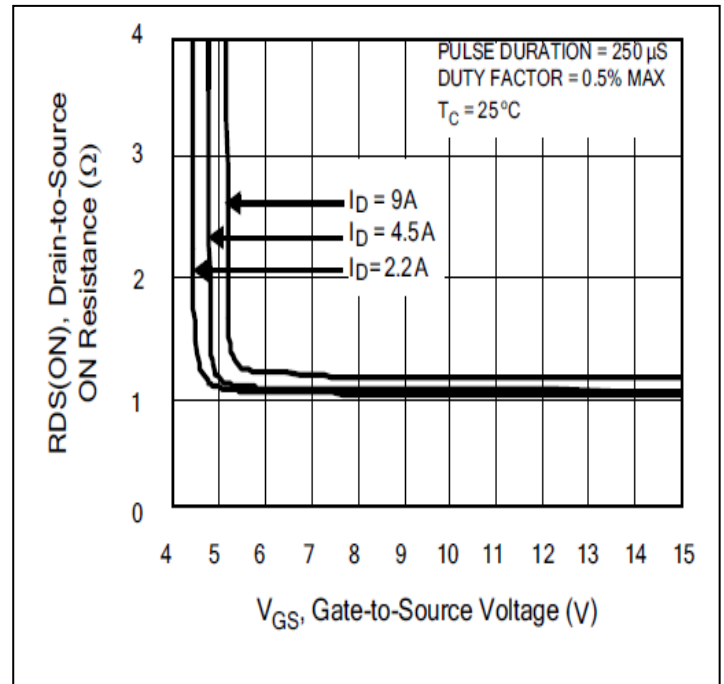


Figure 6. On-Resistance Vs. Gate Voltage and Drain Current

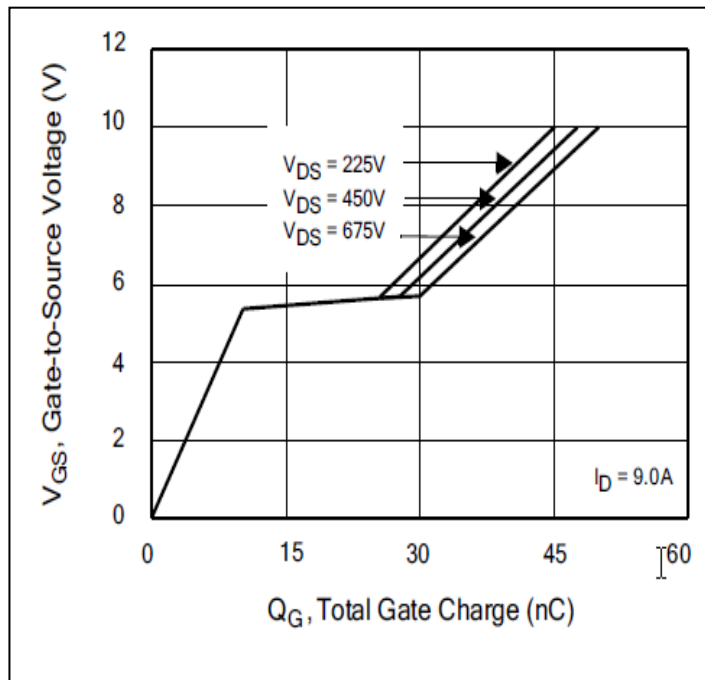


Figure 7. Gate Charge Vs. Drain-to-Source Voltage

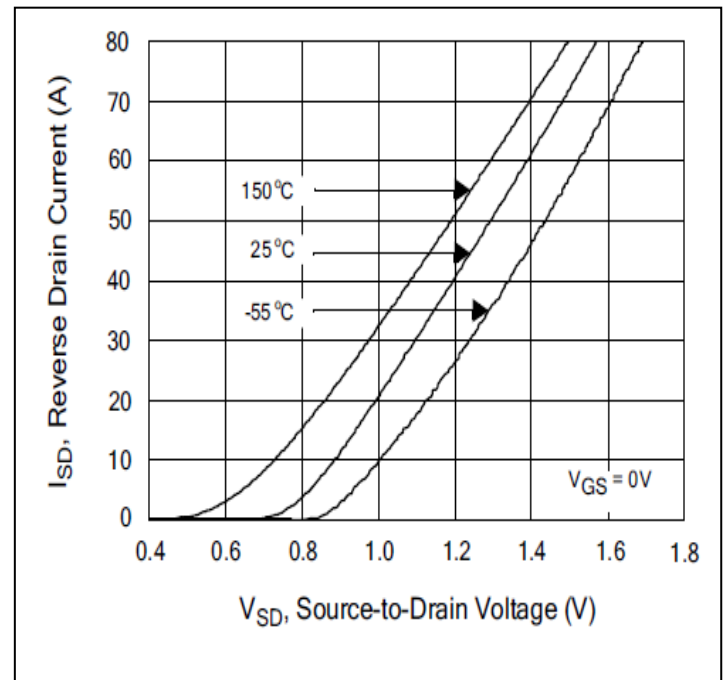


Figure 8: Typical Body Diode Transfer Characteristics

Typical electrical and thermal characteristics

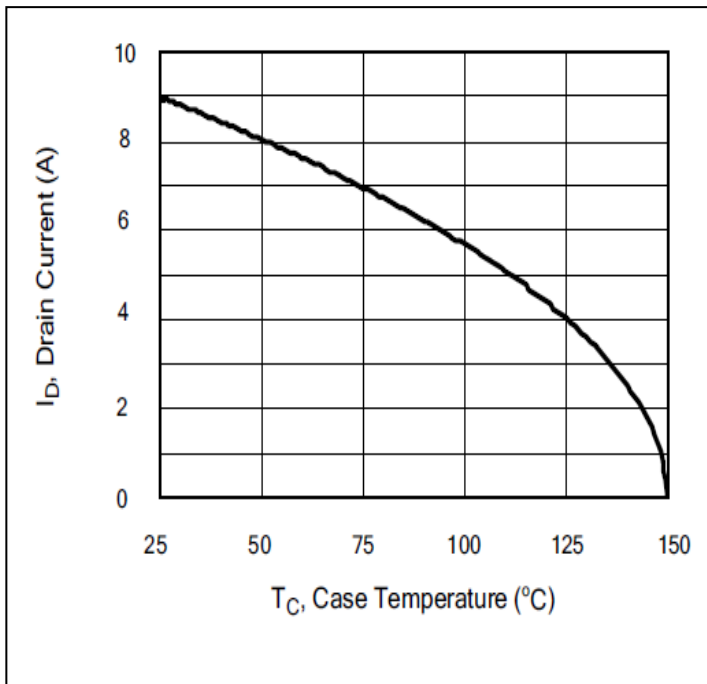


Figure 9. Maximum Drain Current Vs. Case Temperature

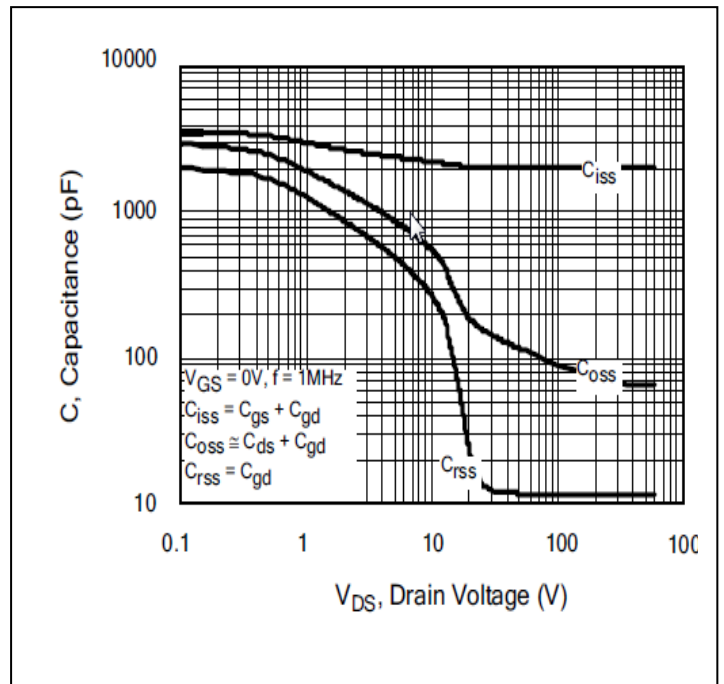


Figure 10. Typical Capacitance Vs. Drain-to-Source Voltage

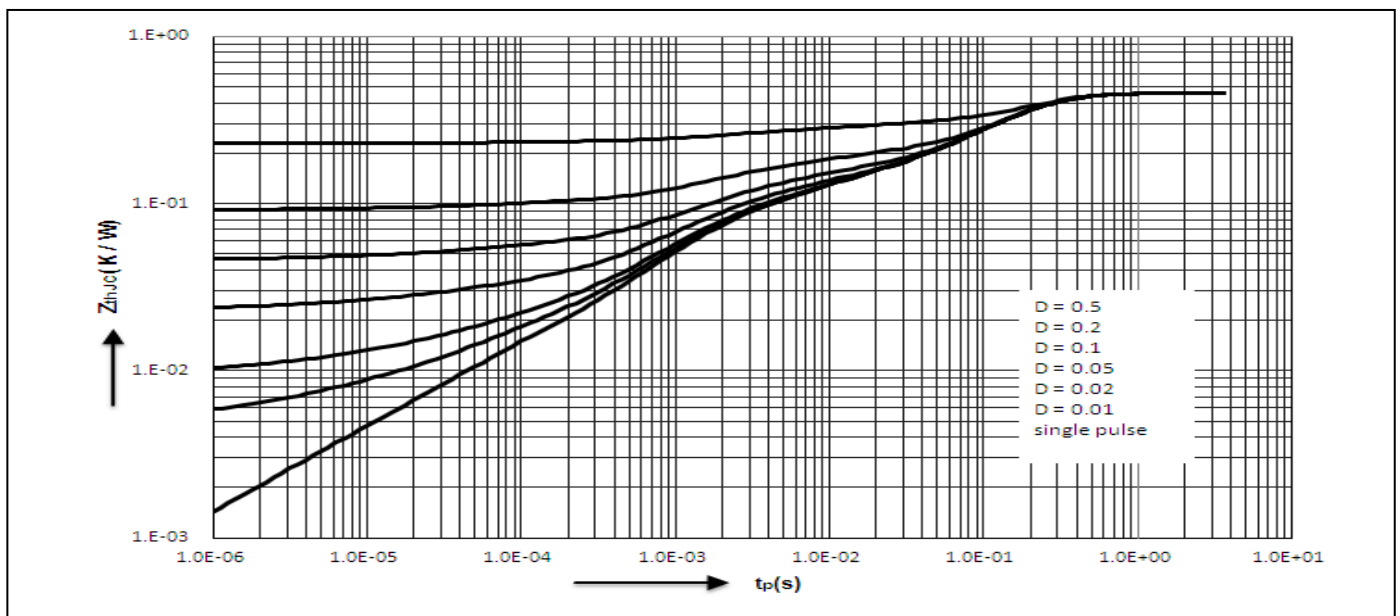
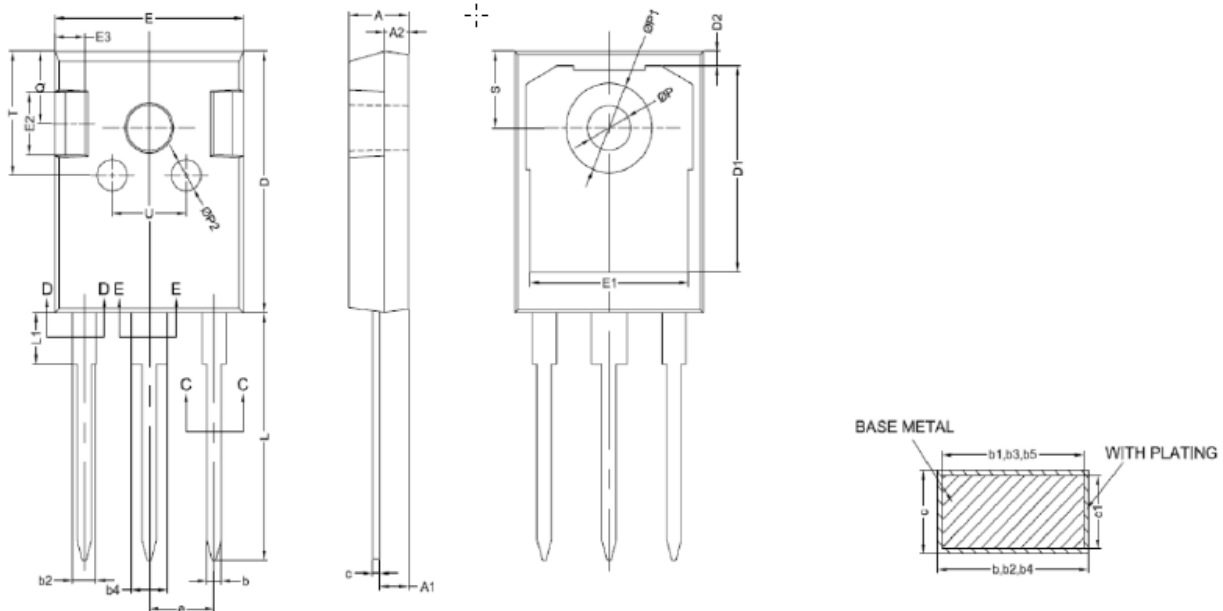


Figure11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

Mechanical Data:
TO247 PACKAGE OUTLINE DIMENSION


Symbol	Dimension In Millimeters			Dimension In Inches		
	Min	Nom	Max	Min	Nom	Max
A	4.900	5.000	5.100	0.193	0.197	0.201
A1	2.300	2.405	2.510	0.091	0.095	0.099
A2	1.900	2.000	2.100	0.075	0.079	0.083
b	1.160	-	1.260	0.046	-	0.050
b1	1.150	1.185	1.220	0.045	0.047	0.048
b2	1.960	-	2.060	0.077	-	0.081
b3	1.950	1.985	2.020	0.077	0.078	0.080
b4	2.960	-	3.060	0.117	-	0.120
b5	2.950	2.985	3.020	0.116	0.118	0.119
c	0.590	-	0.660	0.023	-	0.026
c1	0.580	0.600	0.620	0.023	0.024	0.024
D	20.900	21.000	21.100	0.823	0.827	0.831
D1	16.250	16.550	16.850	0.640	0.652	0.663
D2	1.050	1.200	1.350	0.041	0.047	0.053
E	15.700	15.800	15.900	0.618	0.622	0.626
E1	13.100	13.300	13.500	0.516	0.524	0.531
E2	4.900	5.000	5.100	0.193	0.197	0.201
E3	2.400	2.500	2.600	0.094	0.098	0.102
e	5.44BSC			0.214BSC		
L	19.800	19.950	20.100	0.780	0.785	0.791
L1	-	-	4.300	-	-	0.169
P	3.500	3.600	3.700	0.138	0.142	0.146
P1	-	-	7.400	-	-	0.291
P2	2.400	2.500	2.600	0.094	0.098	0.102
Q	5.600	-	6.000	0.220	-	0.236
S	6.15BSC			0.242BSC		
T	9.800	-	10.200	0.386	-	0.402
U	6.000	-	6.400	0.236	-	0.252

Ordering and Marking Information**Device Marking: SSF9N90ZH****Package (Available)****TO247****Operating Temperature Range****C : -55 to 150 °C****Devices per Unit**

Package Type	Units/ Tube	Tubes/Inner Box	Units/Inner Box	Inner Boxes/Carton Box	Units/Carton Box
TO247	30	8	240	5	1200

Reliability Test Program

Test Item	Conditions	Duration	Sample Size
High Temperature Reverse Bias(HTRB)	$T_j=125^{\circ}\text{C}$ to 150°C @ 80% of Max $V_{DSS}/V_{CES}/V_R$	168 hours 500 hours 1000 hours	3 lots x 77 devices
High Temperature Gate Bias(HTGB)	$T_j=150^{\circ}\text{C}$ @ 100% of Max V_{GSS}	168 hours 500 hours 1000 hours	3 lots x 77 devices

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