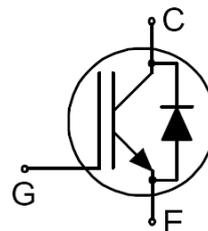


Main Product Characteristics:

V_{CES}	1350V
$V_{CE(sat)}$	1.9V (typ.)
I_D	20A @ TC = 100°C



TO-247



Schematic diagram

Features and Benefits:

- Advanced Trench-FS Process Technology
- Low Collector-Emitter Saturation Voltage, Typical Data is 1.9V@20A
- Fast Switching
- High Input Impedance
- Pb- Free Product
- Power Switch Circuit of Induction Cooker


Description:

It utilizes the latest processing techniques to achieve the high cell density and reduces $V_{CE(sat)}$ rating. These features combine to make this design an extremely efficient and reliable device for use in power switching application of induction cooker and a wide variety of other applications.

Absolute max Rating:

Symbol	Parameter	Max.	Units
I_C @ TC = 25°C	Continuous Collector Current	40	A
I_C @ TC = 100°C	Continuous Collector Current	20	
I_{CM}	Pulsed Collector Current	60	
P_D @TC = 25°C	Power Dissipation@ TC = 25°C	310	W
	Power Dissipation@ TC = 100°C	155	W
V_{CES}	Collector-Emitter Voltage	1350	V
V_{GES}	Gate-to-Emitter Voltage	± 30	V
T_J	Operating Junction Temperature Range	-55 to +175	°C
T_{STG}	Storage Temperature Range	-55 to +175	°C
T_L	Maximum Temperature of Soldering	260	°C

Thermal Resistance

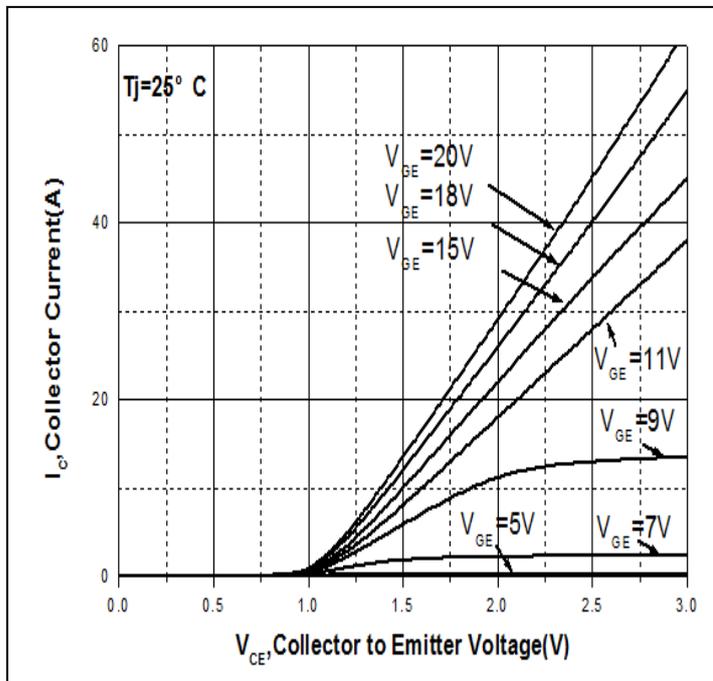
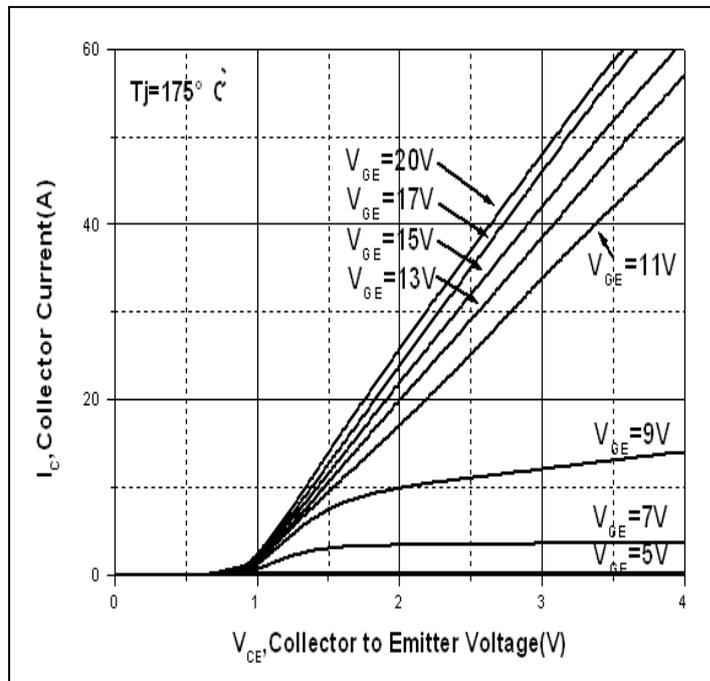
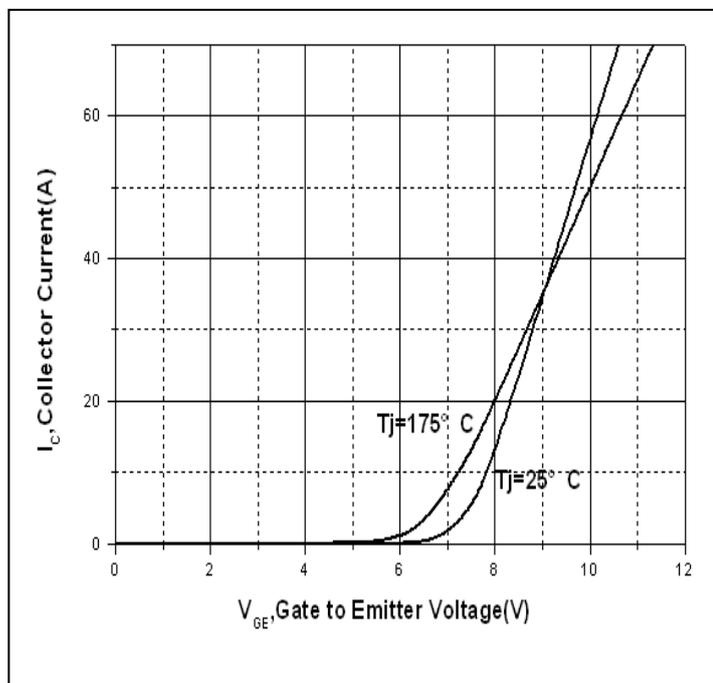
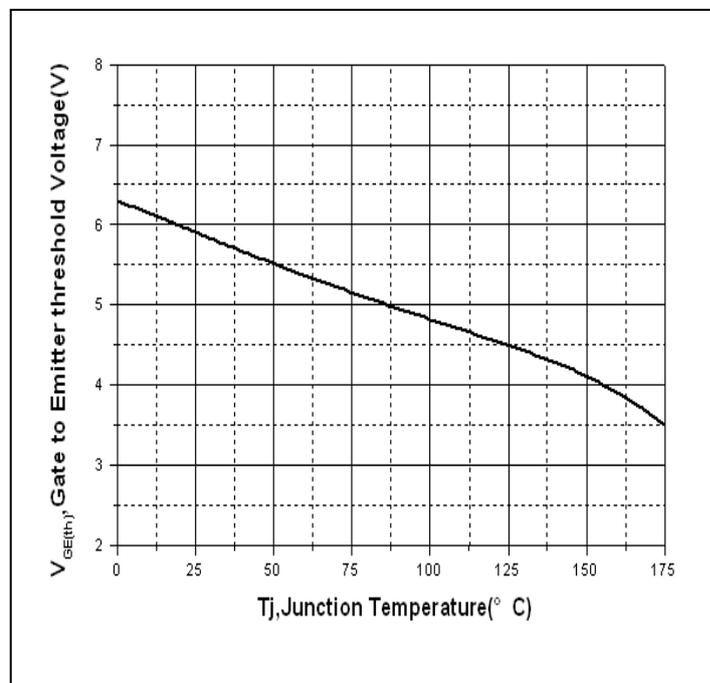
Symbol	Characterizes	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-case ^①	—	0.4	°C/W
$R_{\theta JA}$	Junction-to-ambient ^②	—	40	°C/W

Electrical Characterizes @ $T_A=25^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter breakdown voltage	1350	—	—	V	$V_{GE} = 0V, I_C = 0.5mA$
$V_{CE(sat)}$	Collector-Emitter Saturation voltage	—	1.9	2.1	V	$V_{GE}=15V, I_C=20A, T_C=25^\circ\text{C}$
		—	2.05	—	V	$V_{GE}=15V, I_C=20A, T_C=125^\circ\text{C}$
$V_{GE(th)}$	Gate threshold voltage	4.8	5.8	6.8	V	$V_{GE}=V_{CE}, I_D = 0.4mA$
I_{CES}	Zero gate voltage collector current	—	—	100	μA	$V_{CE} = 1350V$
I_{GES}	Gate-to-Emitter forward leakage	—	—	200	μA	$V_{GE} = 30V$
		—	—	-100		$V_{GE} = -30V$
Q_g	Total gate charge	—	192	—	nC	$I_C = 20A, V_{CE} = 600V, V_{GE} = 15V$
Q_{ge}	Gate-to-Emitter charge	—	16	—		
Q_{gc}	Gate-to-Collector("Miller") charge	—	78	—		
$t_{d(off)}$	Turn-Off delay time	—	190	—	ns	$V_{GE}=15V, V_{CC}=600V, R_g=10\Omega$
t_f	Fall time	—	100	—		
E_{off}	Turn-Off delay time	—	0.9	—	mJ	$I_C=20A, T_J = 25^\circ\text{C}$
C_{ies}	Input capacitance	—	2040	—	pF	$V_{GE} = 0V, V_{CE} = 25V, f = 1MHz$
C_{oes}	Output capacitance	—	70	—		
C_{res}	Reverse transfer capacitance	—	42	—		
t_{rr}	Reverse Recovery Time	—	240	—	ns	$T_J = 25^\circ\text{C}, I_F = 20A, di/dt = 20A/\mu\text{s}$
Q_{rr}	Reverse Recovery Charge	—	3050	—	nC	

Notes:

- ① These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heat sink, assuming maximum junction temperature of $T_J(\text{MAX})=175^\circ\text{C}$.
- ② The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.

Typical electrical and thermal characteristics

Figure 1: Typical Output Characteristics($T_J=25^{\circ}\text{C}$)

Figure 2: Typical Output Characteristics($T_J=175^{\circ}\text{C}$)

Figure 3: Typical Transfer Characteristics

Figure 4: Gate to Emitter threshold Voltage as a function of T_J

Typical electrical and thermal characteristics

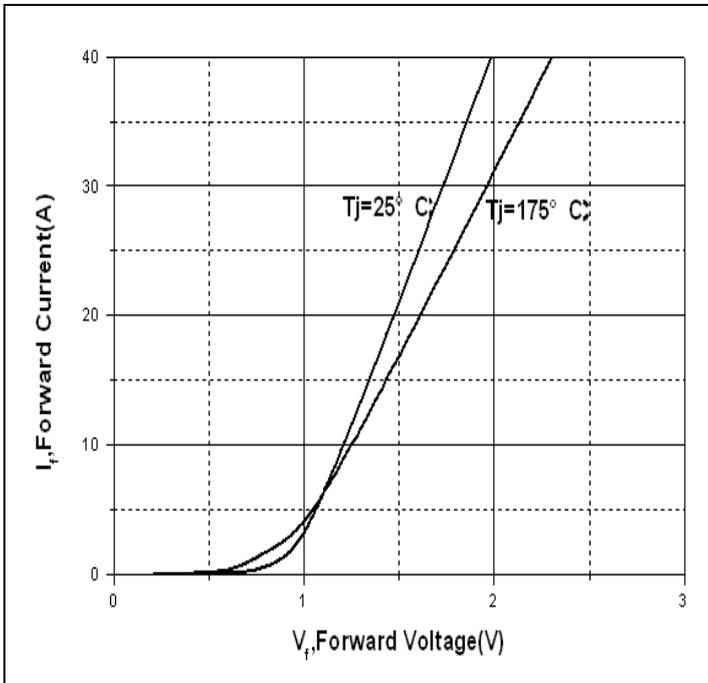


Figure 5: Typical Diode Forward Characteristics

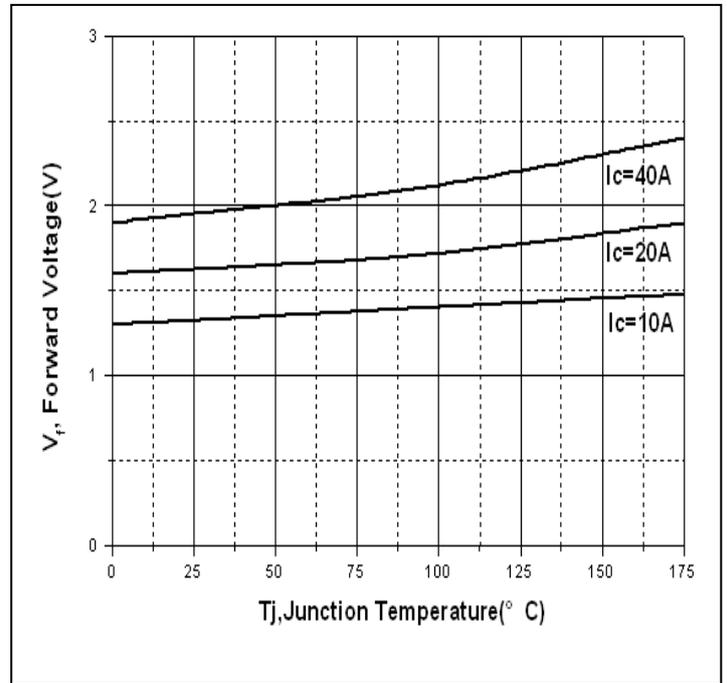


Figure 6: Forward Voltage as a Function of T_j

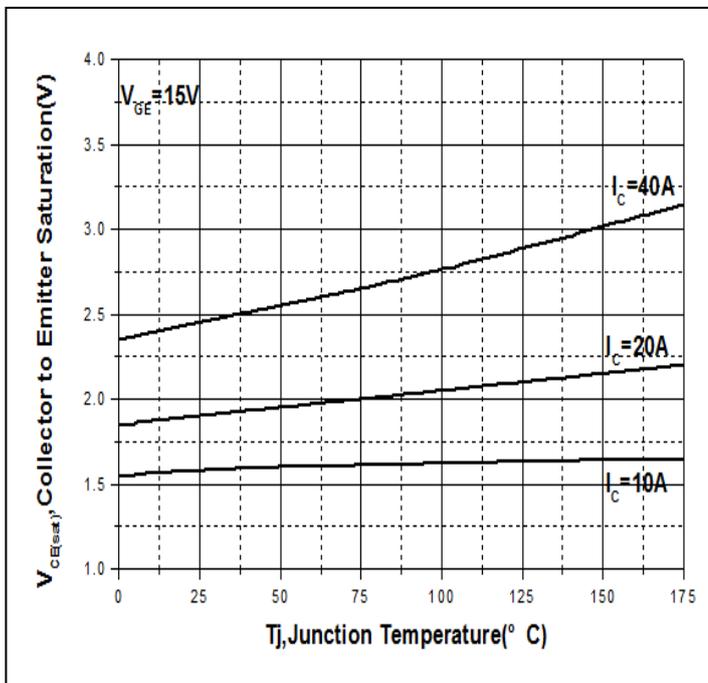


Figure 7: Typical $V_{CE(sat)}$ as a Function of T_j

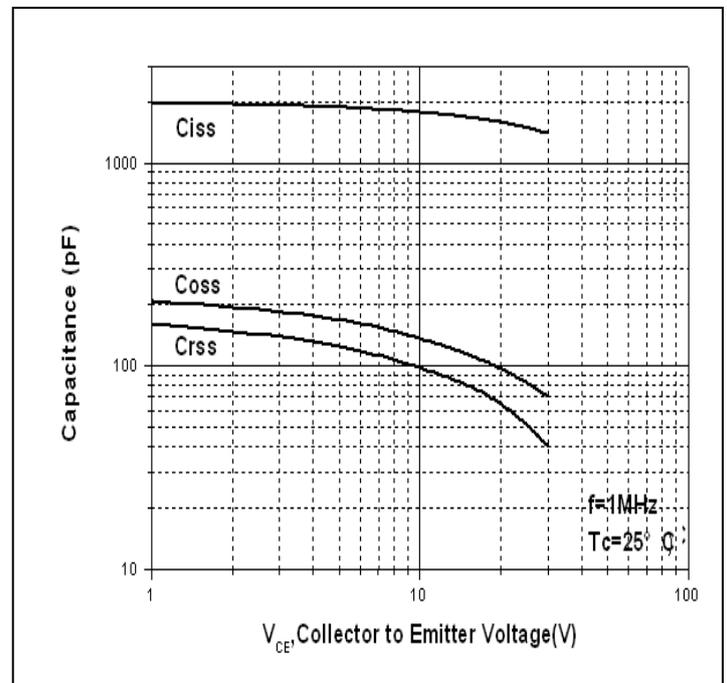


Figure 8: Capacitance Characteristics

Typical electrical and thermal characteristics

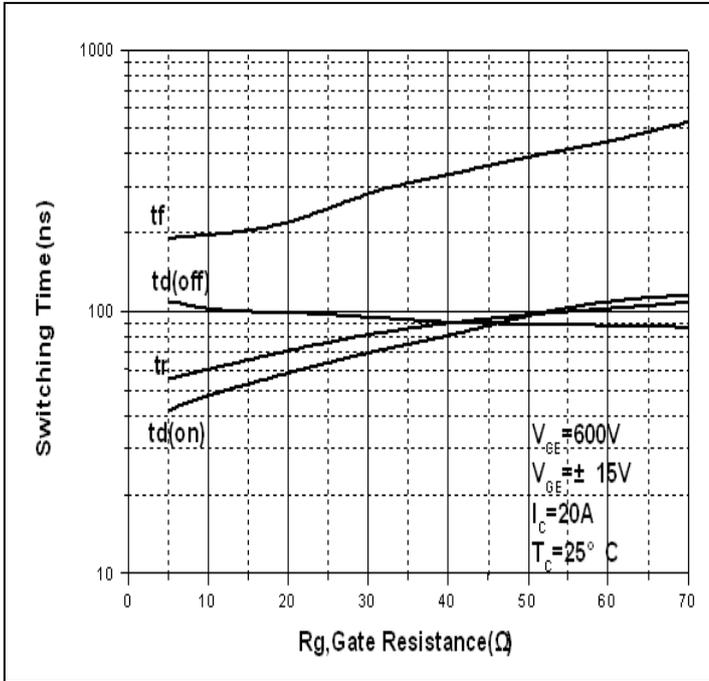


Figure 9: Switching Time Vs Rg

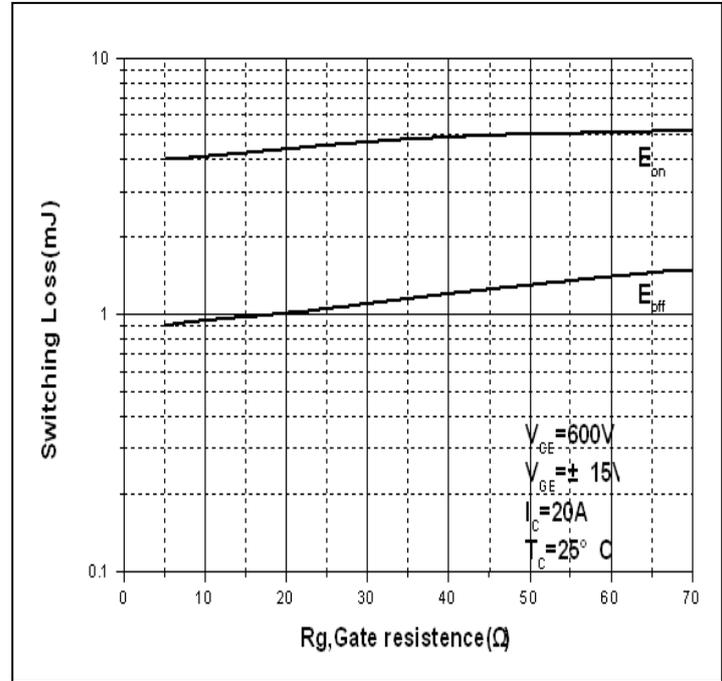


Figure 10: Switching Loss Vs Rg

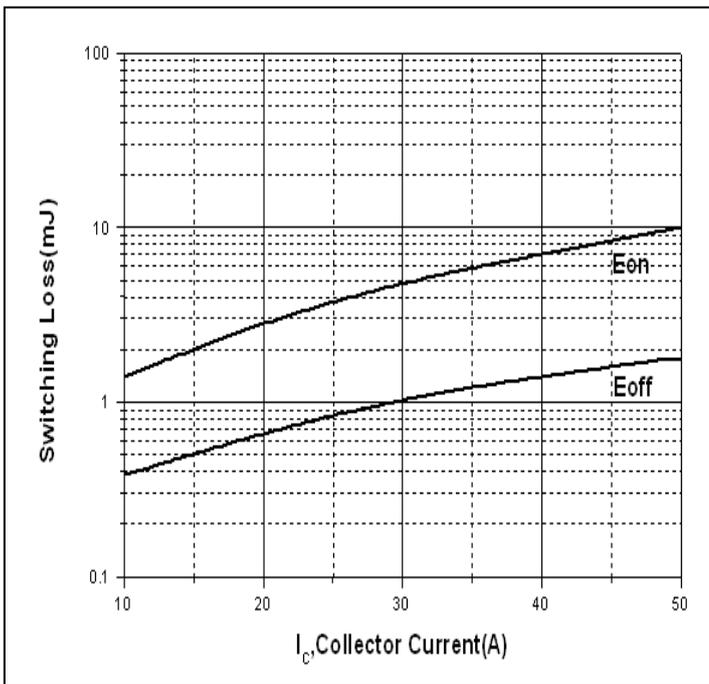


Figure 11: Switching Loss Vs I_C

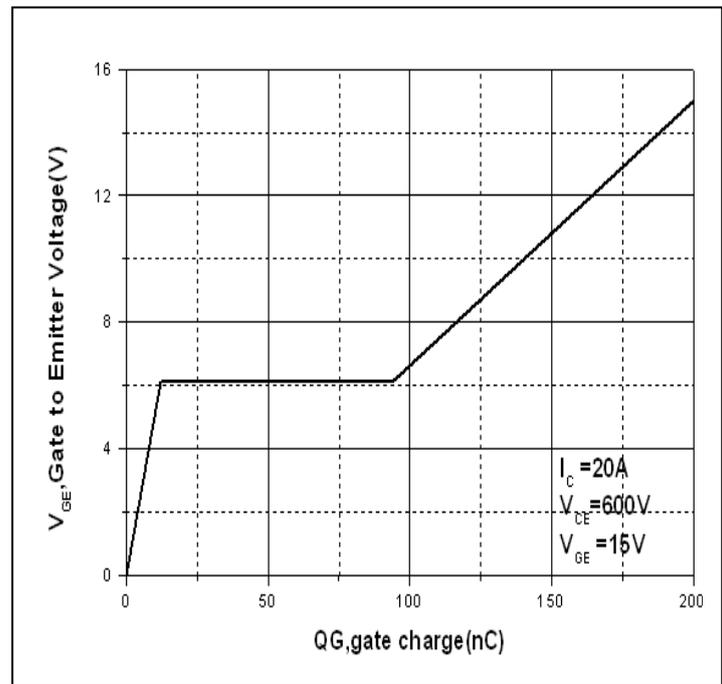


Figure 12: Gate Charge Characteristics

Typical electrical and thermal characteristics

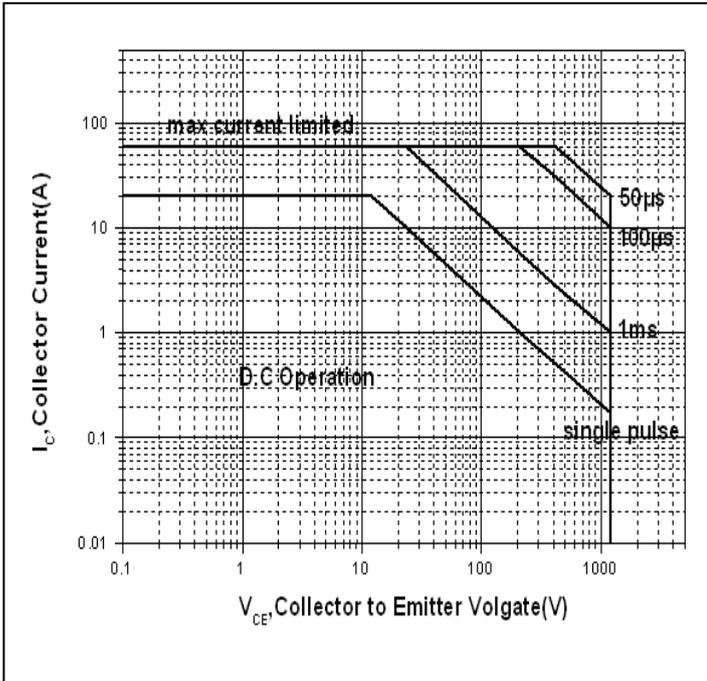


Figure 13. Maximum Forward Biased Safe Operating Area

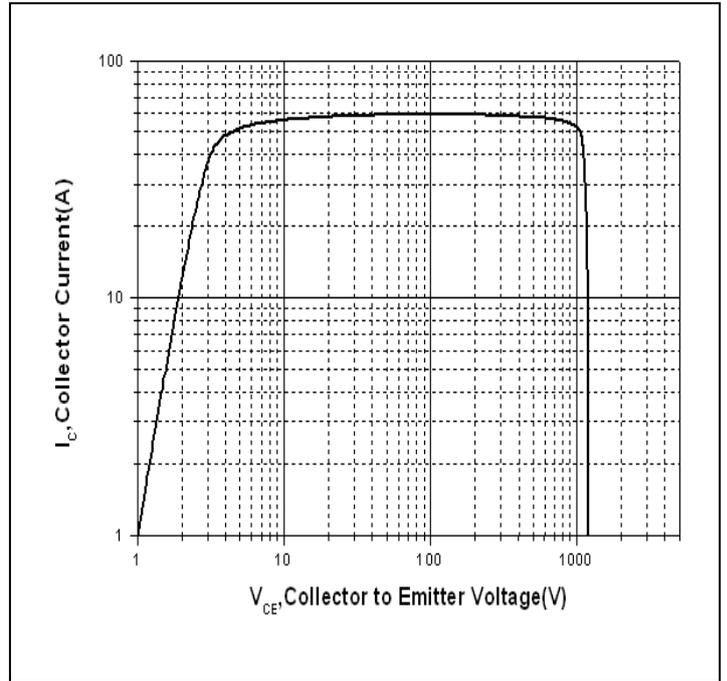


Figure 14. Turn Off Safe Operating Area

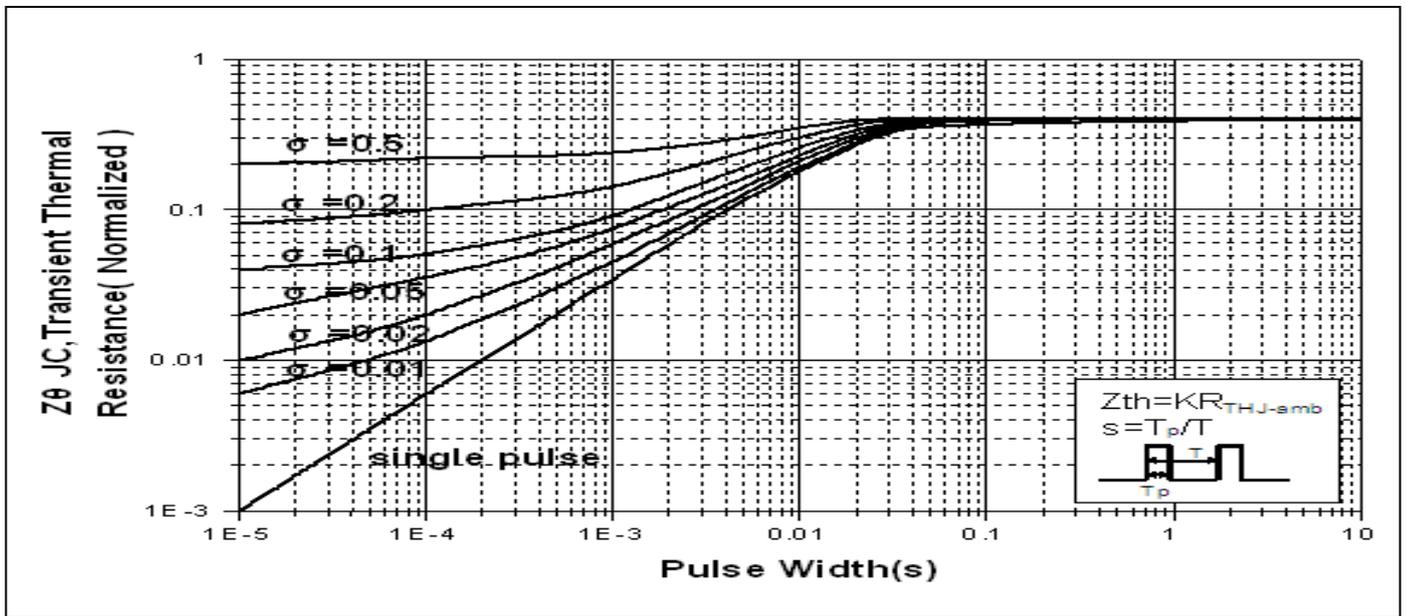
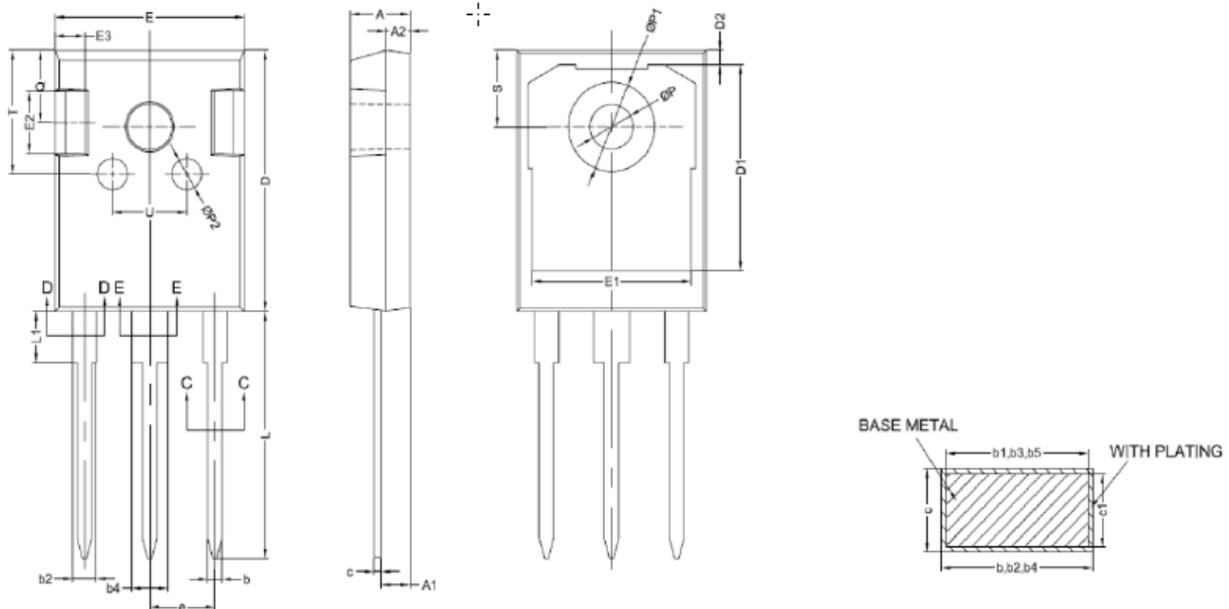


Figure 15. Normalized Maximum Transient Thermal Impedance

Mechanical Data:
TO247 PACKAGE OUTLINE DIMENSION


Symbol	Dimension In Millimeters			Dimension In Inches		
	Min	Nom	Max	Min	Nom	Max
A	4.900	5.000	5.100	0.193	0.197	0.201
A1	2.300	2.405	2.510	0.091	0.095	0.099
A2	1.900	2.000	2.100	0.075	0.079	0.083
b	1.160	-	1.260	0.046	-	0.050
b1	1.150	1.185	1.220	0.045	0.047	0.048
b2	1.960	-	2.060	0.077	-	0.081
b3	1.950	1.985	2.020	0.077	0.078	0.080
b4	2.960	-	3.060	0.117	-	0.120
b5	2.950	2.985	3.020	0.116	0.118	0.119
c	0.590	-	0.660	0.023	-	0.026
c1	0.580	0.600	0.620	0.023	0.024	0.024
D	20.900	21.000	21.100	0.823	0.827	0.831
D1	16.250	16.550	16.850	0.640	0.652	0.663
D2	1.050	1.200	1.350	0.041	0.047	0.053
E	15.700	15.800	15.900	0.618	0.622	0.626
E1	13.100	13.300	13.500	0.516	0.524	0.531
E2	4.900	5.000	5.100	0.193	0.197	0.201
E3	2.400	2.500	2.600	0.094	0.098	0.102
e	5.44BSC			0.214BSC		
L	19.800	19.950	20.100	0.780	0.785	0.791
L1	-	-	4.300	-	-	0.169
P	3.500	3.600	3.700	0.138	0.142	0.146
P1	-	-	7.400	-	-	0.291
P2	2.400	2.500	2.600	0.094	0.098	0.102
Q	5.600	-	6.000	0.220	-	0.236
S	6.15BSC			0.242BSC		
T	9.800	-	10.200	0.386	-	0.402
U	6.000	-	6.400	0.236	-	0.252

Ordering and Marking Information
Device Marking: SSIG20N135H
Package (Available)
TO247
Operating Temperature Range
C : -55 to 175 °C
Devices per Unit

Package Type	Units/Tube	Tubes/Inner Box	Units/Inner Box	Inner Boxes/Carton Box	Units/Carton Box
TO247	30	8	240	5	1200

Reliability Test Program

Test Item	Conditions	Duration	Sample Size
High Temperature Reverse Bias(HTRB)	$T_j=125^{\circ}\text{C}$ to 150°C @ 80% of Max $V_{DSS}/V_{CES}/V_R$	168 hours 500 hours 1000 hours	3 lots x 77 devices
High Temperature Gate Bias(HTGB)	$T_j=150^{\circ}\text{C}$ @ 100% of Max V_{GES}	168 hours 500 hours 1000 hours	3 lots x 77 devices

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