

# Data Sheet

Rev. 1.11 / June 2011

# ZSSC3008

Sensor Signal Conditioner with Diagnostics



# ZSSC3008

Sensor Signal Conditioner with Diagnostics

**ZMDI**<sup>®</sup>  
The Analog Mixed Signal Company



## Brief Description

The ZSSC3008 is a sensor signal conditioner IC that is adjustable to nearly all piezo-resistive bridge sensors. Measured and corrected bridge values are provided at the SIG™ pin, which can be configured as an analog voltage output or as a one-wire serial digital output.

The digital one-wire interface (OWI) can be used for a simple PC-controlled calibration procedure to program a set of calibration coefficients into an on-chip EEPROM. The calibrated ZSSC3008 and a specific sensor are mated digitally: fast, precise, and without the cost overhead associated with trimming by external devices or laser. Integrated diagnostics functions make the ZSSC3008 particularly well-suited for automotive applications.\*

## Features

- Digital compensation of sensor offset, sensitivity, and non-linearity
- Programmable analog gain and digital gain; accommodates bridges with spans < 1mV/V and high offset
- Many diagnostic features on chip (e.g., EEPROM signature, bridge connection checks, bridge short detection, power loss detection)
- Independently programmable high and low clipping levels
- 24-bit customer ID field for module traceability
- Output options: rail-to-rail ratiometric analog voltage (12-bit resolution), absolute analog voltage, digital one-wire interface
- Fast power-up to data out response; output available 5ms after power-up
- Current consumption depends on programmed sample rate: 1mA down to 250µA (typical)
- Fast response time: 1ms (typical)
- High voltage protection up to 30V with external JFET

## Benefits

- PC-controlled configuration and calibration via one-wire interface – simple, low cost
- High accuracy ( $\pm 0.1\%$  FSO @ -25 to 85°C;  $\pm 0.25\%$  FSO @ -40 to 125°C)
- Single-pass calibration – quick and precise

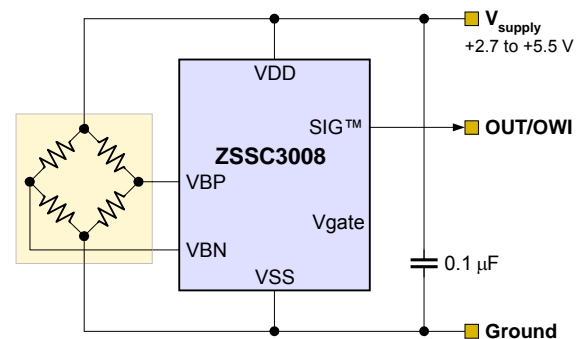
## Available Support

- Development Kit available
- Multi-Unit Calibrator Kit available
- Support for industrial mass calibration available
- Quick circuit customization possible for large production volumes

## Physical Characteristics

- Wide operation temperature: -40°C to +125°C
- Supply voltage 2.7 to 5.5V; with external JFET, 5.5 to 30V
- Small SOP8 package

## ZSSC3008 Application Circuit



\* Not AEC-Q100-qualified.

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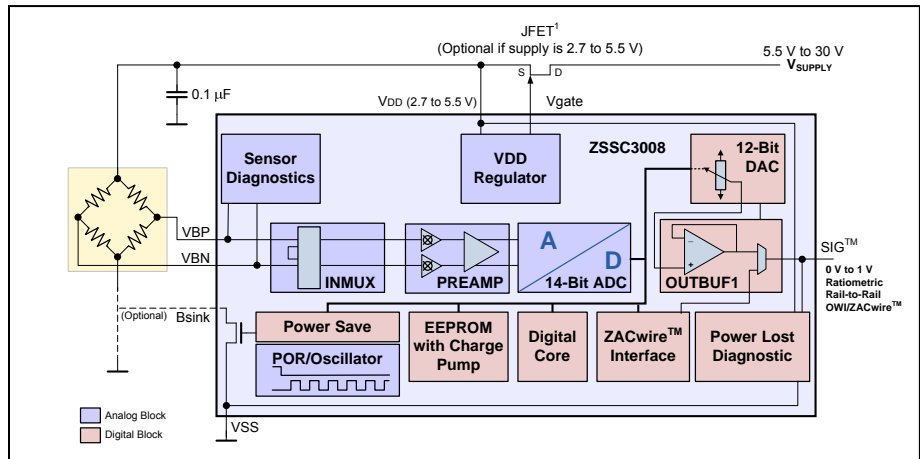


## ZSSC3008 Block Diagram

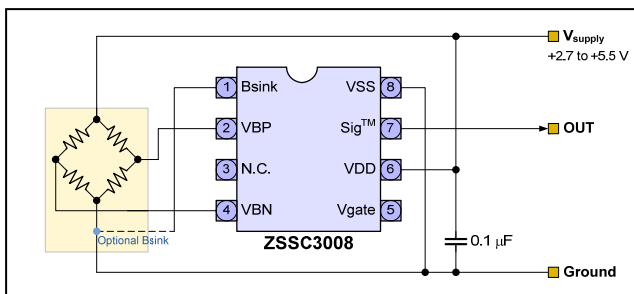
Highly Versatile Applications in Many Markets Including

- ❖ Industrial
- ❖ Building Automation
- ❖ Office Automation
- ❖ White Goods
- ❖ Automotive \*
- ❖ Portable Devices
- ❖ Your Innovative Designs

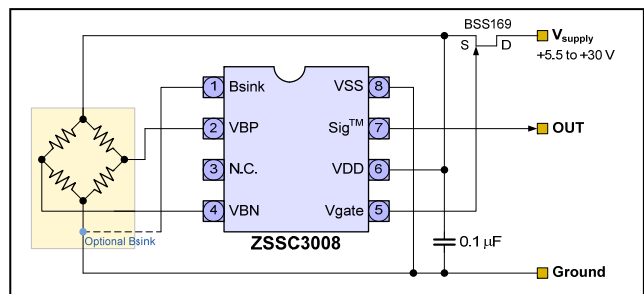
\* Not AEC-Q100-qualified.



### Rail-to-Rail Ratiometric Voltage Output Applications



### Absolute Analog Voltage Output Applications



Product Ordering Codes (Please contact ZMDI Sales for additional options.)

Sales Code	Description	Package
ZSSC3008AA2R	ZSSC3008 SOP8 (150 mil) — Temperature range: -40°C to +125°C	Tape and Reel
ZSSC3008AA2T	ZSSC3008 SOP8 (150 mil) — Temperature range: -40°C to +125°C	Tube
ZSSC3008KIT	ZSSC3008 SSC Evaluation Kit: Communication Board, SSC Board, Sensor Replacement Board, Evaluation Software, USB Cable, 5 IC Samples	Kit

## Sales and Further Information

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# 1 Electrical Characteristics

## 1.1. Absolute Maximum Ratings

**Table 1.1 Absolute Maximum Ratings**

Parameter	Symbol	Min.	Max.	Unit
Analog Supply Voltage	$V_{DD}$	-0.3	6.0	V
Voltages at Analog I/O – In Pin	$V_{INA}$	-0.3	$V_{DD}+0.3$	V
Voltages at Analog I/O – Out Pin	$V_{OUTA}$	-0.3	$V_{DD}+0.3$	V
Storage Temperature Range ( $\geq 10$ hours)	$T_{STOR}$	-50	150	$^{\circ}C$
Storage Temperature Range ( $< 10$ hours)	$T_{STOR < 10h}$	-50	170	$^{\circ}C$

Note: Also see Table 6.1 regarding soldering temperature and storage conditions for the SOP-8 package.

## 1.2. Recommended Operating Conditions

**Table 1.2 Recommended Operating Conditions**

Parameter	Symbol	Min.	Typ.	Max.	Unit
Analog Supply Voltage to Ground	$V_{DD}$	2.7	5.0	5.5	V
Analog Supply Voltage (with external JFET Regulator)	$V_{SUPP}$	5.5	7	30	V
Common Mode Voltage	$V_{CM}$	1		$V_{DDA} - 1.3$	V
Ambient Temperature Range <sup>1,2</sup>	$T_{AMB}$	-40		125	$^{\circ}C$
External Capacitance between $V_{DD}$ and Ground	$C_{VDD}$	100	220	470	nF
Output Load Resistance to $V_{SS}$ or $V_{DD}$ <sup>3</sup>	$R_{L,OUT}$	5			$k\Omega$
Output Load Capacitance <sup>4</sup>	$C_{L,OUT}$		10	15	nF
Bridge Resistance <sup>5</sup>	$R_{BR}$	1		100	$k\Omega$
Power-On Rise Time	$t_{PON}$			100	ms

<sup>1)</sup> Note that the maximum EEPROM programming temperature is 85 $^{\circ}C$ .

<sup>2)</sup> If buying die, designers should use caution not to exceed maximum junction temperature by proper package selection.

<sup>3)</sup> Only needed for Analog Output Mode; not needed for Digital Output Mode. When a pull-down resistor is used as load resistor, the power loss detection diagnostic for loss of VSS cannot be assured at  $R_L=5k$ ;  $R_L=10k$  is recommended for this configuration.

<sup>4)</sup> Using the output for digital calibration,  $C_{L,OUT}$  is limited by the maximum rise time  $T_{ZACrise}$ . See section 1.3.

<sup>5)</sup> Note: Minimum bridge resistance is only a factor if using the Bsink feature. The  $R_{DS(ON)}$  of the Bsink transistor is 8 to 10 $\Omega$  when operating at  $V_{DD}=5V$ . This does give rise to a ratiometricity inaccuracy that becomes greater with low bridge resistances.

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## 1.3. Electrical Parameters

Note: In this section, an asterisk (\*) marks parameters for which there is no verification in mass production; the parameter is guaranteed by design and/or quality observation.

**Table 1.3 Supply/Regulation Characteristics**

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Supply Voltage	$V_{DD}$	2.7	5.0	5.5	V	
Supply Current (varies with update rate and output mode)	$I_{DD}$		0.25		mA	At minimum update rate
			1.0	1.4	mA	At maximum update rate
Power Supply Rejection Ratio *	PSRR	60			dB	
Power-On Reset Level	POR	1.4		2.6	V	

**Table 1.4 Parameters for Analog Front-End (AFE)**

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Leakage Current Pin VBP, VBN	$I_{IN\_LEAK}$			$\pm 10$	nA	Sensor connection and short check must be disabled.

**Table 1.5 Parameters for EEPROM**

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Number Write Cycles	$n_{WRI\_EEP}$			100k	Cycles	At 85°C
Data Retention	$t_{WRI\_EEP}$			10	Years	At 100°C

**Table 1.6 Parameters for A/D Converter**

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
ADC Resolution	$r_{ADC}$			14	Bit	
Integral Nonlinearity (INL) <sup>1)</sup>	$INL_{ADC}$	-4		+4	LSB	Based on ideal slope
Differential Nonlinearity (DNL) *	$DNL_{ADC}$	-1		+1	LSB	

<sup>1)</sup> Note: This is  $\pm 4$  LSBs for the 14-bit A-to-D conversion. This results in absolute accuracy to 12-bits on the A-to-D result. Non-linearity is typically better at temperatures less than 125°C.

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**Table 1.7 Parameters for Analog Output (DAC and Buffer)**

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Max. Output Current	$I_{OUT}$	2.2			mA	Max. current maintaining accuracy
Resolution	Res			12	Bit	Referenced to $V_{DD}$
Absolute Error	$E_{ABS}$			$\pm 0.25$	% $V_{DD}$	DAC input to output ratiometric mode
				$\pm 5$	mV	DAC input to output 0-1V mode
Differential Nonlinearity *	DNL	-0.9		+3.0	LSB <sub>12Bit</sub>	No missing codes
Upper Output Voltage Limit	$V_{OUT}$	95%			$V_{DD}$	$R_L = 5\text{ k}\Omega$
Lower Output Voltage Limit	$V_{OUT}$			16.5mV	mV	With 5k $\Omega$ pull down, 0-1V output
Output Short Circuit Protection Limit	$I_{SC}$	3		40	mA	Depends on operating conditions. Short circuit protection must be enabled via Diag_cfg (EEPROM word [102:100]). See section 2.4.2.
Analog Output Noise Peak-to-Peak	$V_{NOISE,PP}$			5 $\pm 1$ LSB	mV	Shorted input

**Table 1.8 Diagnostics**

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Upper diagnostic output level	$V_{DIA,H}$	97.5%			$V_{DD}$	Ratiometric analog output mode
Lower diagnostic output level	$V_{DIA,L}$			2.5%	$V_{DD}$	Ratiometric analog output mode
Min. load resistor for power loss	$R_{L,OUT,PS}$	5			k $\Omega$	Pull-up or pull-down <sup>1</sup> in Analog Output Mode

<sup>1)</sup> When using a pull-down resistor as load resistor, the power loss detection diagnostic for loss of VSS cannot be assured at  $R_L=5\text{k}$ ;  $R_L=10\text{k}$  is recommended for this configuration.

**Table 1.9 Parameters for ZACwire™ Serial Interface**

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
ZACwire™ Line Resistance *	$R_{ZAC,load}$			3.9	k $\Omega$	The rise time must be $T_{ZAC,rise} = 2 * R_{ZAC,load} * C_{ZACload} \leq 5\mu\text{s}$ . If using a pull-up resistor instead of a line resistor, it must meet this specification. The absolute maximum for $C_{ZACload}$ is 15nF.
ZACwire™ Load Capacitance *	$C_{ZAC,load}$	0	1	15	nF	
Voltage Level Low *	$V_{ZAC,low}$		0	0.2	$V_{DD}$	
Voltage Level High *	$V_{ZAC,low}$	0.8	1		$V_{DD}$	

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**Table 1.10 Parameters for System Response**

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Start-Up-Time	$t_{STA}$			5	ms	Power-up to output Update_rate = 1 kHz (1 ms)
Response Time – Analog Output	$t_{RESP-A}$		1	2	ms	Update_rate = 1 kHz (1 ms)
Response and Transmission Time for Digital Output	$t_{RES, DIG}$		1.6		ms	Varies with update rate. Value given at fastest rate.
Sampling Rate	$f_s$		1000		Hz	Update_rate = 1 kHz (1 ms)
Overall Linearity Error– Digital	$E_{LIND}$		0.025	0.04	%	Bridge input to output
Overall Linearity Error – Analog	$E_{LINA}$		0.1	0.25	%	Bridge input to output
Overall Ratiometricity Error	$RE_{out}$			0.035	%	$\pm 10\%VDD$ , Not using Bsink feature
Overall Accuracy – Digital (only IC, without sensor bridge)	$AC_{outD}$			$\pm 0.1\%$	%FSO	-25°C to 85°C
				$\pm 0.25\%$		-40°C to 125°C
Overall Accuracy – Analog <sup>1)2)</sup> (only IC, without sensor bridge)	$AC_{outA}$			$\pm 0.35\%$	%FSO	-25°C to 85°C
				$\pm 0.5\%$		-40°C to 125°C
1) Not included is the quantization noise of the DAC. The 12-bit DAC has a quantization noise of $\pm \frac{1}{2} \text{ LSB} = 0.61 \text{ mV} (@ 5 \text{ V } VDD) = 0.0125\%$ .						
2) Analog output range 2.5% to 95%						

## 1.4. Analog Input versus Output Resolution

The ZSSC3008 has a fully differential chopper-stabilized pre-amplifier with 4 programmable gain settings. The output of the pre-amplifier feeds into a 14-bit charge-balanced ADC. Span, offset, and non-linearity correction are performed in the digital domain. Then the resulting corrected bridge value can be output in analog form through a 12-bit DAC or as a 16-bit serial digital packet. The resolution of the output depends on the input span (bridge sensitivity) and the analog gain setting programmed. Digital gains can vary from [0,32). Analog gains available are 6, 24, 48, and 96.

Note: At higher analog gain settings, there will be higher output resolution, but the ability of the ZSSC3008 to handle large offsets decreases. This is expected because the offset is also amplified by the analog gain and can therefore saturate the ADC input.

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The following tables outline the guaranteed minimum resolution for a given bridge sensitivity range.

**Table 1.11 ADC Resolution Characteristics for an Analog Gain of 6**

Analog Gain 6				
Input Span [mV/V]			Allowed Offset (+/- % of Span)	Minimum Guaranteed Resolution [Bits]
Min.	Typ.	Max.		
57.8	80.0	105.8	38%	12.4
50.6	70.0	92.6	53%	12.2
43.4	60.0	79.4	73%	12.0
36.1	50.0	66.1	101%	11.7
28.9	40.0	52.9	142%	11.4
21.7	30.0	39.7	212%	11.4

**Table 1.12 ADC Resolution Characteristics for an Analog Gain of 24**

Analog Gain 24				
Input Span [mV/V]			Allowed Offset (+/- % of Span)	Minimum Guaranteed Resolution [Bits]
Min.	Typ.	Max.		
18.1	25.0	33.1	17%	12.7
14.5	20.0	26.5	38%	12.4
7.2	10.0	13.2	142%	11.4
3.6	5.0	6.6	351%	10.4
1.8	2.5	3.3	767%	9.4
0.9	1.2	1.6	1670%	8.4

**Important Note:** The yellow shadowed fields indicate that for these input spans with the selected analog gain setting, the quantization noise is higher than 0.1% FSO.

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**Table 1.13 ADC Resolution Characteristics for an Analog Gain of 48**

Analog Gain 48				
Input Span [mV/V]			Allowed Offset (+/- % of Span)	Minimum Guaranteed Resolution [Bits]
Min.	Typ.	Max.		
10.8	15.0	19.8	3%	13.0
7.2	10.0	13.2	38%	12.4
4.3	6.0	7.9	107%	11.7
2.9	4.0	5.3	194%	11.1
1.8	2.5	3.3	351%	10.4
1.0	1.4	1.85	678%	9.6
0.72	1.0	1.32	976%	9.1

**Important Note:** The yellow shadowed fields indicate that for these input spans with the selected analog gain setting, the quantization noise is higher than 0.1% FSO.

**Table 1.14 ADC Resolution Characteristics for an Analog Gain of 96**

Analog Gain 96				
Input Span [mV/V]			Allowed Offset (+/- % of Span)	Minimum Guaranteed Resolution [Bits]
Min.	Typ.	Max.		
4.3	6.0	7.9	21%	12.7
2.9	4.0	5.3	64%	12.1
1.8	2.5	3.3	142%	11.4
1.0	1.4	1.85	306%	10.6
0.72	1.0	1.32	455%	10.1



## 2 Circuit Description

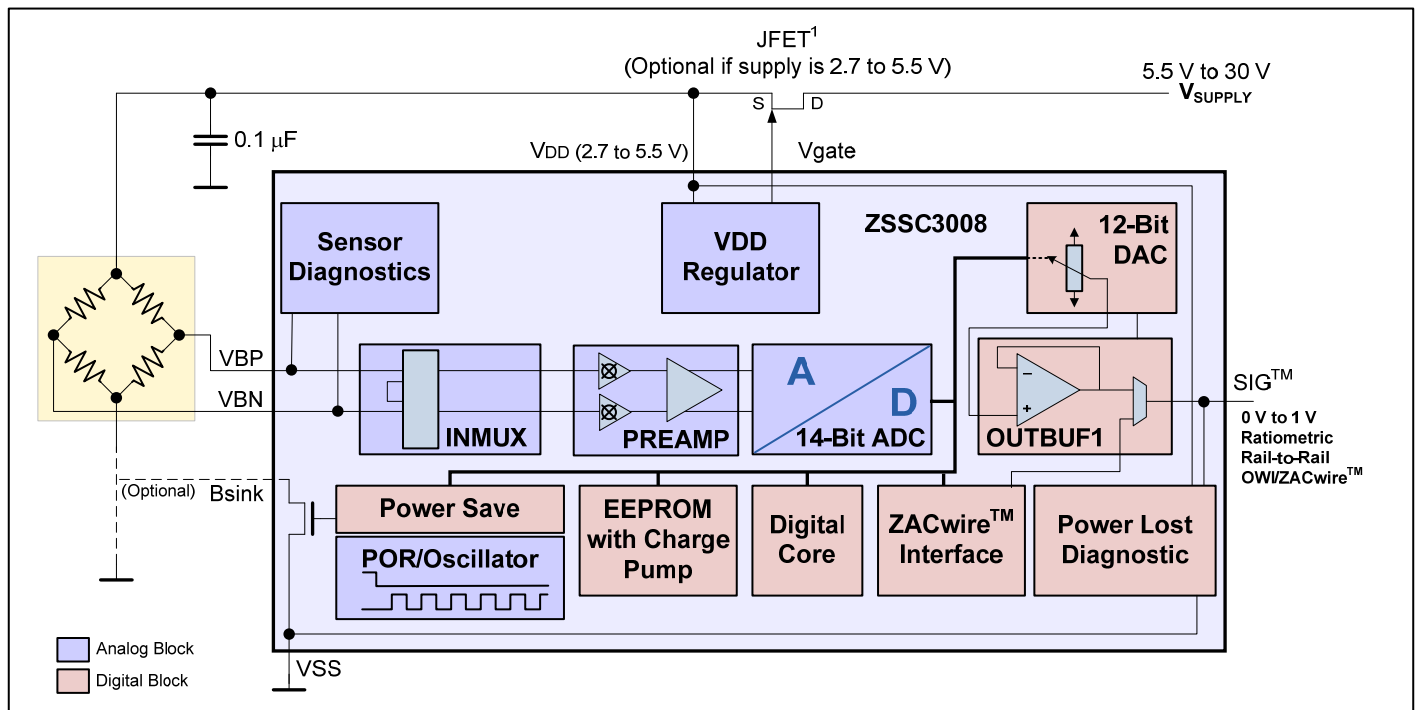
### 2.1. Signal Flow and Block Diagram

ZMDI's series of resistive bridge sensor interface ICs were specifically designed as cost-effective solutions for sensing in building automation, automotive, industrial, office automation, and white goods applications. The ZSSC3008 employs a low-power 14-bit analog-to-digital converter (ADC, A2D, A-to-D) and an on-chip DSP core with EEPROM to precisely calibrate the bridge output signal.

Three selectable outputs, two analog and one digital, offer the ultimate in versatility across many applications. The ZSSC3008 rail-to-rail ratiometric analog  $V_{out}$  signal (0V to  $\sim 5V V_{out} @ V_{DD}=5V$ ) suits most building automation and automotive requirements (12-bit resolution). Typical office automation and white goods applications require the 0 to  $\sim 1V V_{out}$  signal, which in the ZSSC3008 is referenced to the internal bandgap. ZSSC3008 is capable of running in high-voltage (5.5-30V) systems when combined with an external JFET.

Direct interfacing to  $\mu P$  controllers is facilitated via ZMDI's single-wire serial ZACwire™ digital interface.

**Figure 2.1 ZSSC3008 Block Diagram**



\* Not AEC-Q100-qualified.



## 2.2. Analog Front End

### 2.2.1. Bridge Supply

The voltage-driven bridge is usually connected to  $V_{DD}$  and ground. As a power savings feature, the ZSSC3008 also includes a switched transistor to interrupt the bridge current via pin 1 (Bsink). The transistor switching is synchronized to the analog-to-digital conversion and released after finishing the conversion. To use this feature, connect the low supply of the bridge to Bsink instead of ground.

Depending on the programmable update rate, the average current consumption (including bridge current) can be reduced to approximately 20%, 5% or 1%.

### 2.2.2. PREAMP Block

The differential signal from the bridge is amplified through a chopper-stabilized instrumentation amplifier with very high input impedance designed for low noise and low drift. This pre-amp provides gain for the differential signal and re-centers its DC to  $V_{DD}/2$ . The output of the Pre-Amp block is fed into the ADC. The calibration sequence performed by the digital core includes an auto-zero sequence to null any drift in the Pre-Amp over temperature.

The Pre-Amp can be set to a gain of 6, 24, 48 or 96 through EEPROM.

The inputs to the Pre-Amp from (VBN/VBP pins) can be reversed via an EEPROM configuration bit.

### 2.2.3. Analog-to-Digital Converter (ADC)

A 14-bit/1ms 2<sup>nd</sup> order charge-balancing ADC is used to convert signals coming from the pre-amp. The converter, designed in full differential switched-capacitor technique, is used for converting the various signals in the digital domain.

This principle offers the following advantages:

- High noise immunity because of the differential signal path and integrating behavior
- Independence from clock frequency drift and clock jitter
- Fast conversion time due to second order mode

Four selectable values for the zero point of the input voltage allow the conversion to adapt to the sensor's offset parameter. With the Reverse Input Polarity Mode and the negative digital gain options, this results in seven possible zero point adjustments (not eight because the -1/2, 1/2 offset setting is the same regardless of gain polarity).

The conversion rate varies with the programmed update rate. The fastest conversation rate is 1k samples/s and the response time is then 1ms. Based on a best fit, the Integral Nonlinearity (INL) is less than 4 LSB<sub>14Bit</sub>.



### 2.3. Digital Signal Processor

A digital signal processor (DSP) is used for processing the converted bridge data for output on the digital channel. The digital core reads correction coefficients from EEPROM and can correct for the following:

- Bridge Offset
- Bridge Gain
- A single second order effect (SOT) (Second Order Term)

The EEPROM contains a single SOT term that can be applied to correct 2<sup>nd</sup> order behavior of the bridge measurement. The correction formula for the bridge reading is represented as a two step process as follows:

$$ZB = \text{Gain\_B} * (\text{BR\_Raw} - \text{Offset\_B}) \quad (1)$$

$$\text{BR} = ZB(1.25 + \text{SOT} * ZB) \quad (2)$$

Where:

<b>BR</b>	=	Corrected bridge reading that is output as digital or analog on SIG <sup>TM</sup> pin
<b>ZB</b>	=	Intermediate result in the calculations
<b>BR_Raw</b>	=	Raw bridge reading from ADC
<b>Gain_B</b>	=	Bridge gain term
<b>Offset_B</b>	=	Bridge offset term
<b>SOT</b>	=	Second order term

**Note** For solving equation (1) the following condition must be met:

$$\text{BR\_Raw} \geq \text{BR} / \text{Gain\_B}$$

If this condition is not met, the analog Pre-Amp gain must be set to a smaller value because a negative Offset\_B is not supported.

#### 2.3.1. EEPROM

The EEPROM contains the calibration coefficients for gain and offset, etc., and the configuration bits, such as output mode, update rate, etc. The ZSSC3008 also offers 3 user-programmable storage bytes for module traceability. When programming the EEPROM, an internal charge pump voltage is used; therefore a high voltage supply is not needed. The EEPROM is implemented as a shift register. During an EEPROM read, the contents are shifted 8 bits before each transmission of one byte occurs. The charge pump is internally regulated to 12.5 V, and the programming time is 6ms.

See section 2.6.1 regarding EEPROM signatures for verifying EEPROM integrity.

Note: EEPROM writing can only be performed at temperatures lower than 85°C.



### 2.3.2. One-Wire Interface - ZACwire™

The IC communicates via a one-wire serial interface. There are different commands available for the following:

- Reading the conversion result of the ADC (Get\_BR\_Raw)
- Calibration commands
- Reading from the EEPROM (dump of entire contents)
- Writing to the EEPROM (trim setting, configuration, and coefficients)

## 2.4. Output Stage

### 2.4.1. Digital to Analog Converter (Output DAC) with Programmable Clipping Limits

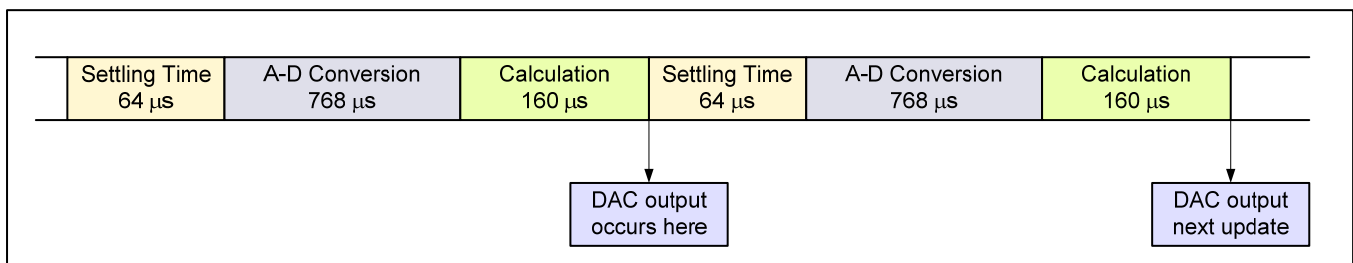
A 12-bit DAC based on sub-ranging resistor strings is used for the digital-to-analog output conversion in the analog ratiometric and absolute analog voltage modes. Options during calibration configure the system to operate in either of these modes. The design allows for excellent testability as well as low power consumption. The DAC allows programming a lower and upper clipping limit for the output signal (analog and digital). The internal 14-bit calculated bridge value is compared against the 14-bit value formed by {11,Up\_Clip\_Lim[6:0],11111} for the upper limit and {00,Low\_Clip\_Lim[6:0],00000} for the lower limit. If the calculated bridge value is higher than the upper limit or less than the lower limit, the analog output value is clipped to this value; otherwise it is output as is.

**Example for the upper clipping level:** If the Up\_Clip\_Lim[6:0] = 0000000, then the 14-bit value used for clipping threshold is 11000000011111. This is 75.19% of full scale. Since there are 7 bits of upper clipping limit, there are 127 possible values between 75.19% and 100%. Therefore the resolution of the clipping limits 0.195%.

**Example for the lower clipping level:** If the Low\_Clip\_Lim[6:0] = 1111111, then the 14-bit value used for clipping threshold is 00111111100000. This is 24.8% of full scale. Since there are 7 bits of lower clipping limit, there are 127 possible values between 0 and 24.8%. Therefore the resolution of the lower clipping limit is 0.195%.

Figure 2.2 shows the data timing of the DAC output for the update rate setting 00.

**Figure 2.2 DAC Output Timing for Highest Update Rate**



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## 2.4.2. Output Buffer

A rail-to-rail op amp configured as a unity gain buffer can drive resistive loads (whether pull-up or pull-down) as low as 5k $\Omega$  and capacitances up to 15nF (for pure analog output). In addition, to limit the error due to amplifier offset voltage, an error compensation circuit is included that tracks and reduces offset voltage to < 1mV. The output of the ZSSC3008 output can be permanently shorted to VDD or VSS without damaging the device. The output driver contains a current-limiting block that detects a hard short and limits the current to a safe level. The short circuit protection current can vary from a minimum of 3mA to a maximum of 40mA depending on operating conditions. Output short circuit protection can be enabled via Diag\_cfg (EEPROM [102:100]). Enabling this protection is recommended when using the analog output.

## 2.4.3. Voltage Reference Block

A linear regulator control circuit is included in the Voltage Reference Block to interface with an external JFET to allow operation in systems where the supply voltage exceeds 5.5V. This circuit can also be used for over-voltage protection. The regulator set point has a coarse adjustment controlled by the JFET\_cfg EEPROM bits that can adjust the set point around 5.0 or 5.5V (See Table 3.5 for bit locations and section 2.3.1 regarding writing to the EEPROM.). The 1V trim setting (see below) can also act as a fine adjust for the regulation set point. The 5V reference can be trimmed within +/-15mV.

Note: If using the external JFET for over-voltage protection purposes (i.e., 5V at JFET drain and expecting 5V at JFET source), there will be a voltage drop across the JFET; therefore ratiometricity will be slightly compromised depending on the rds(on) of the chosen JFET. A Vishay J107 is the best choice because it has only an 8mV drop worst case. If using as regulation instead of over-voltage, a MMBF4392 or BSS169 also works well.

The Voltage Reference Block uses the absolute reference voltage provided by the bandgap to produce two regulated on-chip voltage references. A 1V reference is used for the output DAC high reference when the part is configured in 0-1V Analog Output Mode. For this reason, the 1V reference must be very accurate and includes trim so that its value can be trimmed within +/- 3mV of 1.00V. The 1V reference is also used as the on-chip reference for the JFET regulator block. The regulation set point of the JFET regulator can be fine tuned using the 1V trim.

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The reference trim setting is selected with the 1V\_Trim/JFET\_Trim bits in EEPROM. See Table 3.5 for bit locations. Table 2.1 shows the order of trim codes with 0111 for the lowest reference voltage and 1000 for the highest reference voltage.

**Important:** Optimal reference trim is determined during wafer-level testing and final package testing. Back-up copies of these bits are stored in bits in the CUST\_ID0 bits for applications requiring accurate references. In this case, see section 5 for important notes and instructions for verifying the integrity of the 1V\_Trim/JFET\_Trim bits and if necessary, restoring the value from the CUST\_ID0 bits before calibration.

**Table 2.1** 1V Reference Trim (1V vs. Trim for Nominal Process Run)

Order	1Vref/ 5Vref_trim3	1Vref/ 5Vref_trim2	1Vref/ 5Vref_trim1	1Vref/ 5Vref_trim0
Highest Reference Voltage	1	0	0	0
...	1	0	0	1
...	1	0	1	0
...	1	0	1	1
...	1	1	0	0
...	1	1	0	1
...	1	1	1	0
...	1	1	1	1
...	0	0	0	0
...	0	0	0	1
...	0	0	1	0
...	0	0	1	1
...	0	1	0	0
...	0	1	0	1
...	0	1	1	0
Lowest Reference Voltage	0	1	1	1

## 2.5. Clock Generator / Power-On Reset (CLKPOR)

If the power supply exceeds 2.5V (maximum), the reset signal de-asserts and the clock generator starts working at a frequency of approximately 512kHz ( $\pm 20\%$ ). The exact value only influences the conversion cycle time and communication to the outside world but not the accuracy of signal processing. In addition, to minimize the oscillator error as the  $V_{DD}$  voltage changes, an on-chip regulator is used to supply the oscillator block.



### 2.5.1. Trimming the Oscillator

Settings for the Osc\_Trim bits in EEPROM fine-tune the oscillator frequency. See Table 3.5 for bit locations and Table 2.2 for possible settings. The default value is 0<sub>H</sub> to ensure communication on start-up.

**Important:** Optimal oscillator trimming is determined during wafer-level testing and final package testing, and this part-specific factory value, which can be copied to Osc\_Trim, is stored in bits in the CUST\_ID1 and CUST\_ID2 EEPROM bits for applications requiring optimal response time. In this case, see section 5 for important notes and instructions for copying these optimal values to the Osc\_Trim bits before calibration. It is strongly recommended that only the default value or the factory trim value be used because ZACwire™ communication is not guaranteed at different oscillator frequencies.

**Table 2.2 Oscillator Trimming**

Osc_Trim Bits	Delta Frequency (kHz)
100	+385
101	+235
110	+140
111	+65
000	Nominal
001	-40
010	-76
011	-110

Example: Programming 011<sub>B</sub> → the trimmed frequency = nominal value - 110 kHz.

### 2.6. Diagnostic Features

The ZSSC3008 offers a full suite of diagnostic features to ensure robust system operation in the most “mission-critical” applications. If the part is programmed in Ratiometric Output Mode, then diagnostic states are indicated by an output below 2.5% of VDD or above 97.5% of VDD. If the part is programmed in Digital Output Mode, then diagnostic states will be indicated by a transmission with a generated parity error. Diagnostics are not supported in 0-1V Output Mode.

Table 2.3 gives a summary of the diagnostic features, which are explained in detail in the following sections. EEPROM settings that control diagnostic functions are given in section 3.5.



**Table 2.3** Summary of Diagnostic Features

Detected Fault	Analog Diagnostic Level	ZACwire™ Diagnostic	Delay in Detection
EEPROM signature	Lower	Generates parity error	10ms after power-on
Loss of bridge positive	Upper	Generates parity error	2ms
Loss of bridge negative	Upper	Generates parity error	2ms
Open bridge connection	Upper	Generates parity error	2ms
Bridge input short	Upper	Generates parity error	2ms
Loss of VDD	Lower	Transmissions stop	Dependent on R <sub>L</sub> and C <sub>L</sub>
Loss of VSS	Upper	Transmissions stop	Dependent on R <sub>L</sub> and C <sub>L</sub>

### 2.6.1. EEPROM Integrity

The contents of the EEPROM are protected by an 8-bit LFSR signature (linear feedback shift register). This signature is regenerated and stored in EEPROM every time EEPROM contents are changed. This signature is generated and checked for a match after Power-On-Reset prior to entering Normal Operation Mode. If the generated signature fails to match, the part will output a diagnostic state on the output.

In addition to an extensive temporal and code interlock mechanism used to prevent false writes to the EEPROM, the ZSSC3008 offers an EEPROM lock mechanism for high-security applications. When EEPROM bits 105:103 are programmed with “011” or “110,” this 3-bit field will permanently disable the VPP charge pump and will not allow further writes to the EEPROM. See Table 2.3 in section 2.6 for more information.

### 2.6.2. Sensor Connection Check

Four dedicated comparators permanently check the range of the bridge inputs (BP/BN) to ensure they are within the envelope of 0.8V to 0.85\*VDD during all conversions. The two sensor inputs have a switched ohmic path to ground and if left floating, would be discharged. If any of the wires connecting the bridge break, this mechanism will detect it and put the ASIC in a diagnostic state. This same diagnostic feature can also detect a short between BP/BN. See Table 2.3 in section 2.6 for more information.

### 2.6.3. Sensor Short Check

If a short occurs between BP/BN (bridge inputs), it would normally produce an in-range output signal and therefore would not be detected as a fault. This diagnostic mode, if enabled, will deliberately look for such a short. After the measurement cycle of the bridge, it will deliberately pull the BP bridge input to ground for 4μsec. At the end of this 4μsec window, it will check to see if the BN input “followed” it down below the 0.8V comparator checkpoint. If so, a short must exist between BP/BN, and the part will output a diagnostic state. The bridge will have a minimum of 480μsec recovery time prior to the next measurement. See Table 2.3 in section 2.6 for more information.



#### 2.6.4. Power Loss Detection

If the power or GND connection to the module containing the sensor bridge and ASIC is lost, the ASIC will output a diagnostic state if a pull-up or pull-down terminating resistor greater than or equal to 5k $\Omega$  is connected in the final application. This diagnostic mode only works when the part is configured in Analog Output Mode. See Table 2.3 in section 2.6 for more information.

## 3 Functional Description

### 3.1. General Working Mode

The command/data transfer takes place via the one-wire SIG<sup>™</sup> pin using the ZACwire<sup>™</sup> serial communication protocol.

After power-on, the IC waits for 3ms (the command window) for the Start\_CM command.

Without this command, the Normal Operation Mode (NOM) starts. In this mode, raw bridge values are converted, and the corrected values are presented on the output in analog or digital format depending on the configuration stored in EEPROM.

Command Mode (CM) can only be entered during the 3ms command window after Power ON. If the IC receives the Start\_CM command during the command window, it remains in the CM. The CM allows changing to one of the other modes via command. After command Start\_RM, the IC is in the Raw Mode (RM). Without correction, the raw values are transmitted to the digital output in a predefined order. The RM can only be stopped by Power OFF. The RM is used by the calibration software for collection of raw bridge data so the correction coefficients can be calculated.

If diagnostic features are enabled and a diagnostic fault is detected, diagnostic states are indicated as follows depending on the programmed mode:

- In Analog Output Mode:  
Diagnostic states are indicated by an output below 2.5% of VDD or above 97.5% of VDD.
- In Digital Output Mode:  
Diagnostic states will be indicated by a transmission with a generated parity error.

For more details see section 2.6.

# ZSSC3008

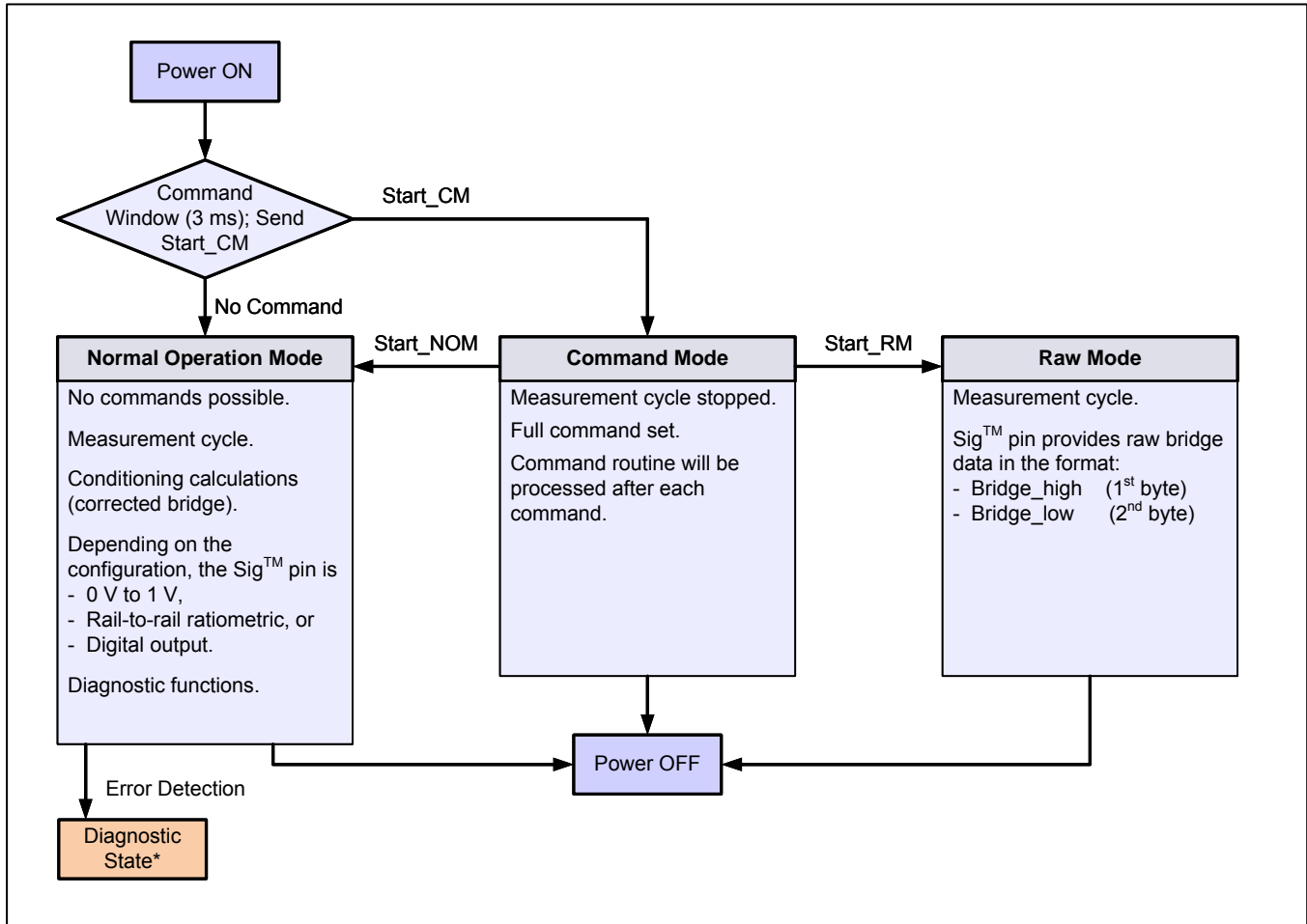
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**ZMDI**<sup>®</sup>

The Analog Mixed Signal Company



Figure 3.1 General Working Mode



\* See section 2.6.



### 3.2. ZACwire™ Communication Interface

#### 3.2.1. Properties and Parameters

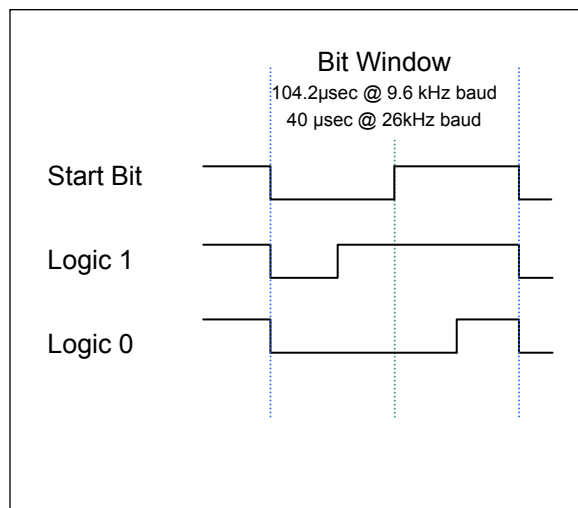
**Table 3.1 Pin Configuration and Latch-Up Conditions**

No.	Parameter	Symbol	Min	Typ	Max	Unit	Comments
1	Pull-up resistor (on-chip)	R <sub>ZAC,pu</sub>		30		kΩ	On-chip pull-up resistor switched on during Digital Output Mode and during Command Mode (first 3 ms after power up)
2	Pull-up resistor (external)	R <sub>ZAC,pu_ext</sub>	150			Ω	If the master communicates via a push-pull stage, no pull-up resistor is needed; otherwise, a pull-up resistor with a value of at least 150 Ω must be connected.
3	ZACwire™ rise time	T <sub>ZAC,rise</sub>			5	μs	Any user RC network included in Sig™ path must meet this rise time
4	ZACwire™ line resistance <sup>1)</sup>	R <sub>ZACload</sub>			3.9	kΩ	Also see section 1.3, Table 1.9.
5	ZACwire™ load capacitance <sup>1)</sup>	C <sub>ZAC,load</sub>	0	1	15	nF	Also see section 1.3, Table 1.9.
6	Voltage low level	V <sub>ZAC,low</sub>		0	0.2	V <sub>DD</sub>	Rail-to-rail CMOS driver
7	Voltage high level	V <sub>ZAC,high</sub>	0.8	1		V <sub>DD</sub>	Rail-to-rail CMOS driver

<sup>1)</sup> The rise time must be  $T_{ZAC,rise} = 2 * R_{ZACload} * C_{ZACload} \leq 5 \mu s$ . If using a pull-up resistor instead of a line resistor, it must meet this specification. The absolute maximum for C<sub>ZACload</sub> is 15nF.

#### 3.2.2. Bit Encoding

**Figure 3.2 Manchester Duty Cycle**



Start bit = 50% duty cycle used to set up strobe time

Logic 1 = 75% duty cycle

Logic 0 = 25% duty cycle

Stop Time

The ZACWire™ bus will be held high for 32μs (nominal) between consecutive data packets regardless of baud rate.

# ZSSC3008

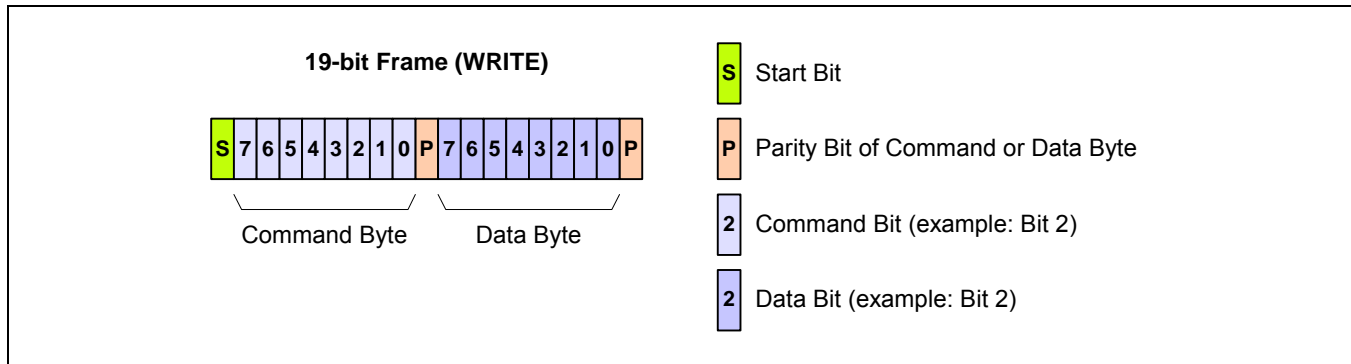
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### 3.2.3. Write Operation from Master to ZSSC3008

The calibration master sends a 19-bit packet frame to the IC.

**Figure 3.3 19-Bit Write Frame**



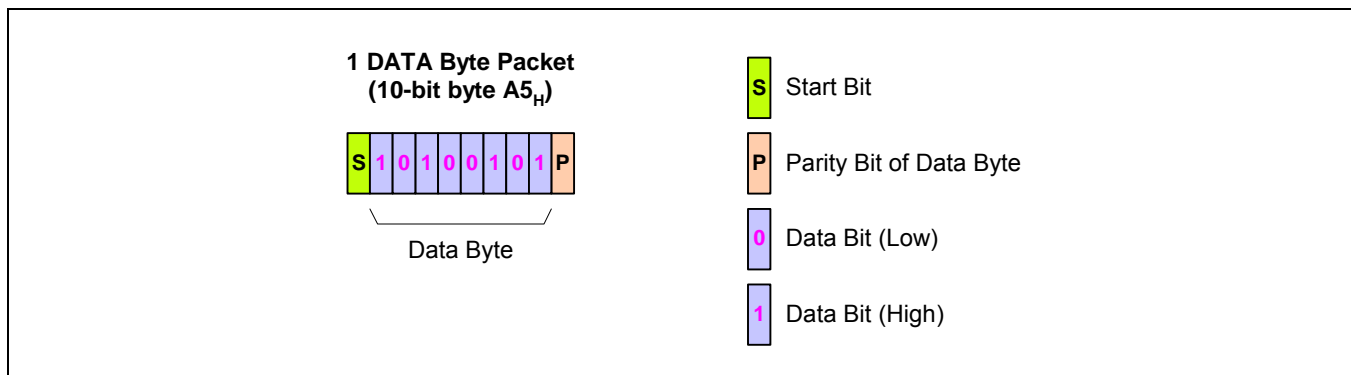
The incoming serial signal will be sampled at a 512 kHz clock rate. This protocol is very tolerant to clock skew, and can easily tolerate baud rates in the 6 kHz to 48 kHz range.

### 3.2.4. ZSSC3008 Read Operations

The incoming frame will be checked for proper parity on both command and data bytes, as well as for any edge time-outs prior to a full frame being received.

Once a command/data pair is received, the ZSSC3008 will perform that command. After the command has been successfully executed by the IC, the IC will acknowledge success by a transmission of an A5<sub>H</sub>-byte back to the master. If the master does not receive an A5<sub>H</sub> transmission within 130 ms of issuing the command, it must assume the command was either improperly received or could not be executed.

**Figure 3.4 Read Acknowledge**



# ZSSC3008

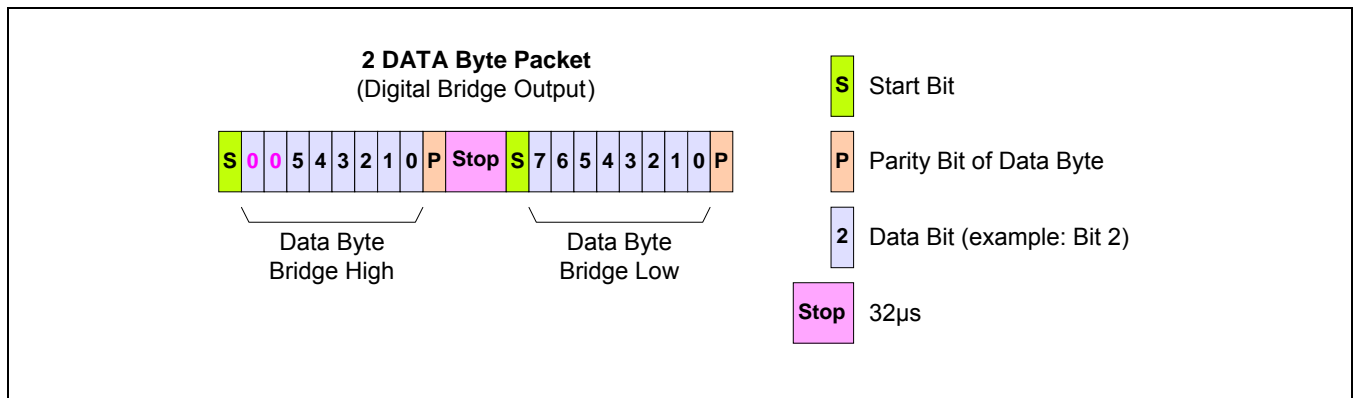
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The ZSSC3008 transmits 10-bit bytes (1 start bit, 8 data bits, 1 parity bit). During calibration and configuration, transmissions are normally either A5<sub>H</sub> or data. A5<sub>H</sub> indicates successful completion of a command.

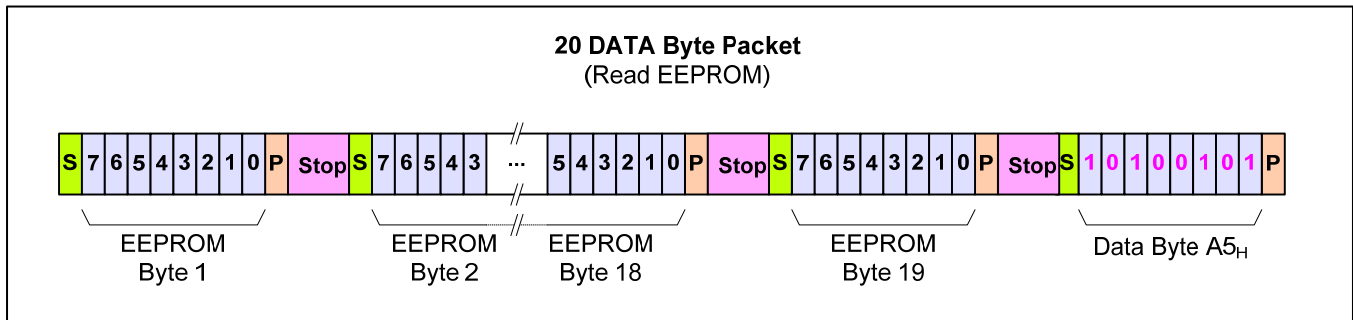
During Normal Operation Mode, if the part is configured for digital output of the bridge reading, it first transmits the high byte of bridge data, followed by the low byte. The bridge data is 14 bits in resolution, so the upper two bits of the high byte are always zero-padded. There is a 32 $\mu$ s stop time when the bus is held high between bytes in a packet.

**Figure 3.5 Digital Output (NOM) Bridge Readings**



The EEPROM transmission occurs in a packet with 20 data bytes, as shown in Figure 3.6.

**Figure 3.6 Read EEPROM Contents**



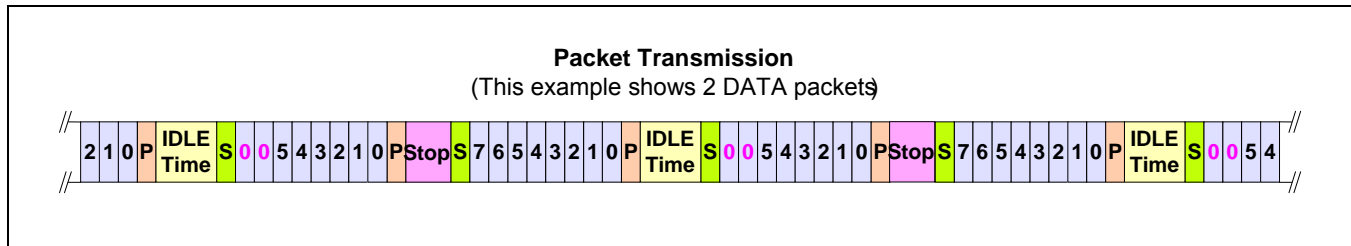
There is a variable idle time between packets. This idle time varies with the update rate setting in EEPROM.

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**Figure 3.7** Transmission of a Number of Data Packets



The table below shows the idle time between packets versus the update rate. This idle time can vary by a nominal +/-15% between parts and over a temperature range of -40°C to 125°C.

**Table 3.2** Special Measurement/Idle Time between Packets versus Update Rate

Update Rate Setting	Idle Time between Packets	Special Measurement
00	1ms	Every 128 bridge measurements
01	4.85ms	Every 64 bridge measurements
10	22.5ms	Every 16 bridge measurements
11	118ms	Every 8 bridge measurements

Transmissions from the IC occur at one of two speeds depending on the update rate programmed in EEPROM. If the user chooses one of the two fastest update rates (1 ms or 5 ms) then the baud rate of the digital transmission will be 32kHz (minimum 26kHz). If, however, the user chooses one of the two slower update rates (25ms or 125ms), then the baud rate of the digital transmission will be 8kHz (maximum 9.6kHz).

The total transmission time is shown in Table 3.3.

**Table 3.3** Total Transmission Time for Different Update Rate Settings

Update Rate	Baud Rate*	Idle Time	Transmission Time – Bridge Readings		
			20.5 bits	31.30µs	
1ms (1kHz)	32kHz	1.0ms	20.5 bits	31.30µs	1.64ms
5ms (200Hz)	32kHz	4.85ms	20.5 bits	31.30µs	5.49ms
25ms (40Hz)	8kHz	22.5ms	20.5 bits	125.00µs	25.06ms
125ms (8Hz)	8kHz	118.0ms	20.5 bits	125.00µs	120.56ms

\* Typical values. Minimum baud rate for 1 ms or 5 ms: 26kHz; maximum baud rate for 25 ms or 125 ms: 9.6kHz.

The 3rd column in Table 3.2 shows the timing for the special measurements in the different update rate modes.

For lower update rates, the output is followed by a power-down as shown in Figure 3.8.

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**Figure 3.8 ZACwire™ Output Timing for Lower Update Rates**

Calculation 160 $\mu$ s	ZACwire™ Output	Power Down (determined by Update Rate)	Power-On Settling 128 $\mu$ s	Settling Time 64 $\mu$ s	ADC Conversion 768 $\mu$ s	Calculation 160 $\mu$ s	ZACwire™ Output
----------------------------	--------------------	--	-------------------------------------	-----------------------------	-------------------------------	----------------------------	--------------------

It is easy to program any standard microcontroller to communicate with the ZSSC3008. ZMDI can provide sample code for a MicroChip PIC microcontroller.

### 3.2.5. High Level Protocol

The ZSSC3008 will listen for a command/data pair to be transmitted for the 3 ms after the de-assertion of its internal Power On Reset (POR). If a transmission is not received within this time frame, then it will transition to Normal Operation Mode (NOM). In the NOM, it will output bridge data in 0-1V analog, rail-to-rail ratiometric analog, or digital depending on how the part is currently configured.

If the ZSSC3008 receives a Start\_CM command within the first 3 ms after the de-assertion of POR, then it will go into Command Mode (CM). In this mode, calibration/configuration commands will be executed. The ZSSC3008 will acknowledge successful execution of commands by transmission of A5H. The calibrating/configuring master will know a command was not successfully executed if no response is received after 130ms of issuing the command. Once in command interpreting/executing mode, the ZSSC3008 will stay in this mode until power is removed or a Start NOM (Start Normal Operation Mode) command is received. The Start\_CM command is used as an interlock mechanism to prevent a spurious entry into Command Mode on power up. The first command received within the 3ms window of POR must be a Start\_CM command to enter into command interpreting mode. Any other commands will be ignored.



### 3.3. Command/Data Bytes Encoding

The 2-byte command sent to the ZSSC3008 consists of 1 byte of command information and 1 byte of data information. Regardless of whether the command requires data or not, 2 bytes MUST be sent. Table 3.4 lists all the command/data pairings. (X=don't care.)

**Table 3.4 Command/Data Bytes Encoding**

Command Byte	Data	Description																														
00 <sub>H</sub>	XX <sub>H</sub>	Read EEPROM command via SIG™ pin. <sup>†</sup>																														
20 <sub>H</sub>	5X <sub>H</sub>	DAC Ramp Test Mode. Gain_B[13:3] contains the starting point, and the increment is (Offset_B/8). The increment will be added every 125µsec.																														
30 <sub>H</sub>		Trim/Configure: 3 <sup>rd</sup> nibble determines what is trimmed/configured. The 4 <sup>th</sup> nibble is data to be programmed.																														
		<table border="1"> <thead> <tr> <th>3<sup>rd</sup> Nibble</th> <th>4<sup>th</sup> Nibble</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0<sub>H</sub></td> <td>Data</td> <td>Trim oscillator. Least significant 3 bits of data used.</td> </tr> <tr> <td>1<sub>H</sub></td> <td>Data</td> <td>Trim 1V reference. Least significant 4 bits of data used.</td> </tr> <tr> <td>2<sub>H</sub></td> <td>Data</td> <td>Offset Mode. Least significant 4 bits of data used.</td> </tr> <tr> <td>3<sub>H</sub></td> <td>Data</td> <td>Set output mode. Least significant 2 bits used.</td> </tr> <tr> <td>4<sub>H</sub></td> <td>Data</td> <td>Set update rate. Least significant 2 bits used.</td> </tr> <tr> <td>5<sub>H</sub></td> <td>Data</td> <td>Configure JFET regulation</td> </tr> <tr> <td>7<sub>H</sub></td> <td>Data</td> <td>Program EEPROM bits [99:96] (Pamp_Gain)</td> </tr> <tr> <td>D<sub>H</sub></td> <td>3<sub>H</sub> or 6<sub>H</sub></td> <td>Program EEPROM bits [105:103]: <b>EEPROM locked!</b> All others: EEPROM unlocked.</td> </tr> <tr> <td>E<sub>H</sub></td> <td>Data</td> <td>Program EEPROM bits [102:100] diag_cfg<sup>‡</sup></td> </tr> </tbody> </table>	3 <sup>rd</sup> Nibble	4 <sup>th</sup> Nibble	Description	0 <sub>H</sub>	Data	Trim oscillator. Least significant 3 bits of data used.	1 <sub>H</sub>	Data	Trim 1V reference. Least significant 4 bits of data used.	2 <sub>H</sub>	Data	Offset Mode. Least significant 4 bits of data used.	3 <sub>H</sub>	Data	Set output mode. Least significant 2 bits used.	4 <sub>H</sub>	Data	Set update rate. Least significant 2 bits used.	5 <sub>H</sub>	Data	Configure JFET regulation	7 <sub>H</sub>	Data	Program EEPROM bits [99:96] (Pamp_Gain)	D <sub>H</sub>	3 <sub>H</sub> or 6 <sub>H</sub>	Program EEPROM bits [105:103]: <b>EEPROM locked!</b> All others: EEPROM unlocked.	E <sub>H</sub>	Data	Program EEPROM bits [102:100] diag_cfg <sup>‡</sup>
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		5 <sub>H</sub>	Data	Configure JFET regulation																												
		7 <sub>H</sub>	Data	Program EEPROM bits [99:96] (Pamp_Gain)																												
D <sub>H</sub>	3 <sub>H</sub> or 6 <sub>H</sub>	Program EEPROM bits [105:103]: <b>EEPROM locked!</b> All others: EEPROM unlocked.																														
E <sub>H</sub>	Data	Program EEPROM bits [102:100] diag_cfg <sup>‡</sup>																														
40 <sub>H</sub>	00 <sub>H</sub>	Start NOM => Ends Command Mode; transition to Normal Operation Mode.																														
40 <sub>H</sub>	10 <sub>H</sub>	Start_RM = Start the Raw Mode (RM) In this mode, if Gain_B = 800H, then the digital output will simply be the raw values of the ADC for the Bridge reading.																														
50 <sub>H</sub>	90 <sub>H</sub>	Start_CM => Start the Command Mode; used to enter Command Interpret Mode.																														
60 <sub>H</sub>	YY <sub>H</sub>	Program SOT (2 <sup>nd</sup> Order Term)																														
80 <sub>H</sub>	YY <sub>H</sub>	Program Gain_B upper 7-bits (Set the MSB to 0.)																														
90 <sub>H</sub>	YY <sub>H</sub>	Program Gain_B lower 8-bits																														
A0 <sub>H</sub>	YY <sub>H</sub>	Program Offset_B upper 6-bits (Set the two MSBs to 0.)																														
B0 <sub>H</sub>	YY <sub>H</sub>	Program Offset_B lower 8-bits																														
08 <sub>H</sub>	YY <sub>H</sub>	Program Upper Clipping Limit (Set the MSB to 0.)																														

<sup>†</sup> For more details, refer to section 3.7.

<sup>‡</sup> For more details, refer to section 3.5.

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Command Byte	Data	Description
18 <sub>H</sub>	YY <sub>H</sub>	Program Lower Clipping Limit (Set the MSB to 0.)
28 <sub>H</sub>	YY <sub>H</sub>	Program Cust_ID0
38 <sub>H</sub>	YY <sub>H</sub>	Program Cust_ID1
48 <sub>H</sub>	YY <sub>H</sub>	Program Cust_ID2

## 3.4. Calibration Sequence

Although the ZSSC3008 can work with many different types of resistive bridges, assume a pressure bridge is being used for the following discussion on calibration.

Calibration essentially involves collecting raw bridge data from the IC for different known pressures. This raw data can then be processed by the calibration master (typically a PC) to compute the coefficients, and the calculated coefficients can then be written to the IC.

ZMDI can provide software and hardware with samples to perform the calibration.

### There are three main steps to calibration:

1. Assigning a unique identification to the IC. This identification is programmed in EEPROM and can be used as an index into the database stored on the calibration PC. This database will contain all the raw values of bridge readings for that part, as well as the known pressure (for this application) that the bridge was exposed to. This unique identification can be stored in a concatenation of the following EEPROM registers: Cust\_ID0, Cust\_ID1, Cust\_ID2. These registers can also form a permanent serial number.
2. Data collection. Data collection involves getting raw data from the bridge at different known pressures. This data is then stored on the calibration PC using the unique identification of the IC as the index to the database.
3. Coefficient calculation and write. Once enough data points have been collected to calculate all the desired coefficients then the coefficients can be calculated by the calibrating PC and written to the IC.

### Step 1 – Assigning Unique Identification

Assigning a unique identification number is as simple as using the commands Program Cust\_ID0, Program Cust\_ID1 and Program Cust\_ID2. These three 8-bit registers allow for more than 16 million unique devices. Gain\_B must be programmed to 800<sub>H</sub> (unity).

### Step 2 – Data Collection

The number of unique pressure points that calibration must be performed at depends on the customer's needs. The minimum number of calibration points required is two or three, depending on the precision desired and the behavior of the resistive bridge in use.

- 2-point calibration can be used if only a gain and offset term are needed.
- 3-point calibration can be used to also obtain 2<sup>nd</sup> order correction.

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To acquire raw data from the part, set ZSSC3008 to enter Raw Mode. This is done by issuing a Start\_CM (Start Command Mode 5090H) command/data pair to the IC followed by a Start\_RM (Start Raw Mode 4010<sub>H</sub>) command/data pair with the LSB of the upper data nibble set. Now if the Gain\_B term has been set to unity (800<sub>H</sub>), then the part will be in the Raw Mode and will output raw data on its SIG<sup>TM</sup> pin instead of corrected bridge data. Capture several of these data points with the user's calibration system (capturing 16 is recommended) and average them. Store these raw data in the database along with the known pressure. The output format during Raw Mode is Bridge\_High, Bridge\_Low. Each of these is an 8-bit quantity. The upper 2-bits of Bridge\_High are zero filled.

### Step 3 – Coefficient Calculations

The math to perform the coefficient calculation is very complicated and will not be discussed in detail. There is a rough overview of the coefficients in the “Calibration Math” section 3.6. ZMDI will provide software to perform the coefficient calculation. After the coefficients are calculated, the final step is to write them to the EEPROM of the ZSSC3008.



### 3.5. EEPROM Bits

Table 3.5 shows the bit order and default settings for the EEPROM, which are programmed through the serial interface. See section 5 for important information for die/wafer customers.

**Table 3.5 ZSSC3008 EEPROM Bits**

EEPROM Range	Description	Default Settings	Notes
2:0	Osc_Trim	0 <sub>H</sub> This default setting minimizes risk of communication failure on start-up. (Actual part-specific factory values for Osc_Trim are initially stored in bits in CUST_ID1 and CUST_ID2 for applications requiring optimal response time. See section 5 for important notes.)	See section 2.5 for details on oscillator trim. 100 => Fastest 101 => 3 clicks faster than nominal 110 => 2 clicks faster than nominal 111 => 1 click faster than nominal 000 => Nominal 001 => 1 click slower than nominal 010 => 2 clicks slower than nominal 011 => Slowest
6:3	1V_Trim/JFET_Trim	SSSS <sub>BIN</sub> where "s" is the part-specific factory bit setting for the reference voltage trim value. (Back-up copies are stored in CUST_ID0 for applications requiring accurate references. See section 5 for important notes.)	See Table 2.1 in the "Voltage Reference Block" section.
10:7	A2D_Offset	3 <sub>H</sub>	The upper two bits are flip polarity and invert bridge input (negative gain) respectively. If both are used in conjunction, negative offset modes can be achieved. 00 => normal polarity, positive gain 01 => normal polarity, negative gain 10 => flip polarity, positive gain 11 => flip polarity, negative gain The lower two bits form the ADC offset selection. Offset selection: 11 => [-1/2, 1/2] mode bridge inputs 10 => [-1/4, 3/4] mode bridge inputs 01 => [-1/8, 7/8] mode bridge inputs 00 => [-1/16, 15/16] mode bridge inputs

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EEPROM Range	Description	Default Settings	Notes
12:11	Output_Select	2 <sub>H</sub>	00 => <b>NOT recommended!</b> Digital (3 bytes with parity) Bridge High {00,[5:0]}, Bridge Low [7:0] 3 <sup>rd</sup> Byte =00 <sub>H</sub> 01 => 0-1V Analog (requires 1kHz update rate) 10 => Rail-to-Rail Ratiometric (requires 1kHz update rate) 11 => Digital (2 bytes with parity) Bridge High {00,[5:0]} Bridge Low [7:0]
14:13	Update_Rate	2 <sub>H</sub>	00 => 1 msec (1kHz) 01 => 5 msec (200Hz) 10 => 25 msec (40Hz) 11 => 125 msec (8 Hz)
16:15	JFET_cfg	3 <sub>H</sub>	00 => No JFET regulation (lower power) 01 => No JFET regulation (lower power) 10 => JFET regulation centered around 5.0V 11 => JFET regulation centered around 5.5V (i.e., over-voltage protection)
31:17	Gain_B	198 <sub>H</sub>	Bridge Gain (also see bits 10:7): Gain_B[14] => multiply x 8 Gain_B[13:0] => 14-bit unsigned number representing a number in the range [0,8)
45:32	Offset_B	0 <sub>H</sub>	Unsigned 14-bit offset for bridge correction
87:46	Reserved	0 <sub>H</sub>	Program to 0.
95:88	SOT	0 <sub>H</sub>	2 <sup>nd</sup> Order Term. This term is a 7-bit magnitude with sign. SOT[7] = 1 → negative SOT[7] = 0 → positive SOT[6:0] = magnitude [0-127]
99:96	Pamp_Gain	1 <sub>H</sub>	Bits [99:96] = Pre-Amp Gain 0000 => 6 0001 => 24 (default setting) 0010 => 48 0011 => 96 All others prohibited
102:100	Diag_cfg	7 <sub>H</sub>	This 3-bit term applies to diagnostic features Diag_cfg[2] → enable output short circuit protection. Diag_cfg[1] → enable sensor short checking. Diag_cfg[0] → enable sensor connection checking.
105:103	EEPROM_Lock	0 <sub>H</sub>	EEPROM lock 011 or 110 => locked All other => unlocked  When EEPROM is locked, the internal charge pump is disabled and the EEPROM can never be programmed again.

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EEPROM Range	Description	Default Settings	Notes
112:106	Up_Clip_Lim	7F <sub>H</sub>	7-bit value used to select an upper clipping limit for the output. It affects both analog and digital output. The 14-bit upper clipping limit value is comprised of {11,Up_Clip_Lim[6:0],11111}. 127 different clipping levels are selectable between 75.19% and 100% of VDD.
119:113	Low_Clip_Lim	0 <sub>H</sub>	7-bit value used to select a lower clipping limit for the output. It affects both analog and digital output. The 14-bit lower clipping limit value is comprised of {00,Low_Clip_Lim[6:0],00000}. 127 different clipping levels are selectable between 0% and 24.8% of VDD.
127:120	Cust_ID0	SS <sub>BIN</sub> where "s" is a part-specific factory bit setting. During factory testing, two back-up copies of the optimal setting for the 1V_Trim/JFET_Trim bits are stored in [123:120] and in [127:124]. See important notes in section 5.	Customer ID byte 0 Can be used to store a customer part identification number. Caution: If the application requires accurate voltage references, do not overwrite this byte until completing the procedures in section 5.
135:128	Cust_ID1	xSSS xSSS <sub>BIN</sub> where "s" is a part-specific factory bit setting and x is "don't care." During factory testing, two copies of the optimal setting for the Osc_Trim bits are stored in [130:128] and in [134:132]. (Also in Cust_ID2.) See important notes in section 5.	Customer ID byte 1 Can be used to store a customer part identification number. Caution: If the application requires optimal response time, do not overwrite this byte until completing the procedures in section 5.

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EEPROM Range	Description	Default Settings	Notes
143:136	Cust_ID2	XXXX XSSSBIN where "s" is a part-specific factory bit setting and X is "don't care." During factory testing, a copy of the optimal setting for the Osc_Trim bits is stored in [138:136]. (Also in Cust_ID1.) See important notes in section 5.	Customer ID byte 2 Can be used to store a customer part identification number. Caution: If the application requires optimal response time, do not overwrite this byte until completing the procedures in section 5.
151:144	Signature		8-bit EEPROM signature. Generated through a linear feedback shift register (LFSR). This signature is checked on power-on to ensure integrity of EEPROM contents.

## 3.6. Calibration Math

### 3.6.1. Correction Coefficients

All terms are calculated external to the IC and then programmed to the EEPROM through the serial interface.

**Table 3.6 Correction Coefficients**

Coefficient	Description
Gain_B	Gain term used to compensate span of Bridge reading
Offset_B	Offset term used to compensate offset of Bridge reading
SOT	Second Order Term( SOT) for bridge measurement

### 3.6.2. Interpretation of Binary Numbers for Correction Coefficients

BR\_Raw should be interpreted as an unsigned number in the set [0, 16383] with a resolution of 1.



### 3.6.2.1. Gain\_B Interpretation

Gain\_B should be interpreted as a number in the set [0, 64]. The MSB (bit 14) is a scaling bit that will multiply the effect of the Gain\_B[13:0] term by 8. The remaining bits Gain\_B[13:0] represent a number in the range of [0,8) with Gain\_B[13] having a weighting of 4, and each subsequent bit has a weighting of ½ the previous bit.

**Table 3.7 Gain\_B [13:0] Weightings**

Bit Position	Weighting
13	$2^2 = 4$
12	$2^1 = 2$
11	$2^0 = 1$
10	$2^{-1}$
...	...
3	$2^{-8}$
2	$2^{-9}$
1	$2^{-10}$
0	$2^{-11}$

Examples:

The binary number:  $010010100110001_B = 4.6489$ ; Gain\_B[14] is 0<sub>B</sub>, so the number represented by Gain\_B[13:0] is not multiplied by 8.

The binary number:  $101100010010110_B = 24.586$ ; Gain\_B[14] is 1<sub>B</sub>, so the number represented by Gain\_B[13:0] is multiplied by 8.

### 3.6.2.2. Offset\_B Interpretation

Offset\_B is a 14-bit unsigned binary number. The MSB has a weighting of 8192. The following bits then have a weighting of: 4096, 2048, 1024 ...

**Table 3.8 Offset\_B Weightings**

Bit Position	Weighting
13	8192
12	4096
11	2048
.	
.	
.	
1	$2^1 = 2$
0	$2^0 = 1$

For example, the binary number 1111 1111 1100 = 4092.

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### 3.6.2.3. SOT Interpretation

SOT is a 2<sup>nd</sup> order term that applies to bridge non-linearity correction.

- Resolution: 0.25% @ Full Scale
- Range: +25% @ Full Scale to -25% @ Full Scale  
(Saturation in internal arithmetic will occur at greater negative non-linearities.)

## 3.7. Reading EEPROM Contents

The contents of the entire EEPROM memory can be read out using the Read EEPROM command (00<sub>H</sub>). This command causes the IC to output consecutive bytes on the ZACwire™. After each transmission, the EEPROM contents are shifted by 8 bits. The bit order of these bytes is given in Table 3.9.

**Table 3.9 EEPROM Read Order**

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Byte 1	Offset_B[7:0]							
Byte 2	RESERVED		Offset_B[13:8]					
Byte 3	RESERVED							
Byte 4								
Byte 5								
Byte 6								
Byte 7								
Byte 8	SOT[7:0]							
Byte 9	EEPROM_Lock[0]	Diag_cfg[2:0]			Pamp_Gain[3:0]			
Byte 10	Up_Clip_Lim[5:0]					EEPROM_Lock[2:1]		
Byte 11	Low_Clip_Lim[6:0]							Up_Clip_Lim[6]
Byte 12	Cust_ID0[7:0]							
Byte 13	Cust_ID1[7:0]							
Byte 14	Cust_ID2[7:0]							
Byte 15	Signature[7:0]							
Byte 16	A2D_Offset[0]	1V_Trim[3:0] *				Osc_Trim[2:0] *		
Byte 17	JFET_cfg[0]	Update_Rate[1:0]	Output_Select[1:0]		A2D_Offset[3:1]			
Byte 18	Gain_B[6:0]							JFET_cfg[1]
Byte 19	Gain_B[14:7]							
Byte 20	A5 <sub>H</sub>							

\* 1V\_Trim/JFET\_Trim



## 4 Application Circuit Examples

The minimum output analog load resistor is  $R_L = 5k\Omega$ . This optional load resistor can be configured as a pull-up or pull-down. If it is configured as a pull-down, it cannot be part of the module to be calibrated because this would prevent proper operation of the ZACwire™. If a pull-down load is desired, it must be added to the system after module calibration.

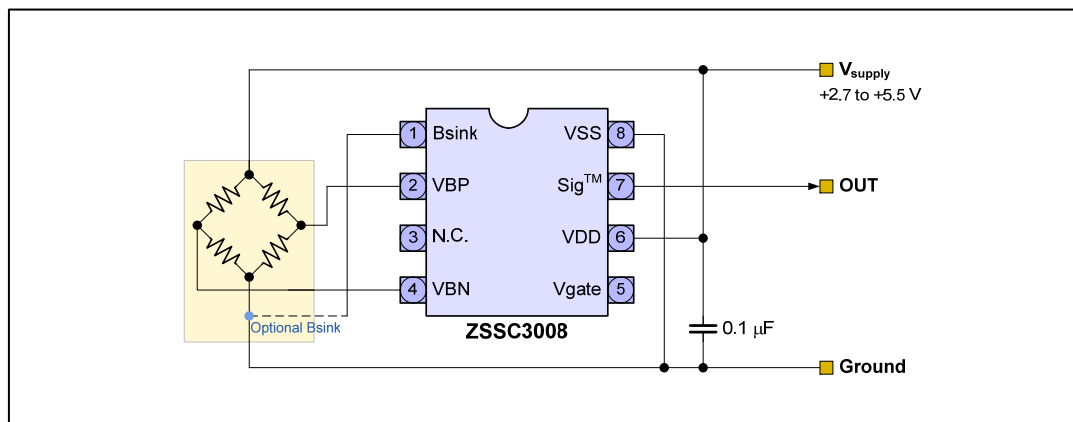
There is no output load capacitance needed.

Applicable EEPROM contents: Output\_Select, JFET\_cfg, 1V\_Trim/JFET\_Trim.

### 4.1. Three-Wire Rail-to-Rail Ratiometric Output

This example shows an application circuit for rail-to-rail ratiometric voltage output configuration. The same circuitry is applicable for a 0 to 1V absolute analog output.

**Figure 4.1 Rail-to-Rail Ratiometric Voltage Output**



The optional bridge sink allows a power savings of bridge current. The output voltage can be either

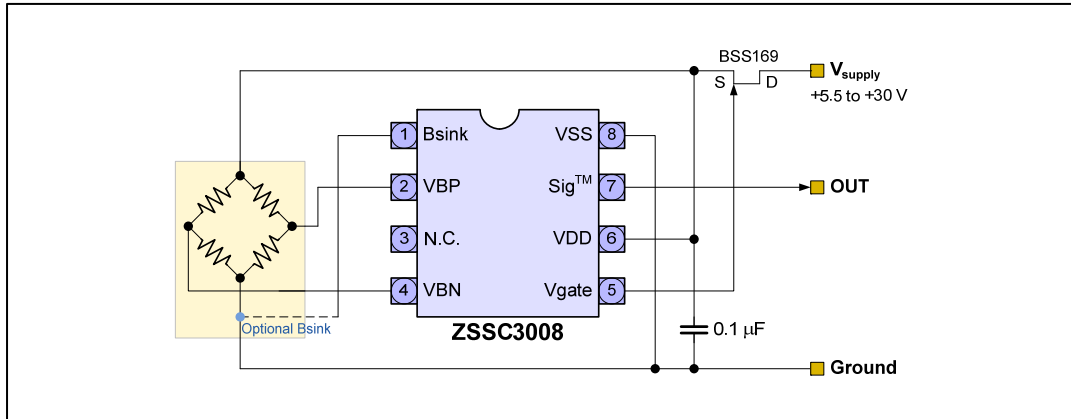
- Rail-to-rail analog output ratiometric to  $V_{DD}$  ( $V_{supply}$ ).
- 0 to 1V absolute analog output. The absolute voltage output reference is trimmable 1V ( $\pm 3mV$ ) in the 1V Output Mode via a 4-bit EEPROM field. (See section 2.4.3).



### 4.2. Absolute Analog Voltage Output

Figure 4.2 shows an application circuit for an absolute voltage output configuration and external JFET regulation for all industry standard applications.

**Figure 4.2 Absolute Analog Voltage Output with External JFET Regulation**



The output signal range can be one of the following options:

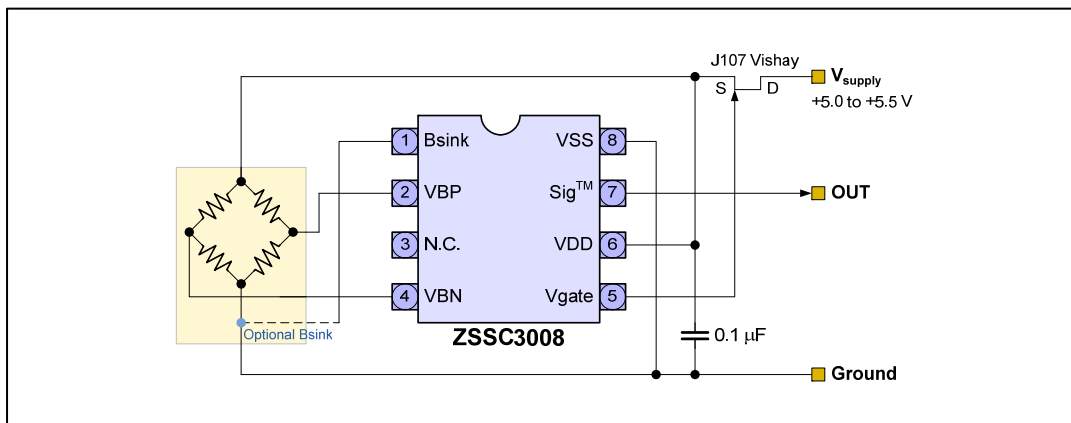
- 0 to 1 V analog output. The absolute voltage output reference is trimmable: 1 V (+/-3 mV) in the 1 V Output Mode via a 4-bit EEPROM field (see section 2.4.3).
- Rail-to-rail analog output. The on-chip reference for the JFET regulator block is trimmable: 5 V ( $\pm 15$  mV) in the Ratiometric Output Mode via a 4-bit EEPROM field. (See section 2.4.3).



### 4.3. Three-Wire Ratiometric Output with Over-Voltage Protection

The figure below shows an application circuit for a ratiometric output. In this application, the JFET is used for voltage protection. JFET\_cfg (16:15) in the EEPROM are configured to 5.5V. There is an additional maximum error of 8mV caused by the non-zero  $r_{ON}$  of the limiter JFET.

**Figure 4.3 Ratiometric Output**



### 4.4. Digital Output

For all three circuits, the output bridge signal can also be digital. For the digital output, no load resistor or load capacity is necessary. No pull down resistor is allowed. If a line resistor or pull-up resistor is used, the requirement for the rise time must be met ( $\leq 5\mu\text{s}$ ). The IC output includes an internal pull up resistor of about 30k $\Omega$ . The digital output can easily be read by firmware from a microcontroller, and ZMDI can provide the customer with software for developing the interface.

### 4.5. Output Resistor/Capacitor Limits

The limits for external components depend on the programmed output mode:

- Pure Analog Output Mode (calibration is done before): The only limit is the minimum load resistance of 5k $\Omega$ .
- Pure Digital Output Mode with end-of-line calibration: The RC time constant of the ZACwire™ line must have a rise time  $\leq 5\mu\text{s}$ .
- Analog output with digital communication during calibration: The RC time constant of the ZACwire™ line must have a rise time  $\leq 5\mu\text{s}$ .

**Warning:** Any series line resistance forms a voltage divider in conjunction with the pull-up load device. If a series line resistance is needed, choose a low value relative to the pull-up load device.



## 5 EEPROM Restoration

If needed, the default settings for the ZSSC3008 (see Table 3.5) can be reprogrammed as described in section 3. The following sections describe EEPROM content validation and handling during and/or after system assembly.

**Important:** During the sawing and dicing process, there is a possibility of the EEPROM contents flipping, and prevention cannot be guaranteed. This is primarily a concern for the factory trim settings, which are customized to each part.

The EEPROM default values programmed during the different test levels have been selected so that customer has the option to refresh/reprogram trim bits that might have flipped during sawing or dicing.

**Important:** The EEPROM lock is stored in the bit range 105:103. A value of 6<sub>H</sub> or 3<sub>H</sub> will lock the EEPROM forever by disabling the charge pump needed for EEPROM writing. The complete contents can also be validated using the EEPROM signature stored in bits [151:144], (see “Signature” in Table 3.5).

### 5.1. Default EEPROM Contents

During the wafer level test (wafer/dice delivery) and during final test for SOP8 packaged parts, the EEPROM is programmed with the default values listed in the Table 3.5.

During the wafer level test, the Osc\_trim bits [2:0] and 1V\_Trim/JFET\_Trim trim bits [6:3] are set to die-specific values.

#### 5.1.1. Osc\_Trim

The oscillator frequency is trimmed to a value of 512kHz±20% using the Osc\_Trim bit setting. The 3-bit setting is copied twice to Cust\_ID1[134:132] and [130:128] and then a third time to Cust\_ID2[138:136] to ensure the factory settings are retained so that the customer can reprogram these values in the Osc\_Trim bit if needed. Based on the most probable trimming, the default values for the Osc\_Trim bits are always set to 0<sub>H</sub> during factory testing to guarantee communication even if bits have flipped.

#### 5.1.2. 1V\_Trim/JFET\_Trim

The 5V reference for the JFET regulation is factory trimmed during the final test to 5V±15mV using the 1V\_Trim/JFET\_Trim bit setting. The 4-bit setting stored in EEPROM bits [6:3] is copied twice to the Cust\_ID0 bits [127:124] and [123:120] to ensure the factory settings are retained so that the customer can reprogram these values in the 1V\_Trim/JFET\_Trim bits if needed.

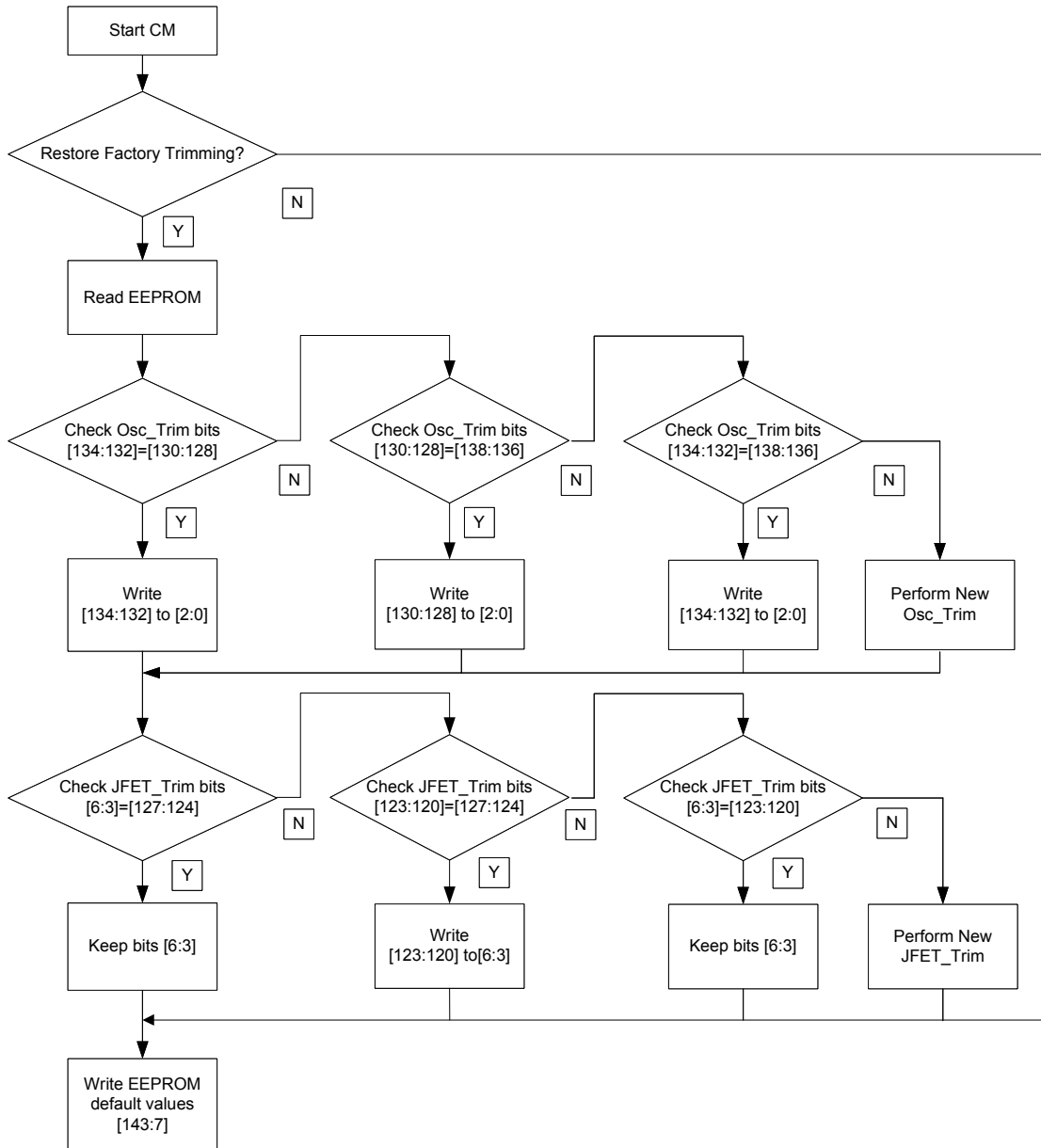
### 5.2. EEPROM Restoration Procedure

After module assembly, the EEPROM content should be refreshed. If JFET regulation is not used for the customer's application and optimized response time is not an important criterion, write the default values shown in Table 3.5 to the EEPROM bit range [143:7] and retain the existing values in the bit range [6:0]. If JFET regulation or optimized response time is required, the bit restoration procedure shown in the flow chart in Figure 5.1 must be used to keep the factory settings programmed during the testing. If customer oscillator trimming is required, see *ZSSC3008\_Tech\_Notes\_JFET\_and\_Osc\_Trimming\_revX.X.pdf* for instructions.)

Note: The EEPROM signature is re-calculated and updated after every EEPROM writing.



**Figure 5.1** EEPROM Validation and Restoration Procedure





## 6 Pin Configuration and Package

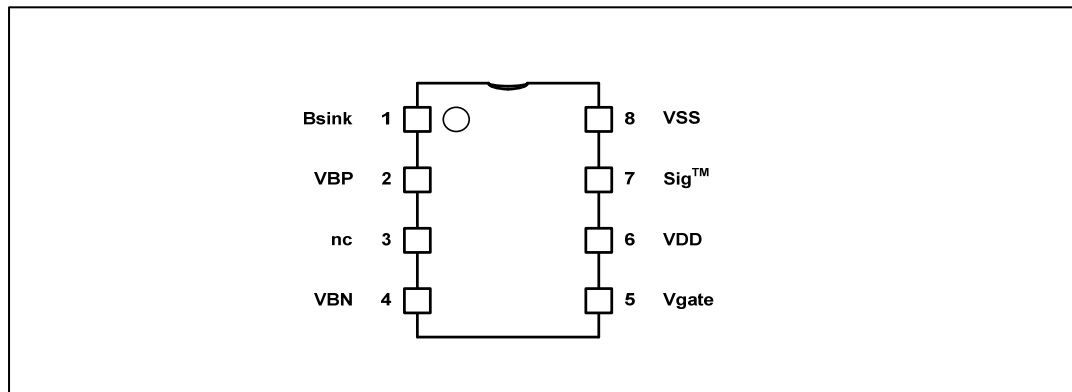
The standard package of the ZSSC3008 is an SOP-8 (3.81 mm / 150 mil body) with a lead-pitch 1.27 mm / 50 mil.

**Table 6.1 Storage and Soldering Conditions**

Storage and Soldering for the SOP-8 Package						
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Maximum Storage Temperature Less than 10hrs Before Mounting	$T_{\max\_storage}$				150	°C
Minimum Storage Temperature:	$T_{\min\_storage}$	Store in original packing only	-50			°C
Maximum Dry-Bake Temperature	$T_{drybake}$	Less than 100 hrs total, before mounting			125	°C
Soldering Peak Temperature	$T_{peak}$	Less than 30s (IPC/JEDEC-STD-020 Standard)			260	°C

Note: Also see Table 6.1 regarding other storage conditions.

**Figure 6.1 ZSSC3008 Pin-Out Diagram**



**Table 6.2 ZSSC3008 Pin Configuration**

Pin No.	Name	Description
1	Bsink	Optional ground connection for bridge ground. Used for power savings.
2	VBP	Positive bridge connection
3	nc	No connection
4	VBN	Negative bridge connection
5	Vgate	Gate control for external JFET regulation/over-voltage protection
6	VDD	Supply voltage (2.7 to 5.5 V)
7	Sig™	ZACwire™ interface (analog out, digital out, calibration interface)
8	VSS	Ground supply

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## 7 ESD/Latch-Up-Protection

All pins have an ESD protection of >4000V and a latch-up protection of  $\pm 100$  mA or of +8V/ -4V (to VSS/VSSA). ESD protection referenced to the Human Body Model is tested with devices in SOP-8 packages during product qualification. The ESD test follows the Human Body Model with 1.5k $\Omega$ /100pF based on MIL 883, Method 3015.7.

## 8 Test

The test program is based on this datasheet. The final parameters which will be tested during series production are listed in the tables of section 1.

The digital part of the IC includes a scan path, which can be activated and controlled during wafer test. Further test support for testing of the analog parts on wafer level is included in the DSP.

## 9 Quality and Reliability

A reliability qualification according to the in-house non-automotive standard has been performed.

## 10 Customization

For high-volume applications, which require an upgraded or downgraded functionality compared to the ZSSC3008, ZMDI can customize the circuit design by adding or removing certain functional blocks.

For this customization, ZMDI has a considerable library of sensor-dedicated circuitry blocks, which enable ZMDI to provide a custom solution quickly. Please contact ZMDI for further information.

## 11 Product Ordering Codes

Please contact ZMDI Sales for additional options.

Sales Code	Description	Package
ZSSC3008AA2R	ZSSC3008 SOP8 (150 mil) — Temperature range: -40°C to +125°C	Tape and Reel
ZSSC3008AA2T	ZSSC3008 SOP8 (150 mil) — Temperature range: -40°C to +125°C	Tube
ZSSC3008KIT	ZSSC3008 SSC Evaluation Kit: Communication Board, SSC Board, Sensor Replacement Board, Evaluation Software, USB Cable, 5 IC Samples	Kit

Contact ZMDI Sales for support and sales of ZMDI's ZSSC3008 Mass Calibration System.

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## 12 Related Documents

Document	File Name
ZSSC3008 Development Kit Documentation	ZSSC3008_Development_Kit_revX.X.pdf
ZSSC3008 Application Notes – In-Circuit Programming Boards	ZSSC3008_App_Notes_In-Circuit_Programming_rev X.X.pdf
ZSSC3008 Die Dimensions and Pad Coordinates	ZSSC3008_Tech_Notes_Die_Pads_revX.X.pdf

Visit ZMDI's website [www.zmdi.com](http://www.zmdi.com) or contact your nearest sales office for the latest version of these documents.

## 13 Definitions of Acronyms

Term	Description
ADC	Analog-to-Digital Converter
AFE	Analog Front-End
BUF	Buffer
CM	Command Mode
CMC	Calibration Microcontroller
DAC	Digital-to-Digital Converter
DNL	Differential Nonlinearity
DSP	Digital Signal Processor
DUT	Device Under Test
ESD	Electrostatic Discharge
FSO	Full-Scale Output
INL	Integrated Nonlinearity
LFSR	Linear Feedback Shift Register
LSB	Least Significant Bit
MUX	Multiplexer
NOM	Normal Operation Mode
OWI	One-Wire Interface
POC	Power-On Clear
POR	Power-On Reset Level
PSRR	Power Supply Rejection Ratio
RM	Raw Mode
SOT	Second Order Term
SSC	Sensor Signal Conditioner

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## 14 Document Revision History

Revision	Date	Description
1.00	February 18, 2011	First release.
1.10	May 5, 2011	Revised minimum temperature from -50°C to -40°C. Revised product ordering code for ZSSC3008 with -40°C to +125°C operating range from ZSSC3008AI2R to ZSSC3008AA2R. Minor revision to product description. Minor edit to section 9.
1.11	June 14, 2011	Update to section 9.

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