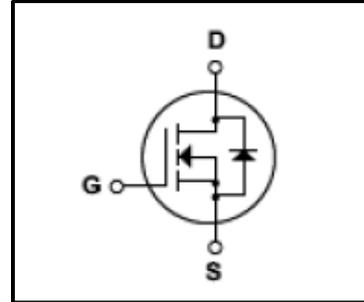


Silicon N-Channel MOSFET

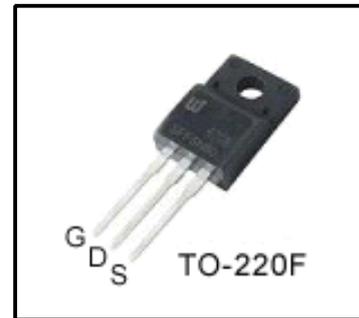
Features

- 4A,600V, $R_{DS(on)}$ (Max 2.5 Ω)@ $V_{GS}=10V$
- Ultra-low Gate Charge(Typical 16nC)
- Fast Switching Capability
- 100%Avalanche Tested
- Isolation Voltage($V_{ISO}=4000V$ AC)
- Maximum Junction Temperature Range(150 $^{\circ}C$)



General Description

This Power MOSFET is produced using Winsemi's advanced planar stripe, VDMOS technology. This latest technology has been especially designed to minimize on-state resistance, have a high rugged avalanche characteristics. This device is specially well suited for half bridge and full bridge resonant topology line a electronic lamp ballast.



Absolute Maximum Ratings

Symbol	Parameter	Value	Units
V_{DSS}	Drain Source Voltage	600	V
I_D	Continuous Drain Current(@ $T_c=25^{\circ}C$)	4*	A
	Continuous Drain Current(@ $T_c=100^{\circ}C$)	2.5*	A
I_{DM}	Drain Current Pulsed (Note1)	16*	A
V_{GS}	Gate to Source Voltage	± 30	V
E_{AS}	Single Pulsed Avalanche Energy (Note2)	240	mJ
E_{AR}	Repetitive Avalanche Energy (Note1)	10	mJ
dv/dt	Peak Diode Recovery dv /dt (Note3)	4.5	V/ ns
P_D	Total Power Dissipation(@ $T_c=25^{\circ}C$)	33	W
	Derating Factor above 25 $^{\circ}C$	0.26	W/ $^{\circ}C$
T_J, T_{stg}	Junction and Storage Temperature	-55~150	$^{\circ}C$
T_L	Channel Temperature	300	$^{\circ}C$

*Drain current limited by maximum junction temperature

Thermal Characteristics

Symbol	Parameter	Value			Units
		Min	Typ	Max	
R_{QJC}	Thermal Resistance , Junction -to -Case	-	-	3.79	$^{\circ}C/W$
R_{QJA}	Thermal Resistance , Junction-to -Ambient	-	-	62.5	$^{\circ}C/W$

Electrical Characteristics(Tc=25 °C)

Characteristics	Symbol	Test Condition	Min	Type	Max	Unit	
Gate leakage current	I _{GSS}	V _{GS} =±30V,V _{DS} =0V	-	-	±100	nA	
Gate-source breakdown voltage	V _{(BR)GSS}	I _G =±10 μA,V _{DS} =0V	±30	-	-	V	
Drain cut -off current	I _{DSS}	V _{DS} =600V,V _{GS} =0V	-	-	10	μA	
		V _{DS} =480V,Tc=125 °C	-	-	100	μA	
Drain -source breakdown voltage	V _{(BR)DSS}	I _D =250 μA,V _{GS} =0V	600	-	-	V	
Gate threshold voltage	V _{GS(th)}	V _{DS} =10V,I _D =250 μA	2	-	4	V	
Drain -source ON resistance	R _{DS(ON)}	V _{GS} =10V,I _D =3.25A	-	1.8	2.5	Ω	
Input capacitance	C _{iss}	V _{DS} =25V, V _{GS} =0V, f=1MHz	-	545	670	pF	
Reverse transfer capacitance	C _{rss}		-	7	10		
Output capacitance	C _{oss}		-	70	90		
Switching time	Rise time	t _r	V _{DD} =300V, I _D =4.4A, R _G =25Ω, (Note4,5)	-	10	30	ns
	Turn-on time	t _{on}		-	35	80	
	Fall time	t _f		-	45	100	
	Turn-off time	t _{off}		-	20	50	
Total gate charge(gate-source plus gate-drain)	Q _g	V _{DD} =480V, V _{GS} =10V, I _D =4.4A (Note4,5)	-	16	20	nC	
Gate-source charge	Q _{gs}		-	3.4	-		
Gate-drain("miller") Charge	Q _{gd}		-	7	-		

Source-Drain Ratings and Characteristics(Ta=25 °C)

Characteristics	Symbol	Test Condition	Min	Type	Max	Unit
Continuous drain reverse current	I _{DR}	-	-	-	4	A
Pulse drain reverse current	I _{DRP}	-	-	-	17.6	A
Forward voltage(diode)	V _{DSF}	I _{DR} =4.4A,V _{GS} =0V	-	-	1.4	V
Reverse recovery time	t _{rr}	I _{DR} =4.4A,V _{GS} =0V, dI _{DR} / dt =100 A / μs	-	390	-	ns
Reverse recovery charge	Q _{rr}		-	2.2	-	μC

Note 1.Repeativity rating :pulse width limited by junction temperature

2.L=18.5mH I_{AS}=4.4A,V_{DD}=50V,R_G=0Ω ,Starting T_J=25 °C

3.I_{SD}≤4A,di/dt≤200A/us,V_{DD}<BV_{DSS},STARTING T_J=25 °C

4.Pulse Test:Pulse Width≤300us,Duty Cycle≤2%

5. Essentially independent of operating temperature.

This transistor is an electrostatic sensitive device

Please handle with caution

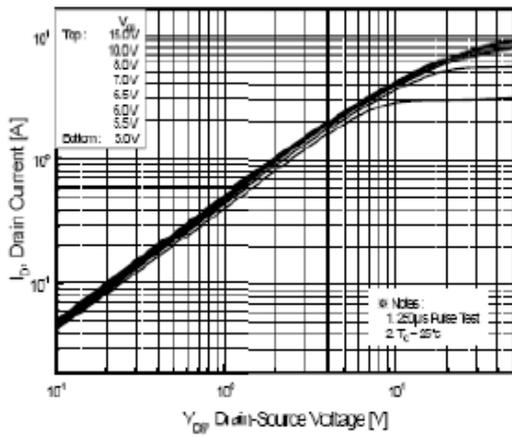


Fig.1 On-State Characteristics

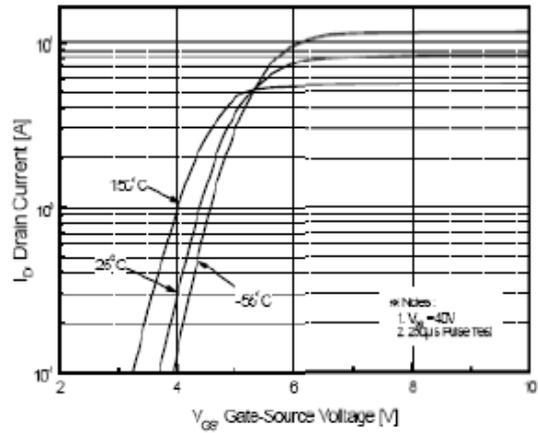


Fig.2 Transfer Current characteristics

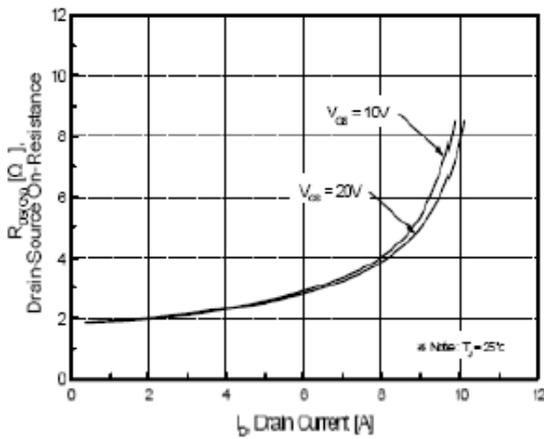


Fig.3 On Resistance variation vs Drain Current

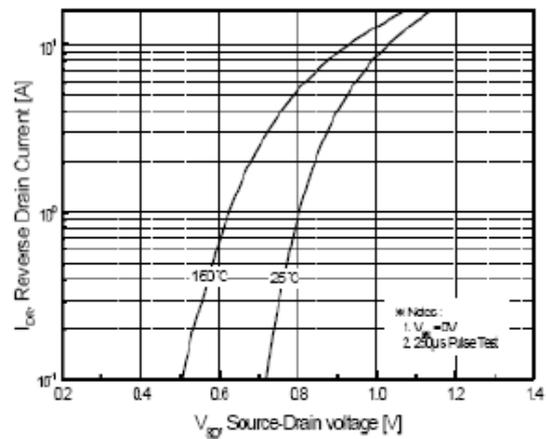


Fig.4 Body Diode Forward Voltage Variation vs Source Current and temperature

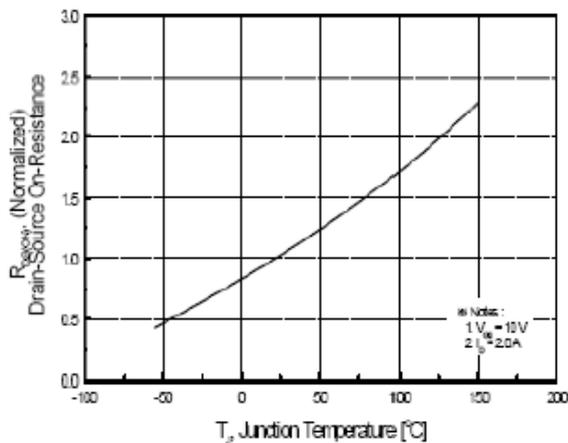


Fig.5 On-Resistance Variation vs Junction Temperature

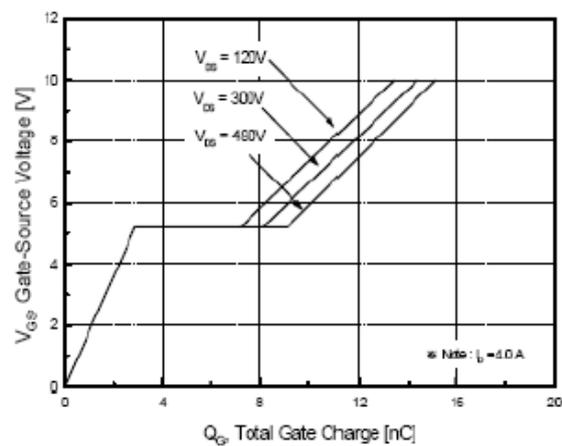
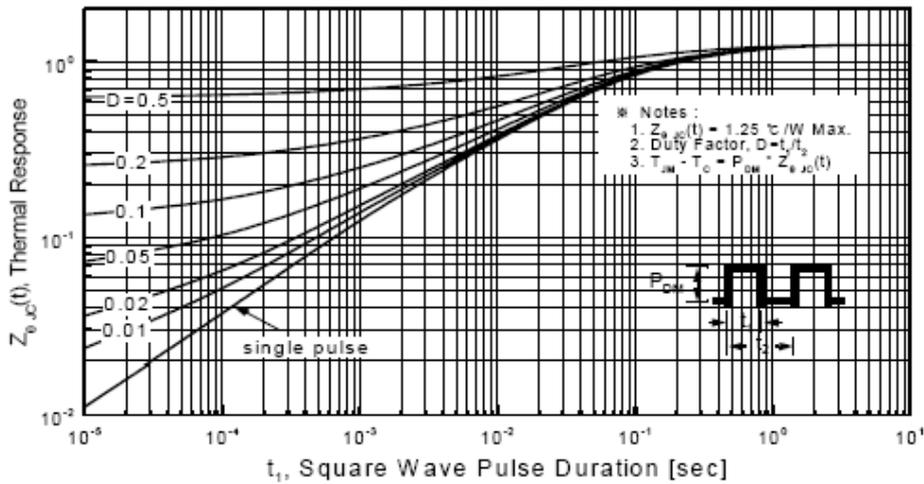
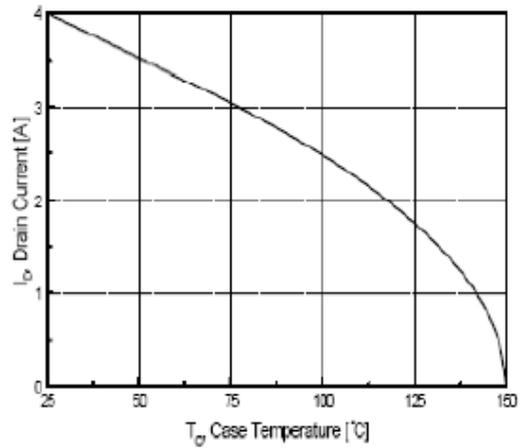
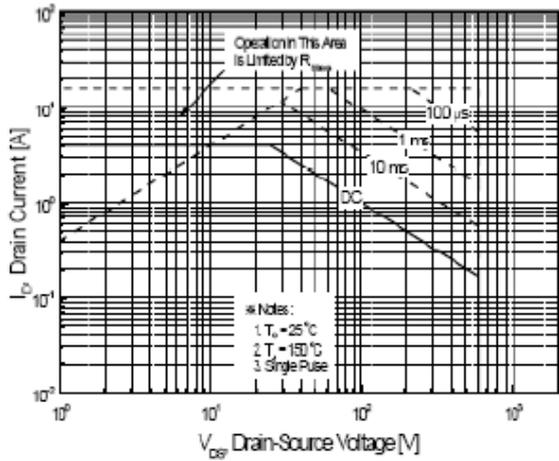


Fig.6 Gate Charge Characteristics



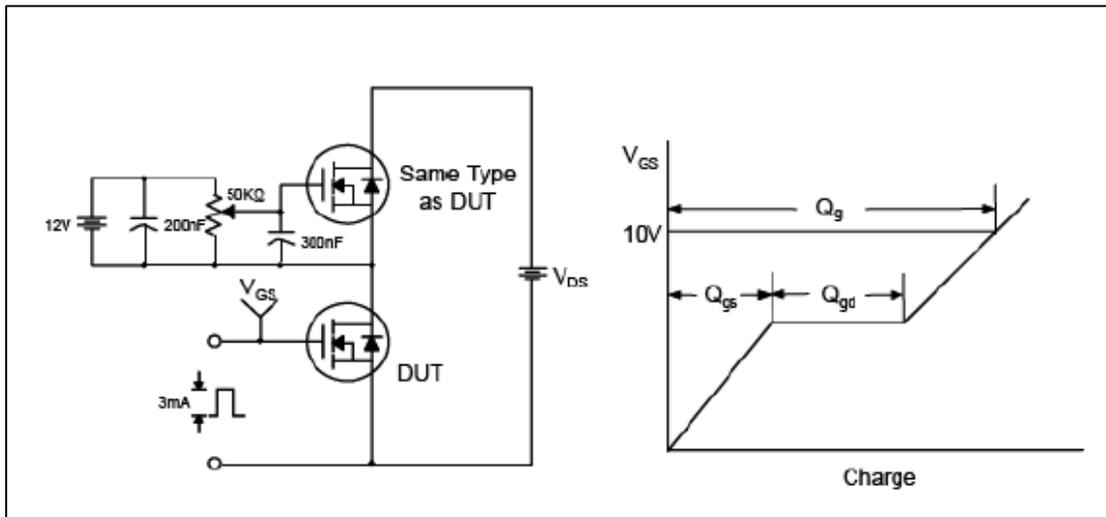


Fig.10 Gate Test circuit & Waveform

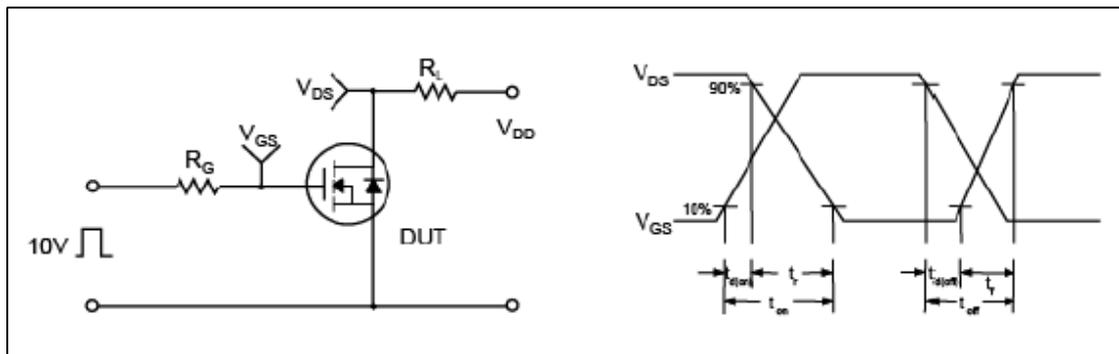


Fig.11 Resistive Switching Test Circuit & Waveform

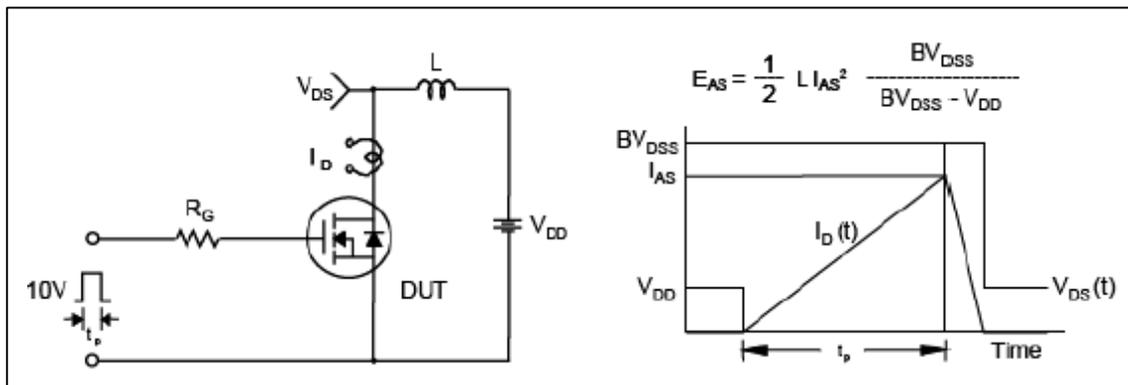


Fig.12 Uncamped Inductive Switching Test Circuit & Waveform

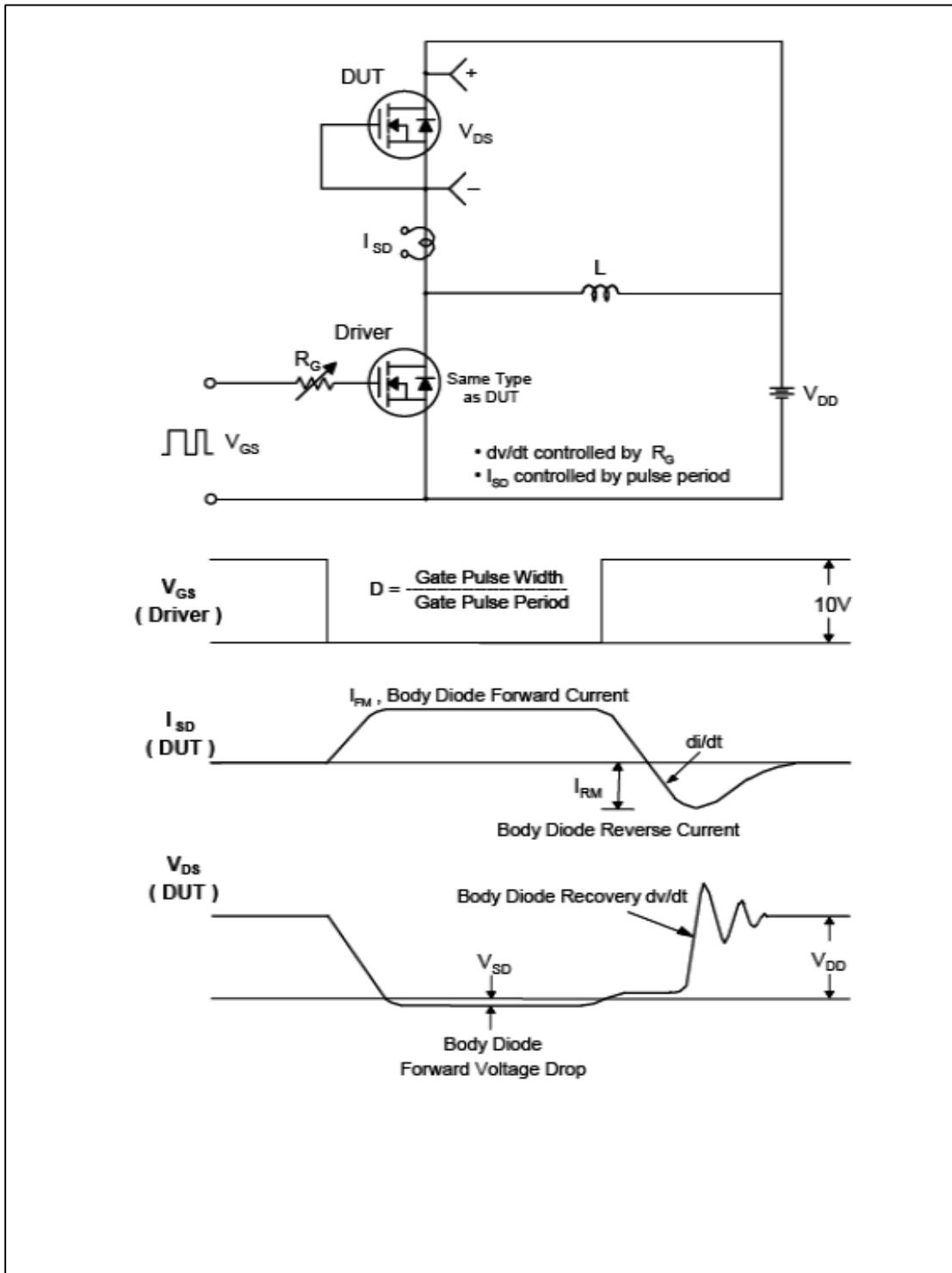


Fig.13 Peak Diode Recovery dv/dt Test Circuit & Waveform

