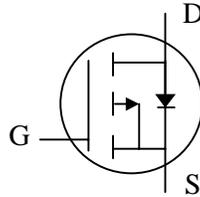


P-CHANNEL ENHANCEMENT-MODE POWER MOSFET

- Simple drive requirement
- 2.5V gate drive capability
- Fast switching

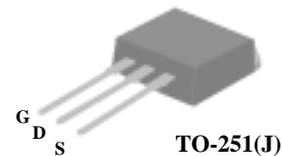
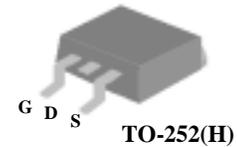


BV_{DSS}	-20V
$R_{DS(ON)}$	52m Ω
I_D	-18A

Description

Power MOSFETs from Silicon Standard provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-252 package is widely preferred for all commercial and industrial surface mount applications and suited for low voltage applications such as DC/DC converters. The through-hole version (SSM20P02J) is available for low-profile applications.



Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	- 20	V
V_{GS}	Gate-Source Voltage	± 12	V
$I_D @ T_A=25^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V	-18	A
$I_D @ T_A=100^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V	-14	A
I_{DM}	Pulsed Drain Current ¹	-50	A
$P_D @ T_A=25^\circ\text{C}$	Total Power Dissipation	31.25	W
	Linear Derating Factor	0.25	W/ $^\circ\text{C}$
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ\text{C}$
T_J	Operating Junction Temperature Range	-55 to 150	$^\circ\text{C}$

Thermal Data

Symbol	Parameter	Value	Unit
Rthj-c	Thermal Resistance Junction-case	Max. 4.0	$^\circ\text{C}/\text{W}$
Rthj-a	Thermal Resistance Junction-ambient	Max. 110	$^\circ\text{C}/\text{W}$

Electrical Characteristics @ $T_j=25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=-250\mu A$	-20	-	-	V
$\Delta BV_{DSS}/\Delta T_j$	Breakdown Voltage Temperature Coefficient	Reference to 25°C , $I_D=-1\text{mA}$	-	-0.03	-	$V/^\circ\text{C}$
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS}=-4.5V, I_D=-8A$	-	-	52	$\text{m}\Omega$
		$V_{GS}=-2.5V, I_D=-5A$	-	-	85	$\text{m}\Omega$
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=-250\mu A$	-0.5	-	-	V
g_{fs}	Forward Transconductance	$V_{DS}=-10V, I_D=-8A$	-	15	-	S
I_{DSS}	Drain-Source Leakage Current ($T_j=25^\circ\text{C}$)	$V_{DS}=-20V, V_{GS}=0V$	-	-	-1	μA
	Drain-Source Leakage Current ($T_j=150^\circ\text{C}$)	$V_{DS}=-16V, V_{GS}=0V$	-	-	-25	μA
I_{GSS}	Gate-Source Leakage	$V_{GS}=\pm 12$	-	-	± 100	nA
Q_g	Total Gate Charge ²	$I_D=-8A$	-	13.5	-	nC
Q_{gs}	Gate-Source Charge	$V_{DS}=-16V$	-	2.1	-	nC
Q_{gd}	Gate-Drain ("Miller") Charge	$V_{GS}=-4.5V$	-	1.6	-	nC
$t_{d(on)}$	Turn-on Delay Time ²	$V_{DS}=-10V$	-	12	-	ns
t_r	Rise Time	$I_D=-8A$	-	20	-	ns
$t_{d(off)}$	Turn-off Delay Time	$R_G=3.3\Omega, V_{GS}=-4.5V$	-	45	-	ns
t_f	Fall Time	$R_D=1.25\Omega$	-	27	-	ns
C_{iss}	Input Capacitance	$V_{GS}=0V$	-	1050	-	pF
C_{oss}	Output Capacitance	$V_{DS}=-16V$	-	410	-	pF
C_{rss}	Reverse Transfer Capacitance	$f=1.0\text{MHz}$	-	110	-	pF

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
I_S	Continuous Source Current (Body Diode)	$V_D=V_G=0V, V_S=-1.2V$	-	-	-10	A
I_{SM}	Pulsed Source Current (Body Diode) ¹		-	-	-50	A
V_{SD}	Forward On Voltage ²	$T_j=25^\circ\text{C}, I_S=-10A, V_{GS}=0V$	-	-	-1.2	V

Notes:

- 1.Pulse width limited by safe operating area.
- 2.Pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$.

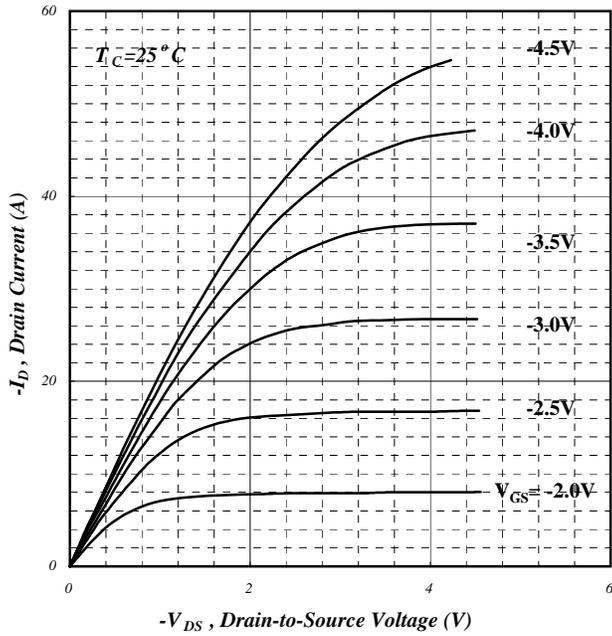


Fig 1. Typical Output Characteristics

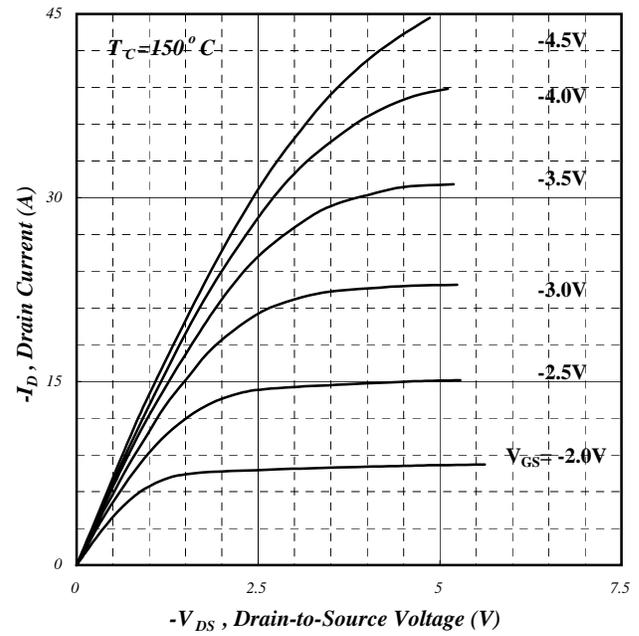


Fig 2. Typical Output Characteristics

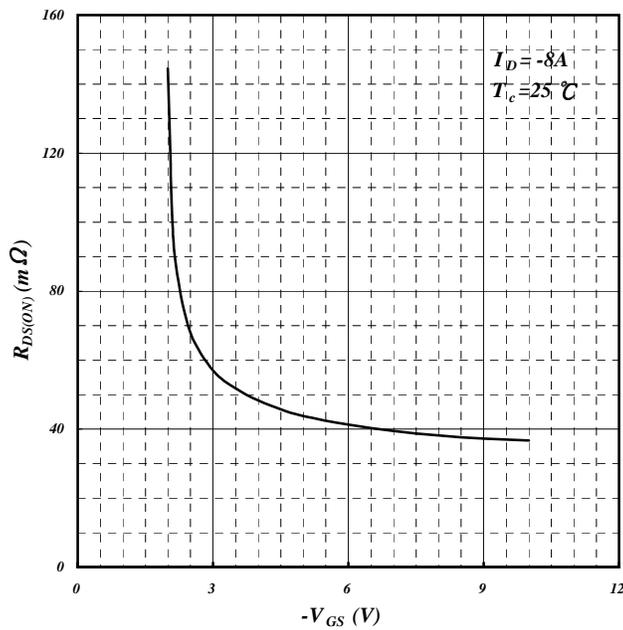


Fig 3. On-Resistance v.s. Gate Voltage

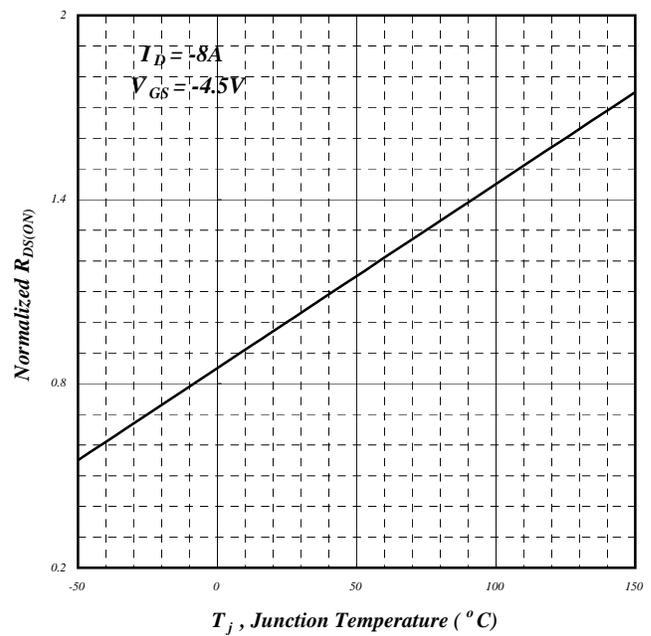


Fig 4. Normalized On-Resistance v.s. Junction Temperature

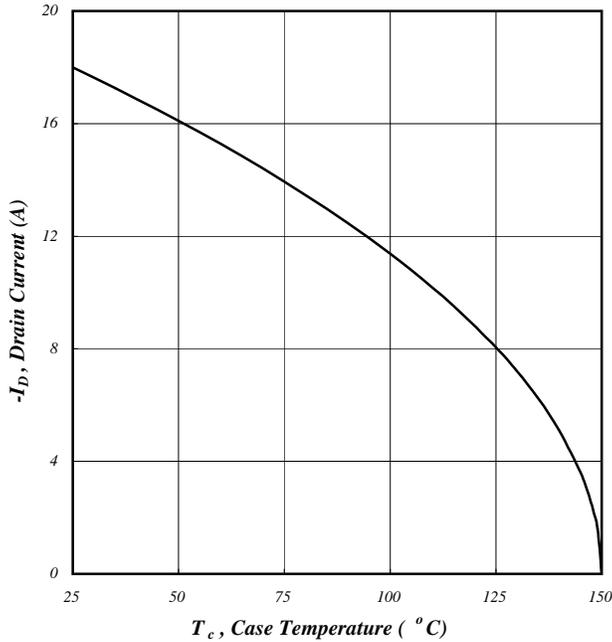


Fig 5. Maximum Drain Current v.s. Case Temperature

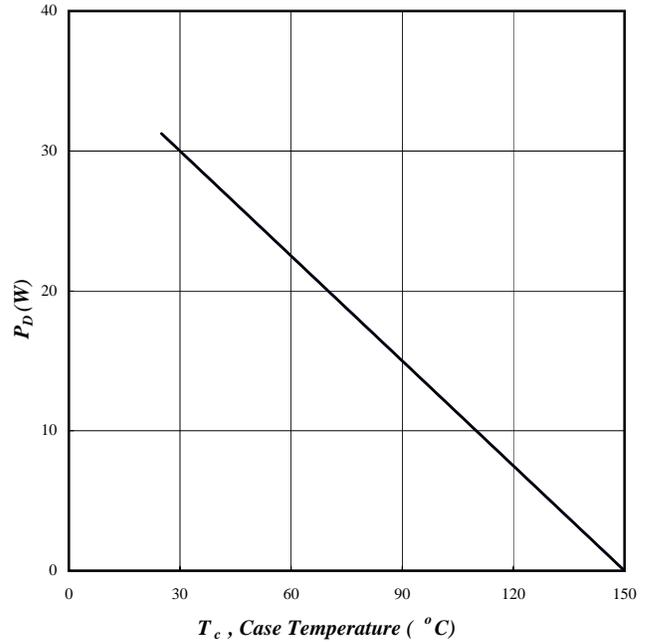


Fig 6. Typical Power Dissipation

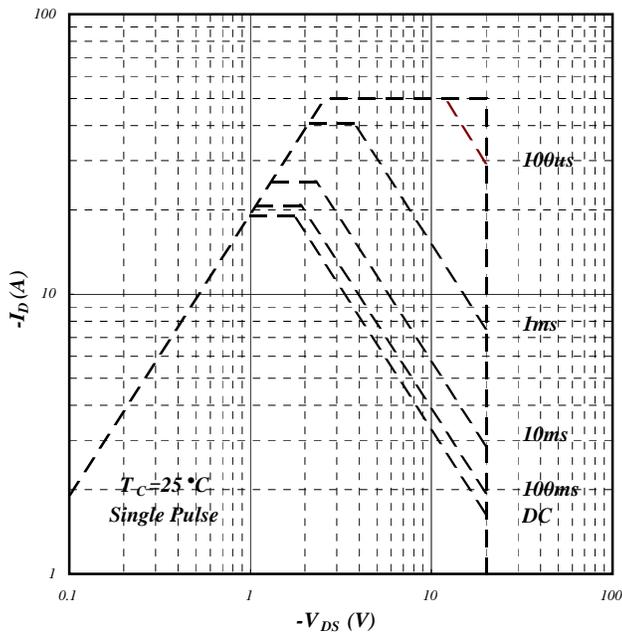


Fig 7. Maximum Safe Operating Area

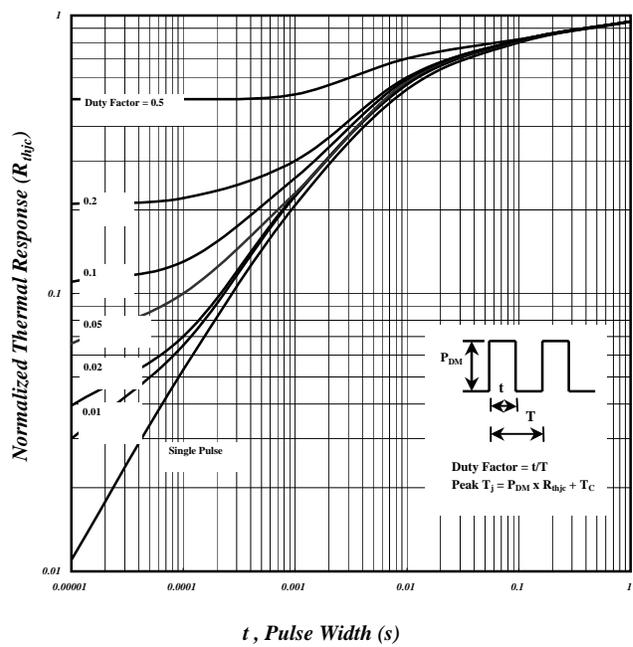


Fig 8. Effective Transient Thermal Impedance

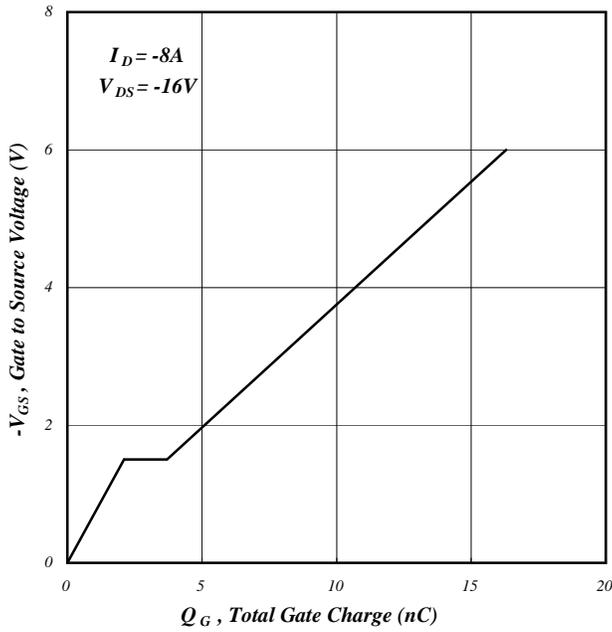


Fig 9. Gate Charge Characteristics

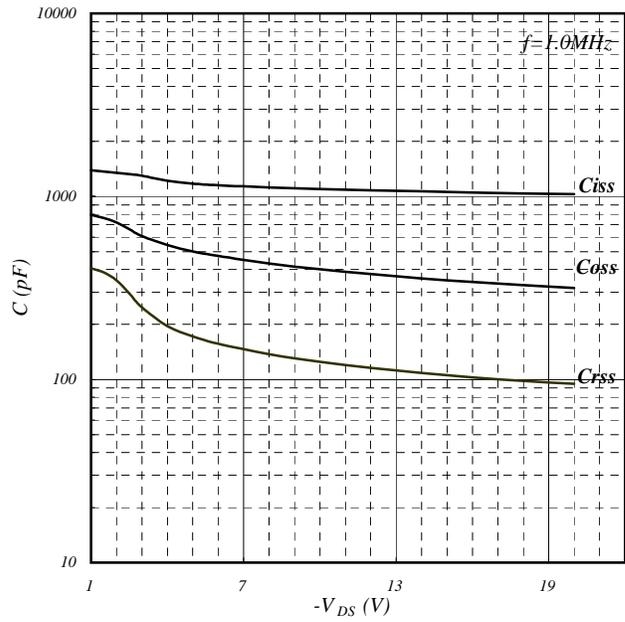


Fig 10. Typical Capacitance Characteristics

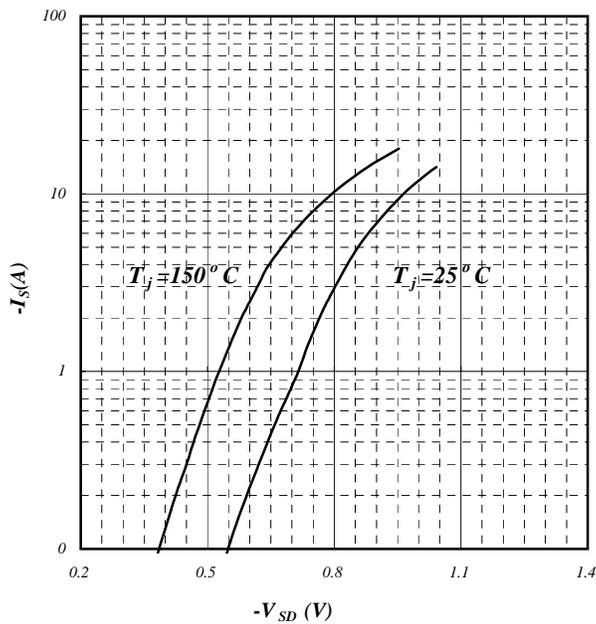


Fig 11. Forward Characteristic of Reverse Diode

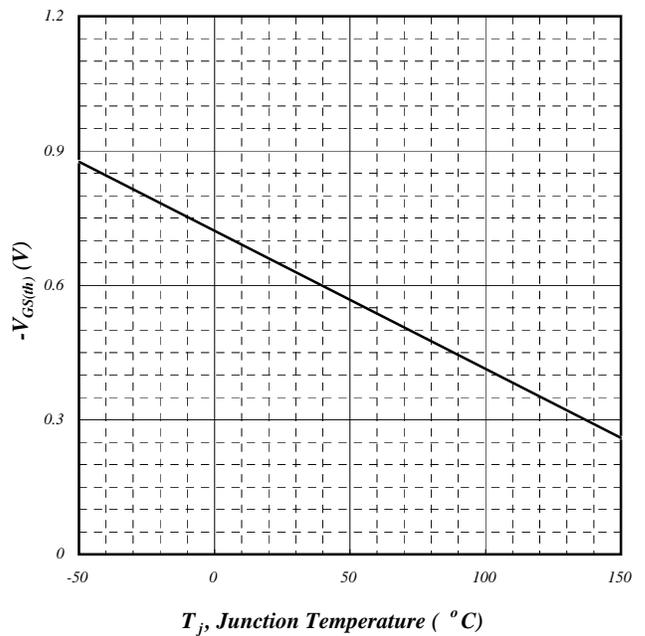


Fig 12. Gate Threshold Voltage v.s. Junction Temperature

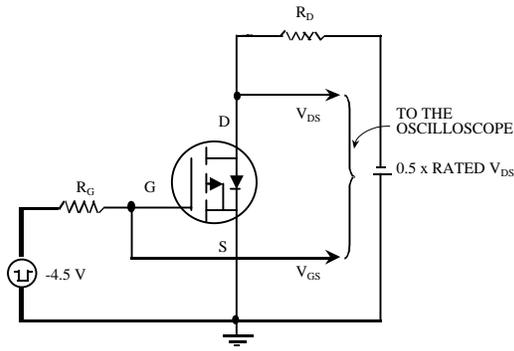


Fig 13. Switching Time Circuit

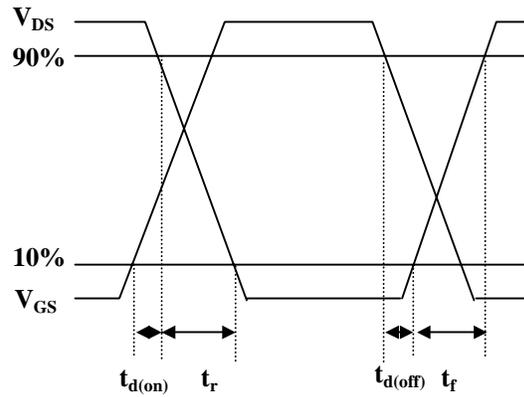


Fig 14. Switching Time Waveform

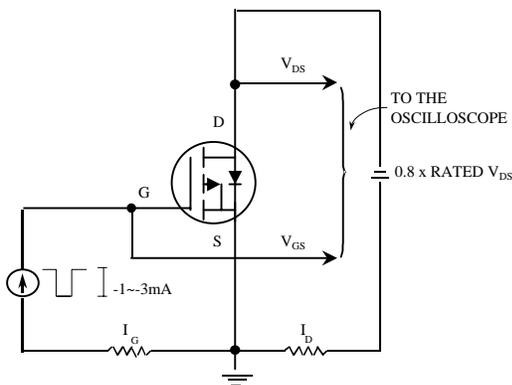


Fig 15. Gate Charge Circuit

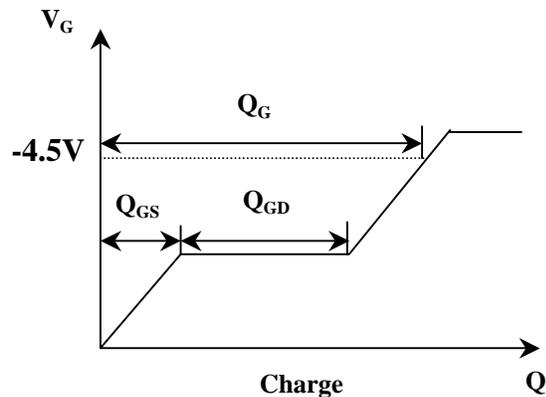


Fig 16. Gate Charge Waveform

Information furnished by Silicon Standard Corporation is believed to be accurate and reliable. However, Silicon Standard Corporation makes no guarantee or warranty, express or implied, as to the reliability, accuracy, timeliness or completeness of such information and assumes no responsibility for its use, or for infringement of any patent or other intellectual property rights of third parties that may result from its use. Silicon Standard reserves the right to make changes as it deems necessary to any products described herein for any reason, including without limitation enhancement in reliability, functionality or design. No license is granted, whether expressly or by implication, in relation to the use of any products described herein or to the use of any information provided herein, under any patent or other intellectual property rights of Silicon Standard Corporation or any third parties.