ATT7025 User Manual

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Revision History

Revision	*Date*	*Remark*
V1.0	2007-04-02	found
V1.1	2008-01-15	released

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1 General Description

1.1 Introduction

The ATT7025 is a low cost, high performance SOC Integrated with Energy measurement Unit, enhaced 8052 MCU core, an LCD driver, a RTC and all the peripherals to make an electronic energy meter with LCD display with a single part.

1.2 Features

1.2.1 Gerneral Features:

- Wide supply voltage operation :2.7V-3.6V
- Operating temperature:-40℃~85℃
- Packages :Lead free QFP100

1.2.2 Energy Measurment Features:

- Less than 0.1% error on active energy over a dynamic range of 1000 to 1
- Less than 0.5% error on reactive energy over a dynamic range of 1000 to 1
- Supprot Active power and active energy; reactive power and reactive energy; apparent power and apparent energy mearsuement.
- Supprot RMS mearsuement for voltage and current.
- Supprot Voltage frequency mearsuement.
- Three ADCs synchronous sample data ; active power ,reactive power, apparent power waveform data
- On-chip reference 1.25v±3%(temperature modulus ±25ppm/℃)
- Flexible anti-tamper method, the threshold value can be changed through register.
- Flexible no-load threshold level for anti-creep
- Auto-calibration for DC offset
- Various energy accumulating mode
- Apply fast pulse count register, preventing energe lose when power on and down.
- Width of pulse output PF/QF/SF is selectable
- Support single phase three wire system
- Zero-crossing interrupt
- Reactive power 90° shift phase compensation

1.2.3 Microprocessor Features:

- 8052 based core with 8052 compatible instruction set and architectures
- Clock: Integrated a high frequency crystal oscillating circuit and a 32.768khz crystal oscillating circuit ;Integrated a RC oscillator used for watchdog
- Memory:: 24K+8K FLASH program memory, 64 bytes Info FLASH memory with write-protect functions, 256 bytes internal RAM; 1K bytes external RAM including 256 bytes may maintain data by the bakeup battery when power down
- Support the power supply monitoring
- Low power consumption: Less than 6 mA current supply in normal mode, Less than 80uA current supply in Power saving mode; Less than 3Ua current supply in Power down mode.

- Integrated a hardware watch dog timer
- Integrated Real-time clock : Supprot ten-thousand years calendar,software compensate and write-protect
- Integrated LCD driver: Supprot maximum 4 commons x 40 segments
- Integrated Temperature sensor
- Integrated KEY, UART, SPI, I2C,PWM etc. on-chip peripherals
- On-chip ICE :support on-chip debug,In-system Programming and In-application programming

1.3 Abbreviations

Table 1-3 Abbreviations

Abbreviations	Original text
SFR	Special Function Register
PS0	Programe memory Section0
PS1	Programe memory Section1
WDT	Watch Dog Timer
RTC	Real Time Clock
GPIO	General Purpose IO
TPS	Temperature Sensor
LVD	Low Voltage Detect
POR	Power On Reset
BOR	Brown Out Reset
WKR	Wakeup Reset
EMU	Energy Mearsurment Unit
PSM	Power Saving Mode
PDM	Power Down Mode
SCM	System Clock Managment
KBI	Key Board Interface
UAM	User Application Mode
SFPM	Serial Flash Programming Mode
PFPM	Parallel Flash Programming Mode

1.4 Block Diagram

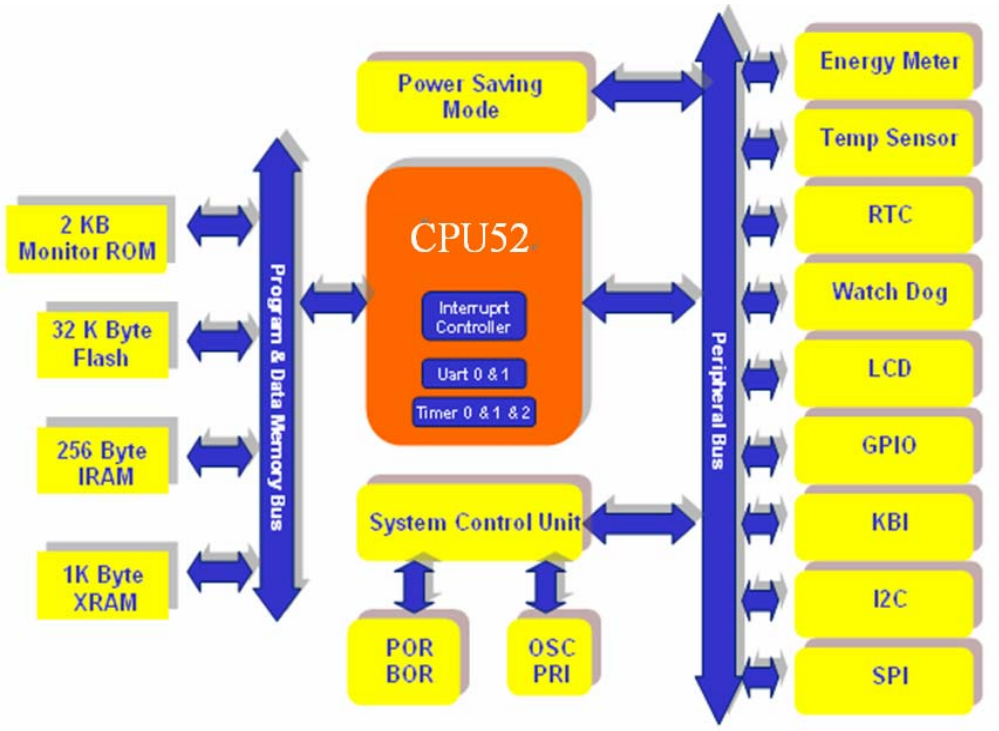


Fig 1-1 ATT7025 System block Diagram

1.5 Pin Definition

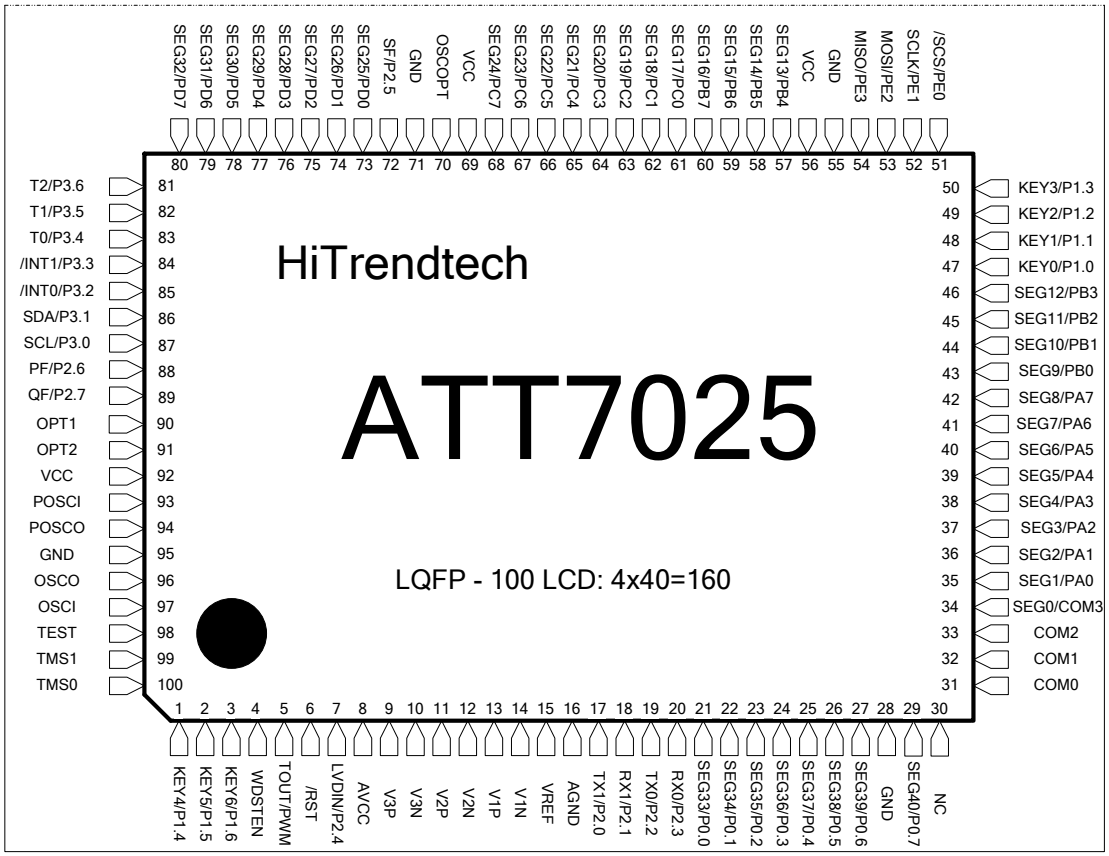


Figure 1-2 ATT7025 pins definition

1.6 Pins Description

Table 1-1 ATT7025 pins descriptions

Pins	Marking	Characteristic	Function
1	KEY4	input	Keyboard input
	P1.4	IO	GPIO port
2	KEY5	input	Keyboard input
	P1.5	IO	GPIO port
3	KEY6	input	Keyboard input
	P1.6	IO	GPIO port
4	WDTSEN	input	This pin is used to enable internal WDT when pulled high.When pulled low, an internal register determines WDT enable instead of this pin. This pin also contains an internal pull up 30K resistances.
5	TOUT	output	This pin is used for real time clock calibration. It is from RTC clock frequency division
	PWM	output	PWM module output
6	/RST	input	A logic 0 on this pin forces entires system to a known start-up state.A Schmitt-trigger and a spike filter is associated with this pin so that the device is more robust to EMC noise.This pin also contain an internal pull up 30K resistances .
7	LVDIN	input	Analog input for low voltage detection.
	P2.4	IO	GPIO port
8	AVCC	Power supply	This pin is the voltage supply for the analog parts of the device .The supply should be maintained at 2.7V-3.6V for specified operation.For maximum noise immunity, route this pin via a separate trace and place bypass capacitors as close as possible to the package.
9	V3P	input	Positive analog input for voltage channel.Internal ESD protection circuit is associated with this pin, the maximum input signal level is ±800mV.
10	V3N	input	Negative analog input for voltage channel.Internal ESD protection circuit is associated with this pin, the maximum input signal level is ±800mV.
11	V2P	input	Positive analog input for current channel 2, Internal ESD protection circuit is associated with this pin, the maximum input signal level is ±800mV.
12	V2N	input	Negative analog input for current channel 2, Internal ESD protection circuit is associated with this pin, the maximum input signal level is ±800mV.
13	V1P	input	Positive analog input for current channel 1, Internal ESD protection circuit is associated with this pin, the maximum input signal level is ±800mV.
14	V1N	input	Negative analog input for current channel 1, Internal ESD protection circuit is associated with this pin, the maximum input signal level is ±800mV.
15	VREF	IO	This pin provides access to the ADC on-chip voltage reference. the on-chip reference has a nominal value of 1.25v±3%(temperature modulus ±25ppm/℃) This pin can also be a input of the external voltage reference when tied to 10uF and 0.1uF capacitor external.
16	AGND	Power supply	This pin provides the ground reference for the analog circuitry .this pin should be tied to the analog ground plane.

17	TX1	output	Data output for the UART1 and IR
	P2.0	IO	GPIO port
18	RX1	input	Data input for the UART1 and IR.This pin should be pulled high outside.
	P2.1	IO	GPIO port
19	TX0	output	Data output for the UART0
	P2.2	IO	GPIO port
20	RX0	input	Data intput for the UART0. This pin should be pulled high outside.
	P2.3	IO	GPIO port
21	SEG33	output	LCD Segement output
	P0.0	IO	GPIO port
22	SEG34	output	LCD Segement output
	P0.1	IO	GPIO port
23	SEG35	output	LCD Segement output
	P0.2	IO	GPIO port
24	SEG36	output	LCD Segement output
	P0.3	IO	GPIO port
25	SEG37	output	LCD Segement output
	P0.4	IO	GPIO port
26	SEG38	output	LCD Segement output
	P0.5	IO	GPIO port
27	SEG39	output	LCD Segement output
	P0.6	IO	GPIO port
28	GND	Power supply	This pin provides the ground reference for the digital circuitry. This pin should be connected to the digital ground on the PCB.
29	SEG40	output	LCD Segement drive output
	P0.7	IO	GPIO port
30	NC		
31	COM0	output	Common output,COM0 is used for LCD backplanes
32	COM1	output	Common output,COM1 is used for LCD backplanes
33	COM2	output	Common output,COM2 is used for LCD backplanes
34	SEG0	output	LCD Segement drive output
	COM3	output	Common output, COM3 is used for LCD backplanes
35	SEG1	output	LCD Segement output
	PA0	IO	GPIO port
36	SEG2	output	LCD Segement output
	PA1	IO	GPIO port
37	SEG3	output	LCD Segement output
	PA2	IO	GPIO port
38	SEG4	output	LCD Segement output
	PA3	IO	GPIO port
39	SEG5	output	LCD Segement output
	PA4	IO	GPIO port
40	SEG6	output	LCD Segement output
	PA5	IO	GPIO port
41	SEG7	output	LCD Segement output
	PA6	IO	GPIO port
42	SEG8	output	LCD Segement output
	PA7	IO	GPIO port
43	SEG9	output	LCD Segement output
	PB0	IO	GPIO port
44	SEG10	output	LCD Segement output
	PB1	IO	GPIO port
45	SEG11	output	LCD Segement drive output

	PB2	IO	GPIO port
46	SEG12	output	LCD Segement drive output
	PB3	IO	GPIO port
47	KEY0	input	Keyboard input
	P1.0	IO	GPIO port
48	KEY1	input	Keyboard input
	P1.1	IO	GPIO port
49	KEY2	input	Keyboard input
	P1.2	IO	GPIO port
50	KEY3	input	Keyboard input
	P1.3	IO	GPIO port
51	/SCS	IO	Slave select when SPI is in slave mode.
	PE0	IO	GPIO port
52	SCLK	IO	SPI serial clock
	PE1	IO	GPIO port
53	MOSI	IO	SPI serial data pin, Master Out/Slave In
	PE2	IO	GPIO port
54	MISO	IO	SPI serial data pin,Master In/Slave Out
	PE3	IO	GPIO port
55	GND	Power supply	This pin provides the ground reference for the digital circuitry.
56	VCC	Power supply	Digital power supply.
57	SEG13	output	LCD Segement output
	PB4	IO	GPIO port
58	SEG14	output	LCD Segement output
	PB5	IO	GPIO port
59	SEG15	output	LCD Segement output
	PB6	IO	GPIO port
60	SEG16	output	LCD Segement output
	PB7	IO	GPIO port
61	SEG17	output	LCD Segement output
	PC0	IO	GPIO port
62	SEG18	output	LCD Segement output
	PC1	IO	GPIO port
63	SEG19	output	LCD Segement output
	PC2	IO	GPIO port
64	SEG20	output	LCD Segement output
	PC3	IO	GPIO port
65	SEG21	output	LCD Segement output
	PC4	IO	GPIO port
66	SEG22	output	LCD Segement output
	PC5	IO	GPIO port
67	SEG23	output	LCD Segement output
	PC6	IO	GPIO port
68	SEG24	output	LCD Segement output
	PC7	IO	GPIO port
69	VCC	Power supply	This pin is the voltage supply for the digital parts of the device .The supply should be maintained at 2.7V-3.6V.This pin should be decoupled with a 10uF capacitor in parallel with a ceramic 100nF capacitor.
70	OSCOPT	input	Fosc select pin. When OSCOPT=1, fosc comes from external 32.768khz oscillator; When OSCOPT =0, fosc comes from RC oscillator. Fosc is the clock of RTC,so when use the interior RTC.OSCOPT=1 is commended .

71	GND	Power supply	This pin provides the ground reference for the digital circuitry.
72	SF	output	This pin gives instantaneous apparent power information
	P2.5	IO	GPIO port
73	SEG25	output	LCD Segement output
	PD0	IO	GPIO port
74	SEG26	output	LCD Segement output
	PD1	IO	GPIO port
75	SEG27	output	LCD Segement output
	PD2	IO	GPIO port
76	SEG28	output	LCD Segement output
	PD3	IO	GPIO port
77	SEG29	output	LCD Segement output
	PD4	IO	GPIO port
78	SEG30	output	LCD Segement output
	PD5	IO	GPIO port
79	SEG31	output	LCD Segement output
	PD6	IO	GPIO port
80	SEG32	output	LCD Segement output
	PD7	IO	GPIO port
81	T2	output	Timer2 input.
	P3.6	IO	GPIO port
82	T1	output	Timer1 input.
	P3.5	IO	GPIO port
83	T0	output	Timer0 input
	P3.4	IO	GPIO port
84	/INT1	input	External interrupt 1 input
	P3.3	IO	GPIO port
85	/INT0	input	External interrupt 0 input
	P3.2	IO	GPIO port
86	SDA	IO	I2C serial data pin
	P3.1	IO	GPIO port
87	SCL	IO	I2C serial clock pin
	P3.0	IO	GPIO port
88	PF	output	Active Power high Frequency Logic Output.
	P2.6	IO	GPIO port
89	QF	output	Reactive Power high Frequency Logic Output
	P2.7	IO	GPIO port
90	OPT1	output	This pin hould be decoupled with a 10uF capacitor in parallel with a ceramic 100nF capacitor.
91	OPT2	output	This pin should be decoupled with a 10uF capacitor in parallel with a ceramic 100nF capacitor.
92	VCC	Power supply	This pin is the voltage supply for the digital parts of the device. The supply should be maintained at 2.7V-3.6V
93	POSCI	input	High frequency crystal oscillator input. A High frequency crystal oscillator (typical: 5.5MHz) can be connected across this pin and POSCO to provide one of clock source for ATT7025.
94	POSCO	output	High frequency crystal oscillator output. A High frequency crystal oscillator (typical: 5.5MHz) can be connected across this pin and POSCI to provide one of clock source for ATT7025.
95	GND	Power supply	These provide the ground reference for the digital circuitry
96	OSCO	output	Low frequency Crystal oscillator circuit output. A low frequency crystal oscillator (typical: 32.768Khz) can be connected across this pin and OSCI to provide one of clock source for ATT7025.

<table>
<tr><td>97</td><td>OSCI</td><td>input</td><td>Low frequency Crystal oscillator input. A low frequency crystal oscillator (typical: 32.768Khz) can be connected across this pin and OSCO to provide one of clock source for ATT7025.</td></tr>
<tr><td>98</td><td>TEST</td><td>input</td><td>Test mode pin. This pin also contains an internal pull up 30K resistances.</td></tr>
<tr><td>99</td><td>TMS1</td><td>input</td><td>Test mode pin This pin also contains an internal pull up 30K resistances.</td></tr>
<tr><td>100</td><td>TMS0</td><td>input</td><td>Test mode pin. This pin also contains an internal pull up 30K resistances.
<table>
<tr><td>TEST</td><td>TMS1</td><td>TMS0</td><td>work mode</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>UAM mode</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>SFPM mode</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>PFPM mode</td></tr>
</table>
</td></tr>
</table>

2 Electric Specification

2.1 Absolute Maximum Rating

parameter	sign	Min	Typ	Max	Unit
Digital power supply voltage	V_{CC}	-0.3	--	3.8	V
Analog power supply voltage	AV_{CC}	-0.3	--	3.8	V
The maximum I/O output source current	I_{source}	--	--	±10	mA
The maximum I/O output sunk current	I_{sunk}	--	--	±10	mA
Digital input voltage relative to GND	V_{IND}	-0.3	--	V_{CC}+0.3	V
Analog input voltage relative to AGND	V_{INA}	-0.3	--	AV_{CC}+0.3	V
Working temperature range	T_A	-40	--	85	℃
Storage temperature range	T_{stg}	-65	--	150	℃

2.2 DC Parameters

(V_{CC}=AV_{CC}=3.3V, temperature range -40℃～+85℃)

Object	Sym bol	Min	Typ	Max	Unit	Condition
Output high-level	V_{OH}	V_{CC}-0.4	--	--	V	
Output low-level	V_{OL}	--	--	0.4	V	
Input high-level	V_{IH}	0.7* V_{CC}	--	V_{CC}	V	
Input low-level	V_{IL}	V_{SS}	--	0.3* V_{CC}	V	
Normal mode	I_{ADD1}	5.5	--	5.6	mA	fsys=5.5MHz,fadc =450KHz, V_{CC}=3.3V
	I_{ADD2}	4.1	--	4.2	mA	fsys=1.3MHz,fadc =230KHz, V_{CC}=3.3V
Normal mode	I_{ADD1}	5.5	--	5.6	mA	fsys=5.5MHz,fadc =450KHz, V_{CC}=3.3V
	I_{ADD2}	4.1	--	4.2	mA	fsys=1.3MHz,fadc =230KHz, V_{CC}=3.3V
Power Saving Mode	I_{SDD1}	70	--	80	uA	fsys=32KHz,V_{CC}= 3.3V,With LCD on
	I_{SDD2}	65	--	75	uA	fsys=16KHz,V_{CC}= 3.3V,With LCD on
Power Down Mode	I_{PDD1}	35	--	37	uA	With OSC,RTC, RC,LCD,LVD on
	I_{PDD2}	19	--	21	uA	With OSC,RTC, RC,LCD on
	I_{PDD3}	11	--	13	uA	With OSC,RTC, RC on
	I_{PDD4}	2	--	3	uA	With OSC,RTC on
I/O pull high register	R_{PU}		30		kΩ	
POR startup voltage	V_{POR}	0	--	100	mV	

2.3 Enengy Metering Parameters

(V_{CC}=AV_{CC}=3.3V, @25C)

Item	Sym bol	Min	Typ	Max	Unit	Condition
Active energy Measurment Error			0.1%			Over Dynamic range of 1000:1 @25C
Active energy bandwidth			14		kHz	
Reactive energy Measurment Error			0.3%			Over Dynamic range of 1000:1 @25C
VRMS Measurment error			0.5%			
VRMS Measurment bandwidth			14		kHz	
IRMS Measurment error			0.5%			
IRMS Measurment bandwidth			14		kHz	
Phase error between channels PF=0.8 Capacitive PF=0.5 inductive			 ±0.04 ±0.04		 ° °	 Phase lead 37 ° Phase lag 60°

2.4 ADC

(V_{CC}=AV_{CC}=3.3V, @25C)

Item	Sym bol	Min	Typ	Max	Unit	Condition
The maximum signal voltage	V_{xn}			±800	mV	Analog channel difference input
Direct current input impedence	Z_{DC}	400			kΩ	
Signal-To-Noise	SNR		86		dB	
−3dB bangwidth	B_{-3dB}		14		kHz	

2.5 ADC Reference Voltage

(V_{CC}=AV_{CC}=3.3V,temperature range:-40℃～+85℃)

Item	Sym	Min	Typ	Max	Unit	Condition
Output voltage	V_{ref}		1.25		V	
Temperature modulus	T_c		±25		ppm/℃	

3 ATT7025 Architecture

3.1 Introduction

The ATT7025 integrate an 8-bit MCU core-CPU52 which compatible with the standard 8052 and has the corresponding compatible system architecture.

The CPU52 has two buses: Memory bus and SFR bus. The Memory bus can extend program and data memory on-chip, e.g. extending on-chip ROM, Flash, XRAM etc. The SFR(Special Function Register) bus provides an interface between the CPU and all on-chip peripheral.Except registers R0～R7, program counter(PC) and instruction register(IR), all the other control, configuration and statue registers are mapped into the SFR space .CPU52 can access these registers to control system. The whole chip architecture is shown in **fig 1-1**.

3.2 Memory

3.2.1 Memory Overview

The ATT7025 does not support external memory device. The on-chip memory is logically divided into 3 areas shown in **Fig 3-1**:

- Program memory（PM）: address 0000H-FFFFH
- Internal data memory（IRAM）: address 00H-FFH
- Data memory（DM）: address 0000H-FFFFH

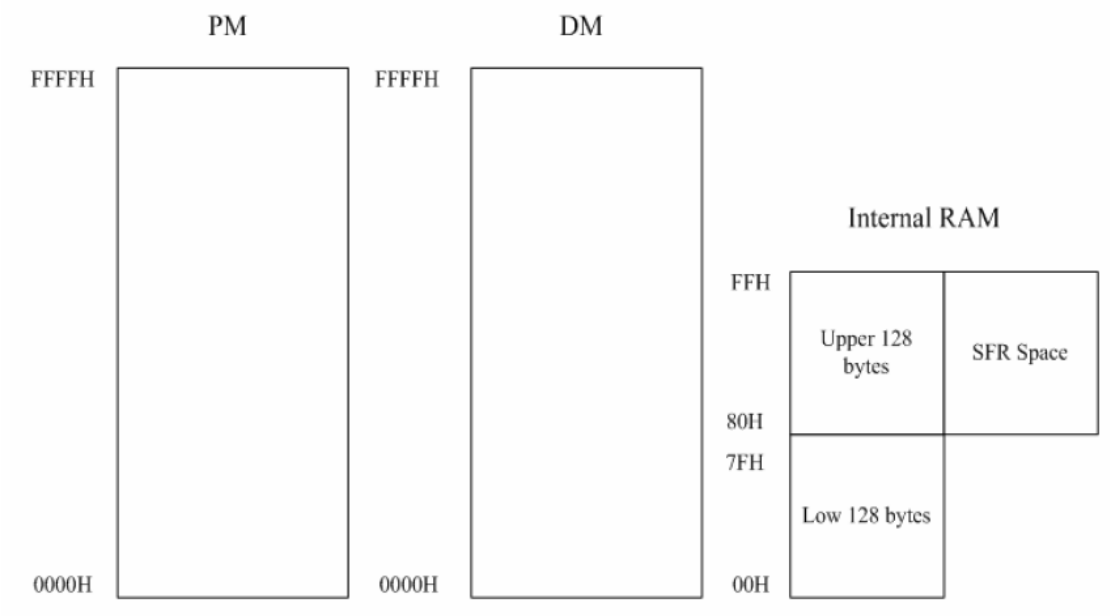


Fig 3-1 ATT7025 memory address

The address space of Program memory, IRAM and data memory are independent, they have their own addressing system, control signals and functions. Program memory which is read when fetches instructions or performs a MOVC operation is used to store program code. Data memory is used to store constants and variables, MOV instruction can access internal data memory while MOVX instruction can access external data memory.

3.2.2 Internal RAM

The internal RAM are organized is as shown in Fig 3-2.

The lower 32 bytes (00h–1Fh) form four banks of eight registers (R0–R7). The R0~R7 addresses are shown as **table 3-1**. Two bits RS1 and RS2 on the program status word PSW（SFR 0xD0H）select which bank is in use. The relation between PSW status and work registers is shown in **table 3-9** .CPU can select one work register with modifying RS1 and RS0 in PSW. It makes CPU have the quick scene protection capability. If user program needn't all the four registers, then the register units that are not in use can work as RAM.

The next 16 bytes form a block of bit-addressable memory space at bit addresses 00h–7Fh.

20H~2FH in internal RAM form a block of bit-addressable memory space (see **table 3-2**), every bit in the 16 unites has a bit address ranging from 00H to 7FH. Each bit in the addressing space can be regarded as a software trigger. Usually program status flags and bit control variables are located in bit addressing range. Also, the bit addressable units can be used as common data ram.

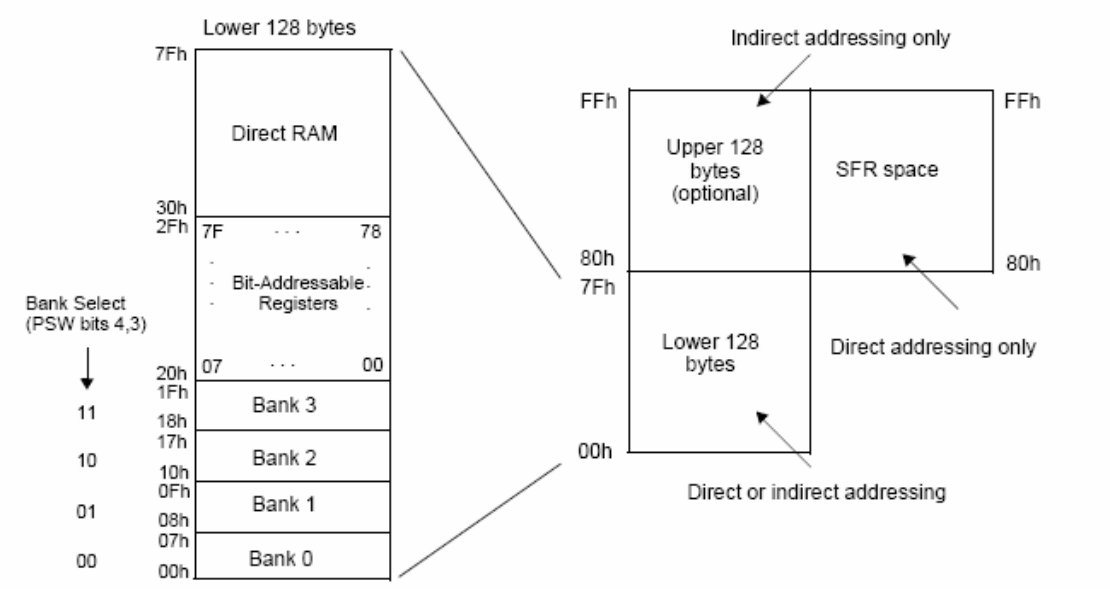


Fig 3-2 Internal RAM Organization

Table 3-1 General register ranges of internal RAM

0 zone		1 zone		2 zone		3 zone	
address	register	address	register	address	register	address	register
00H	R0	08H	R0	10H	R0	18H	R0
01H	R1	09H	R1	11H	R1	19H	R1
02H	R2	0AH	R2	12H	R2	1AH	R2
03H	R3	0BH	R3	13H	R3	1BH	R3
04H	R4	0CH	R4	14H	R4	1CH	R4
05H	R5	0DH	R5	15H	R5	1DH	R5
06H	R6	0EH	R6	16H	R6	1EH	R6
07H	R7	0FH	R7	17H	R7	1FH	R7

Table 3-2 bit-addressable ranges of internal RAM

byte address	bit address							
	D7	D6	D5	D4	D3	D2	D1	D0

2FH	7F	7E	7D	7C	7B	7A	79	78
2EH	77	76	75	74	73	72	71	70
2DH	6F	6E	6D	6C	6B	6A	69	68
2CH	67	66	65	64	63	62	61	60
2BH	5F	5E	5D	5C	5B	5A	59	58
2AH	57	56	55	54	53	52	51	50
29H	4F	4E	4D	4C	4B	4A	49	48
28H	47	46	45	44	43	42	41	40
27H	3F	3E	3D	3C	3B	3A	39	38
26H	37	36	35	34	33	32	31	30
25H	2F	2E	2D	2C	2B	2A	29	28
24H	27	26	25	24	23	22	21	20
23H	1F	1E	1D	1C	1B	1A	19	18
22H	17	16	15	14	13	12	11	10
21H	0F	0E	0D	0C	0B	0A	09	08
20H	07	06	05	04	03	02	01	00

Stack is required to save CPU scene in programs and it can be set in any range in internal RAM. But usually it is set in 30H~FFH. The location of top stack is pointed out by stack pointer SP.

3.2.3 Extended Memory Mapping

The ATT7025 on-chip extensive memory includes:

- 24K-bytes Code Flash memory, mapping as PM
- 8K-bytes Data Flash memory, mapping as PM or DM
- 64-bytes Info Flash memory, mapping as PM
- 1K-bytes XRAM, mapping as PM or DM
- 2K-bytes Monitor ROM ,mapping as PM

In UAM mode, PM and DM memory mapping are shown in fig 3-3

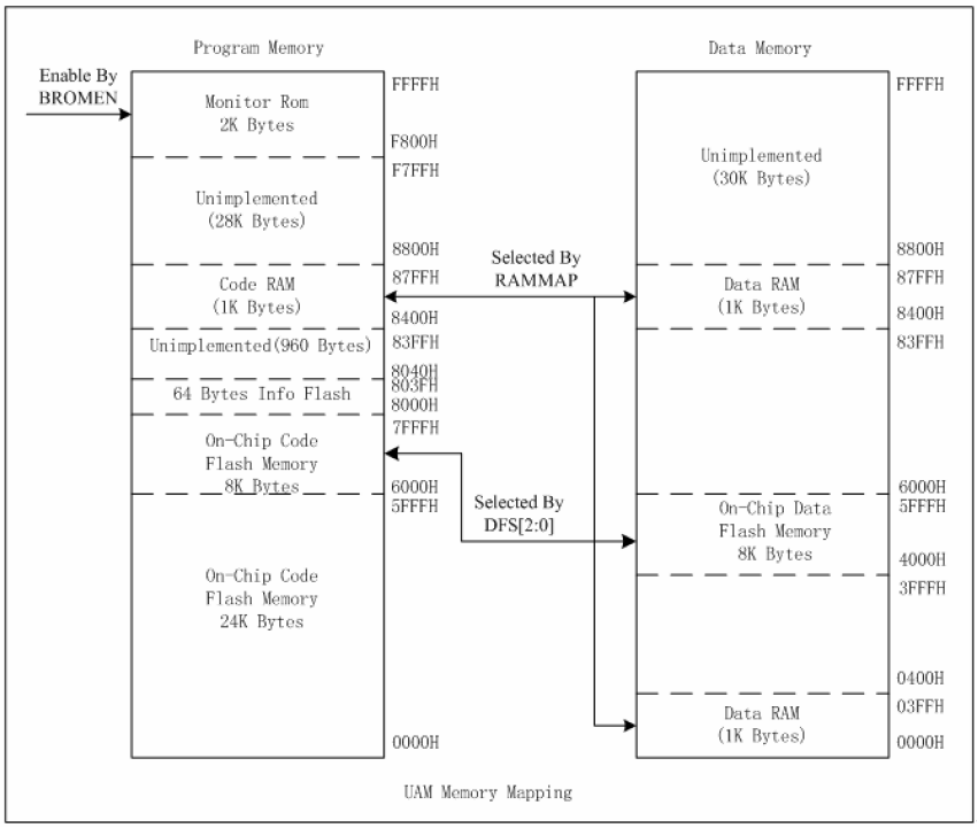


Fig 3-3 PM and DM memory mapping in UAM

1. Monitor Rom

In UAM mode, the address space of Monitor Rom is PM: F800H-FFFFH;

BROMEN **(Table 3-3)** controls Monitor Rom mapping. When BROMEN=1, Monitor Rom can be read in UAM mode, i.e., user can employ the program in Monitor Rom to support IAP function. When BROMEN=0, Monitor Rom rejects to be read in UAM mode and will return to 00H when application program accesses Monitor Rom.

2. XRAM

XRAM address mapping can be selected by RAMMAP **table 3-4**.

When RAMMAP=0, the RAM is located in addresses 0000H through 03FFH and can only be used as data RAM. But when RAMMAP=1, the RAM is located in addresses 8400H through 87FFH and then can be used as not only data RAM but also program RAM, i.e., address space 8400H-87FFH is shared by data and program..

3. Info Flash memory (PS1)

The 64-byte Flash is located in PM address space **(PS1):** 8000H-803FH.

PS1MAP**(table 10-4)** controls PS1 mapping. When PS1MAP=0, PS1 can not be accessed by direct addressing, returning 00H when accessing the space from 8000H to 803FH; When PS1MAP=1, PS1 is mapped to the space from 8000H to 803FH and its content can be read or modified by directly addressing.

4. Code Flash Memory

The 24Kbytes Flash is used to store program and located in PM address space **(PS0):**: 0000H-5FFFH.

5. Data Flash Memory

The 8K-byte Flash is defined as PM or DM by DFS[2:0]**(table 10-2).**

When DFS[2:0]=111, 8K-bytes Data Flash Memory is mapped as DM address space: 4000-5FFFH;

When DFS[2:0]=0xx, Data Flash Memory is mapped as PM address space(PS0): 6000-7FFFH;

In reset state, DFS[2:0]=000, Code Flash and Data Flash form a consecutive 32Kbyte program memory in addresses 0000 through 7FFFH.

3.2.4 Program Memory

Program memory is used to store program and table constant etc. Program memory uses PC as a address pointer, it can address up to 64K memory space with 16 bit address bus. As described above, the ATT7025 program memory includes: a 2Kbyte Monitor ROM, a 64byte Info Flash, a 24Kbyte Code Flash, an 8Kbyte Data Flash(DFS[2:0]=0XX), a 1Kbyte Code RAM(REMAP=1).

Software in Monitor Rom is mainly used for ICE function, for further information please see **on chip ICE support**.

Info Flash: It can be used to store manufactures information, ammeter parameters, etc..

Code Flash: Store the program code. In UAM the content of PC is 0000H after reset, so system starts taking instructions and running program from Code Flash 0000H.

Data Flash: When DFS[2:0]=0XX, it can be used as program memory and forms a consecutive 32K program memory space with Code Flash .

Code RAM: When RAMMAP=1, XRAM can work as program memory which can not only store program temporarily but also support to update the whole user program in flash.

3.2.5 Data Memory

Data memory is used to store data or operation results. As described above, the ATT7025 extened data memory includes: an 8Kbyte Data Flash memory and a 1Kbyte XRAM.

Data Flash: When DFS=111, it is mapped as a data memory. Data Flash memory is a hard-loss and high reliable memory, the read/write times are over 500,000 and the data storage time is over 100 years at 25C. It can replace E2PROM to store the result of energy measurment in application.

Data RAM: When RAMMAP=0, XRAM can work as a data memory to store user's temporal data. For the energy meter application, XRAM is devised in two parts: one is a 256 byte XRAM which is mapping from 0000H to 00FFH（RAMMAP=0） or from 8400H to 84FFH（RAMMAP=1）.It can work in power down mode and is used to store some important data for user in power down mode. The other is a 768 byte XRAM which is mapping from 0100H to 03FFH（RAMMAP=0） or from 8500H to 87FFH（RAMMAP=1）,This 768 bytes XRAM can not work in power down mode.

3.2.6 Registers

1．BROMEN control bit（write protect）

Table 3-3 BROMEN control bit (0xBEH,FMCFG. 2)

FMCFG			Address: BEH					
	Bit7	6	5	4	3	2	1	Bit0
Read:	DFS2	DFS1	DFS0	0	0	BROMEN	PMLOCK	RSLOCK
Write:				X	X			
Reset:	0	0	0	0	0	0	0	0

Note: when BROMEN=1, it can read Monitor Rom in UAM mode; when BROMEN=0, it can not read Monitor Rom in UAM mode. It will return to 00H if user program access the Monitor Rom address.

2．RAMMAP control bit

Table 3-4 RAMMAP control bit (0xF6H,MCON.0)

Memory Control Register (MCON)			Address: F6H					
	Bit7	6	5	4	3	2	1	Bit0
Read:	0	0	0	0	0	0	0	RAMMAP
Write:		X	X	x	X	X	X	
Reset:	0	0	0	0	0	0	0	0

Note: when REMAP=1, XRAM is used as a program memory; when AMMAP=0 XRAM is used as a data memory.

3.3 Instruction System

3.3.1 Addressing Mode

The ATT7025 provides the same addressing modes as the standard 8052 core.. There are six addressing modes shown as below:

1．Immediate addressing

In Immediate Addressing, the expression entered after the number sign (#) will be evaluated by the assembler and stored in the memory address specified. The value will be computed by the assembler.

For example:

```
MOV   A, #70H        ;70H->A
```

2．Direct addressing

The instruction includes the direct address of the operand which has pointed out the byte address or bit address of the data involved in operation. In the direct addressing way there are 3 kinds of the operand memory space:

1）low 128 bytes (00H-7FH)of IRAM. For example:

MOV A,70H ;(70H)->A

send the content of IRAM 70H to accumulator A

2）Bit address space. For example:

MOV C,00H

3）SFR

SFR can only be accessed by direct addressing. For example

MOV IE,#85H ;data 85H->Severance permission register IE

3．Register addressing

The instruction points out the content of a register as operand. In this addressing way, the working register is R0-R7. For example:

INC R0 ;(R0)+1->R0, operates on register R0 to make its content add 1

4． Indirect addressing

The instruction points out the content of the register as the operand address. In the register indirect addressing, the content in the register is not the operand but is the storage address of the operand.

Register indirect addressing can only use register R0 and R1 addressing the data in IRAM (00H~FFH). And it is also suitable to use R0, R1 or DPTR as the address pointer to access the external RAM. The register indirect addressing is expressed with the mark "@". For example:

MOVX A, @R0 ;((R0))->A

Send the IRAM content that R0 pointed out into accumulator A

5．Code indirect addressing

The addressing way is used to access the data table in the program memory. It accesses the data table in the PM by adding the contents of the base register (DPTR or PC) and the index register (A) as unsigned data to form a 16 bit address .For example:

MOVC A,@A+DPTR ;

MOVC A,@A+PC ;

6．Relative adressing

The addressing way takes the content of PC as the base address and adds the offset that the instruction presents, the result is considered to be the shift address. It is only suitable for the double-byte move instruction. The offset is a sign data in +127~128 and represented with 2 complement. For example:

JC rel ;C=1,JUMP

3.3.2 Instruction Set

The ATT7025 instruction set is compatible with the standard 8052 in operating code, function and the influence of instruction function on the flag bit.

Table3-5 ATT7025 instruction set list sign explain

Symbol	Function
A	Accumulator

(A)	Accumulator content
Rn	Register R0-R7
(Rn)	R0-R7 content
Ri	Data pointer R0or R1
(Ri)	Content of R0 or R1
((Ri))	Content of the unit pointed by R0 or R1
@Ri	Internal register pointed to by R0or R1(except MOVE)
(X)	Content of one register
X	Register
((X))	Content of the unit pointed to by one register
direct	Internal register address
(direct)	Content of direct
rel	Two's complement offset byte
bit	Direct bit address
#data	8-bit constant
#data 16	16-bit constant
addr 16	16-bit destination address
addr 11	11-bit destination address
←	Data transfer way
∧	Logic and
∨	Logic or
⊕	Logic
√	Affect the flag bit
×	Not affect the flag bit

Table 3-6 ATT7025 instruction set

Mnemonic	Description	Influence on the flag bit				Byte	Cycle	Hex Code
		P	OV	Ac	C_Y			
Arithmetic								
ADD A,Rn	A←(A)+(Rn)	√	√	√	√	1	1	28-2F
ADD A,direct	A←(A)+(direct)	√	√	√	√	2	2	25
ADD A,@Ri	A←(A)+((Ri))	√	√	√	√	1	1	26-27
ADD A,#data	A←(A)+data	√	√	√	√	2	2	24
ADDC A,Rn	A←(A)+(Rn)+(C_Y)	√	√	√	√	1	1	38-3F
ADDC A,direct	A←(A)+(direct)+ (C_Y)	√	√	√	√	2	2	35
ADDC A,@Ri	A←(A)+((Ri)) + (C_Y)	√	√	√	√	1	1	36-37
ADDC A,#data	A←(A)+data+ (C_Y)	√	√	√	√	2	2	34
SUBB A,Rn	A←(A)-(Rn)-(C_Y)	√	√	√	√	1	1	98-9F
SUBB A,direct	A←(A)-(direct)- (C_Y)	√	√	√	√	2	2	95
SUBB A,@Ri	A←(A)-((Ri)) - (C_Y)	√	√	√	√	1	1	96-97
SUBB A,#data	A←(A)-data- (C_Y)	√	√	√	√	2	2	94
INC A	A←(A)+1	√	×	×	×	1	1	04
INC Rn	Rn←Rn+1	×	×	×	×	1	1	08-0F
INC direct	direct←direct+1	×	×	×	×	2	2	05
INC @Ri	(Ri)← ((Ri)) + 1	×	×	×	×	1	1	06-07
INC DPTR	DPTR ←(DPTR)+1					1	1	A3
DEC A	A←(A)-1	√	×	×	×	1	1	14
DEC Rn	A←(Rn)-1	×	×	×	×	2	2	18-1F

DEC direct	A←(direct)-1	×	×	×	×	1	1	15
DEC @Ri	A← ((Ri)) - 1	×	×	×	×	1	3	16-17
MUL AB	AB←(A).(B)	√	√	×	√	1	5	A4
DIV AB	AB←(A)/(B)	√	√	×	√	1	5	84
DA A	Decimal adjust A	√	√	√	√	1	1	D4
Logic								
ANL A,Rn	A←(A)∧(Rn)	√	×	×	×	1	1	58-5F
ANL A,direct	A←(A)∧(direct)	√	×	×	×	2	2	55
ANL A,@Ri	A←(A)∧((Rn))	√	×	×	×	1	1	56-57
ANL A,#data	A←(A)∧data	√	×	×	×	2	2	54
ANL direct,A	direct←(direct) ∧A	×	×	×	×	2	2	52
ANL direct,#data	direct←(direct) ∧data	×	×	×	×	3	3	53
ORL A,Rn	A←(A) ∨(Rn)	√	×	×	×	1	1	48-4F
ORL A,direct	A←(A) ∨(direct)	√	×	×	×	2	2	45
ORL A,@Ri	A←(A) ∨((Ri))	√	×	×	×	1	1	46-47
ORL A,#data	A←(A) ∨data	√	×	×	×	2	2	44
ORL direct,A	direct←(direct) ∨A	×	×	×	×	2	2	42
ORL direct,#data	direct←(direct) ∨data	×	×	×	×	3	3	43
XRL A,Rn	A←(A) ⊕(Rn)	√	×	×	×	1	1	68-6F
XRL A,direct	A←(A) ⊕(direct)	√	×	×	×	2	2	65
XRL A,@Ri	A←(A) ⊕((Ri))	√	×	×	×	1	1	66-67
XRL A,#data	A←(A) ⊕data	√	×	×	×	2	2	64
XRL direct,A	direct←(direct) ⊕A	×	×	×	×	2	2	62
XRL direct,#data	direct←(direct) ⊕data	×	×	×	×	3	3	63
CLR A	A←0	√	×	×	×	1	1	E4
CPL A	A←$\overline{(A)}$	×	×	×	×	1	1	F4
SWAP A	Swap nibbles of A	×	×	×	×	1	1	C4
RL A	Rotate A left	×	×	×	×	1	1	23
RLC A	Rotate A left through carry	√	×	×	√	1	1	33
RR A	Rotate A right	×	×	×	×	1	1	03
RRC A	Rotate A right through carry	√	×	×	√	1	1	13
Data Transfer								
MOV A,Rn	A← (Rn)	√	×	×	×	1	1	E8-EF
MOV A,direct	A← （direct）	√	×	×	×	2	2	E5
MOV A,@Ri	A←((Ri))	√	×	×	×	1	1	E6-E7
MOV A,#data	A←data	√	×	×	×	2	2	74
MOV Rn,A	Rn←(A)	×	×	×	×	1	1	F8-FF
MOV Rn,direct	Rn ←(direct)	×	×	×	×	2	2	A8-AF
MOV Rn,#data	Rn ←data	×	×	×	×	2	2	78-7F
MOV direct,A	direct←(A)	×	×	×	×	2	2	F5
MOV direct,Rn	direct ←(Rn)	×	×	×	×	2	2	88-8F
MOV direct,direct	direct ← (direct)	×	×	×	×	3	3	85
MOV direct,@Ri	direct←((Ri))	×	×	×	×	2	2	86-87
MOV direct,#data	direct←data	×	×	×	×	3	3	75
MOV @Ri,A	((Ri))←(A)	×	×	×	×	1	1	F6-F7
MOV @Ri,direct	(Ri)←(direct)	×	×	×	×	2	2	A6-A7
MOV @Ri,#data	(Ri)←data	×	×	×	×	2	2	76-77
MOV DPTR,#data	DPTR←data	×	×	×	×	3	3	90

MOVC A,@A+DPTR	A←((A)+(DPTR))	√	×	×	×	1	3	93
MOVC A,@A+PC	A←((A)+(PC))	√	×	×	×	1	3	83
MOVX A,@Ri	A←((Ri+P2))	√	×	×	×	1	2-9*	E2-E3
MOVX A,@DPTR	A←((DPTR))	√	×	×	×	1	2-9*	E0
MOVX @Ri,A	((Ri)+P2)←A	×	×	×	×	1	2-9*	F2-F3
MOVX A,@DPTR	A←((DPTR))	×	×	×	×	1	2-9*	F0
PUSH direct	SP←SP+1,(SP) ←(direct)	×	×	×	×	2	2	C0
POP direct	direct←((SP)),SP←(SP)-1	×	×	×	×	2	2	D0
XCH A,Rn	(A)←→(Rn)	√	×	×	×	1	1	C8-CF
XCH A,direct	(A)←→(direct)	√	×	×	×	2	2	C5
XCH A,@Ri	(A)←→((Ri))	√	×	×	×	1	1	C6-C7
XCHD A,@Ri	$(A)_{0\sim3}$←→$((Ri))_{0\sim3}$	√	×	×	×	1	1	D6-D7
Boolean								
CLR C	C_Y←0	×	×	×	√	1	1	C3
CLR bit	bit←0	×	×	×		2	2	C2
SETB C	C_Y←1	×	×	×	√	1	1	D3
SETB bit	bit←1	×	×	×		2	2	D2
CPL C	$C_Y \leftarrow \overline{(C_Y)}$	×	×	×	√	1	1	B3
CPL bit	bit←$\overline{(bit)}$	×	×	×		2	2	B2
ANL C,bit	C_Y ←(C_Y)∧(bit)	×	×	×	√	2	2	82
ANL C,/bit	C_Y ←(C_Y)∧ $\overline{(bit)}$	×	×	×	√	2	2	B0
ORL C,bit	C_Y ←(C_Y)∨(bit)	×	×	×	√	2	2	72
ORL C,/bit	C_Y ←(C_Y)∨ $\overline{(bit)}$	×	×	×	√	2	2	A0
MOV C,bit	C_Y ←(bit)	×	×	×	√	2	2	A2
MOV bit,C	bit←(C_Y)	×	×	×	×	2	2	92
Branching								
ACALL addr11	PC←(PC)+2,SP←(SP)+1,(SP)←$(PC)_L$,SP←(SP)+1,(SP)←$(PC)_H$, $PC_{10\sim0}$←addr11	×	×	×	×	2	3	11-F1
LCALL addr16	PC←(PC)+2,SP←(SP)+1,(SP)←$(PC)_L$,SP←(SP)+1,(SP)←$(PC)_H$, $PC_{10\sim0}$←addr16	×	×	×	×	3	4	12
RET	$(PC)_H$←((SP)), SP←(SP)-1, $(PC)_L$←((SP)), SP←(SP)-1	×	×	×	×	1	4	22
RETI	$(PC)_H$←((SP)), SP←(SP)-1, $(PC)_L$←((SP)), SP←(SP)-1, return from interrupt	×	×	×	×	2	3	32
AJMP addr11	$PC_{10\sim0}$← addr11	×	×	×	×	3	4	01-E1
LJMP addr16	PC← addr16	×	×	×	×	2	3	02
SJMP rel	PC← PC+rel	×	×	×	×	2	3	80
JC rel	PC← PC+2,jump on carry equal to 1	×	×	×	×	2	3	40
JNC rel	PC← PC+2,jump on carry equal to 0	×	×	×	×	2	3	50
JB bit,rel	PC← PC+3,jump on direct bit=1	×	×	×	×	3	4	20
JNB bit,rel	PC← PC+3,jump on direct bit=0	×	×	×	×	3	4	30
JBC bit,rel	PC← PC+3,jump on direct bit=1 and clear	×	×	×	×	3	4	10

JMP @A+DPTR	PC←(A)+(DPTR)	×	×	×	×	1	3	73
JZ rel	PC←PC+2,jump on accumulator=0	×	×	×	×	2	3	60
JNZ rel	PC←PC+2,jump on accumulator not equal to 0	×	×	×	×	2	3	70
CJNE A,direct,rel	PC← PC+3,Compare A, direct JNE relative	×	×	×	×	3	4	B5
CJNE A,#d,rel	PC← PC+3 Compare A, immediate JNE relative	×	×	×	×	3	4	B4
CJNE Rn,#d,rel	PC← PC+3,Compare register, immediate JNE relative	×	×	×	×	3	4	B8-BF
CJNE @Ri,#d,rel	PC← PC+3,Compare indirect, immediate JNE relative	×	×	×	×	3	4	B6-B7
DJNZ Rn,rel	PC← PC+2, Decrement register, JNZ relative	×	×	×	×	2	3	D8-DF
DJNZ direct,rel	PC← PC+2, direct =(direct)-1, Decrement direct byte, JNZ relative	×	×	×	×	3	4	D5
Else								
NOP	No operation	×	×	×	×	1	1	00

3.3.3 Instruction Timing

There are some differences between the ATT7025 instruction timing and the standard 8052 .Their machine cycle and instruction cycle are different.As illustrated in Figure 3-4, machine cycles in the ATT7025 are 4 clock cycles in length, as opposed to the 12 clock cycles per instruction cycle in the standard 8052. This translates to a 3X improvement in execution time for most instructions.

However, some instructions require a different number of machine cycles on the ATT7025 than they do on the standard 8052. In the standard 8052, all instructions except for MUL and DIV take one or two machine cycles to complete. In the ATT7025 architecture, instructions can take between three and five machine cycles to complete. For example, in the standard 8052, the instructions MOVX A, @DPTR and MOV direct, direct each take 2 machine cycles (24 clock cycles) to execute. In the ATT7025 architecture, MOVX A, @DPTR takes two machine cycles (8 clock cycles) and MOV direct, direct takes three machine cycles (12 clock cycles). Both instructions execute faster on the ATT7025 than they do on the standard 8052, but require different numbers of clock cycles.

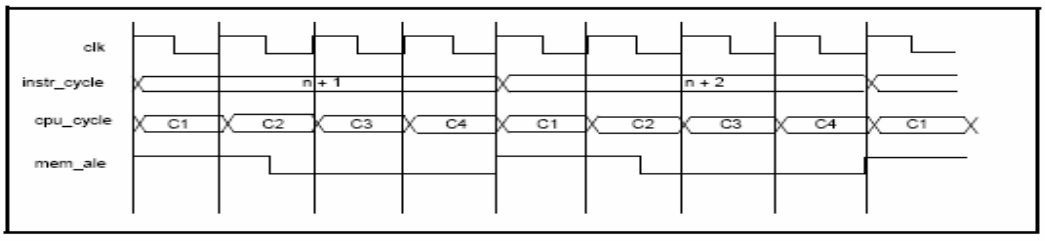


Figure 3-4 CPU machine cycle

For timing of real-time events, use the numbers of machine cycles from table 3-6 to calculate the timing of software loops. The bytes column of table 3-6 indicates the number of

memory accesses (bytes) needed to execute the instruction. In most cases, the number of bytes is equal to the number of instruction cycles required to complete the instruction. However, there are some instructions (for example, DIV and MUL) that require a greater number of instruction cycles than memory accesses.

By default, the ATT7025 timer/counters run at 12 clock cycles per increment so that timer-based events have the same timing as with the standard 8052. The timers can be configured to run at 4 clock cycles per increment to take advantage of the higher speed of the ATT7025.

3.4 Special Function Register

3.4.1 Introduction

All registers except the register R0~R7,program counter (PC) and instruction register (IR) reside in the SFR area from 80H to FFH. The **table 3-7** lists the symbol, address and the bit name of theSFR. In the table ,bit fence of SFR bit positions that contain 0 or 1 is inefficacy , SFR bit positions that contain "–" have no defining bit name and SFR bit positions that contain "*" have no definition, users do not have to operate on these registers. In the table the one marked black shadow is the ATT7025 CPU52 interior register and the others are the ATT7025 expansion registers.

Table 3-7 ATT7025 SFR

Address	Flags	BIT name							
		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x80	P0	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0
0x81	SP	-	-	-	-	-	-	-	-
0x82	DPL0	-	-	-	-	-	-	-	-
0x83	DPH0	-	-	-	-	-	-	-	-
0x84	DPL1	-	-	-	-	-	-	-	-
0x85	DPH1	-	-	-	-	-	-	-	-
0x86	DPS	0	0	0	0	0	0	0	SEL
0x87	PCON	SMOD0	-	1	1	GF1	GF0	STOP	IDLE
0x88	TCON	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
0x89	TMOD	GATE	C/T	M1	M0	GATE	C/T	M1	M0
0x8A	TL0	-	-	-	-	-	-	-	-
0x8B	TL1	-	-	-	-	-	-	-	-
0x8C	TH0	-	-	-	-	-	-	-	-
0x8D	TH1	-	-	-	-	-	-	-	-
0x8E	CKCON	-	-	T2M	T1M	T0M	MD2	MD1	MD0
0x8F	SPC_FNC	0	0	0	0	0	0	0	WRS
0x90	P1	0	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0
0x91	EXIF	IE5	IE4	IE3	IE2	1	0	0	0
0x92	MPAGE	-	-	-	-	-	-	-	-
0x93	PTA	PTA7	PTA6	PTA5	PTA4	PTA3	PTA2	PTA1	PTA0
0x94	PTB	PTB7	PTB6	PTB5	PTB4	PTB3	PTB2	PTB1	PTB0
0x95	PTC	PTC7	PTC6	PTC5	PTC4	PTC3	PTC2	PTC1	PTC0
0x96	PTD	PTD7	PTD6	PTD5	PTD4	PTD3	PTD2	PTD1	PTD0
0x97	PTE	*	*	*	*	PTE3	PTE2	PTE1	PTE0
0x98	SCON0	SM0_0	SM1_0	SM2_0	REN_0	TB8_0	RB8_0	TI_0	RI_0
0x99	SBUF0	-	-	-	-	-	-	-	-
0x9A	BWPR	PASS4	PASS3	PASS2	PASS1	PASS0	BITPS	PMOD1	PMOD0

0x9B	**DDRA**	DDRA7	DDRA6	DDRA5	DDRA4	DDRA3	DDRA2	DDRA1	DDRA0
0x9C	**DDRB**	DDRB7	DDRB6	DDRB5	DDRB4	DDRB3	DDRB2	DDRB1	DDRB0
0x9D	**DDRC**	DDRC7	DDRC6	DDRC5	DDRC4	DDRC3	DDRC2	DDRC1	DDRC0
0x9E	**DDRD**	DDRD7	DDRD6	DDRD5	DDRD4	DDRD3	DDRD2	DDRD1	DDRD0
0x9F	**DDRE**	*	*	*	*	DDRE3	DDRE2	DDRE1	DDRE0
0xA0	**P2**	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0
0xA1	**DDRP0**	DDRP07	DDRP06	DDRP05	DDRP04	DDRP03	DDRP02	DDRP01	DDRP00
0xA2	**DDRP1**	0	DDRP16	DDRP15	DDRP14	DDRP13	DDRP12	DDRP11	DDRP10
0xA3	**DDRP2**	DDRP27	DDRP26	DDRP25	DDRP24	DDRP23	DDRP22	DDRP21	DDRP20
0xA4	**DDRP3**	*	DDRP36	DDRP35	DDRP34	DDRP33	DDRP32	DDRP31	DDRP30
0xA5	**LEDP0**	LEDP07	LEDP06	LEDP05	LEDP04	LEDP03	LEDP02	LEDP01	LEDP00
0xA6	**LEDP1**	0	LEDP16	LEDP15	LEDP14	LEDP13	LEDP12	LEDP11	LEDP10
0xA7	**LEDP3**	*	LEDP36	LEDP35	LEDP34	LEDP33	LEDP32	LEDP31	LEDP30
0xA8	**IE**	EA	ES1	ET2	ES0	ET1	EX1	ET0	EX0
0xA9	**EMUIE**	PFIE	QFIE	SFIE	SPLIE	ZXIE	0	0	0
0xAA	**RTCIE**	ALMIE	SCNTIE	RTC2IE	RTC1IE	DAYIE	HRIE	MINIE	SECIE
0xAB	**SCIIE**	0	0	0	I2CIE	SPTIE	SPRIE	SPERIE	0
0xAC	**LVIIE**	0	0	0	0	0	0	LVDIE	BORIE
0xAD	**KEYIE**	0	KEYIE6	KEYIE5	KEYIE4	KEYIE3	KEYIE2	KEYIE1	KEYIE0
0xAE	**LEDC**	LEDC7	LEDC6	LEDC5	LEDC4	LEDC3	LEDC2	LEDC1	LEDC0
0xAF	**LEDE**	*	*	*	*	LEDE3	LEDE2	LEDE1	LEDE0
0xB0	**P3**	*	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0
0xB1	**EMUIF**	PFIF	QFIF	SFIF	SPLIF	ZXIF	0	0	0
0xB2	**RTCIF**	ALMF	SCNTF	RTC2F	RTC1F	DAYF	HRF	MINF	SECF
0xB3	**SCIIF**	I2RXIF	I2TXIF	0	0	SPTEIF	SPRFIF	SPOVIF	SPMDIF
0xB4	**LVIIF**	0	0	0	0	0	0	LVDIF	BORIF
0xB5	**LVDCON**	LVDS3	LVDS2	LVDS1	LVDS0	0	0	0	0
0xB6	**SYSSCR**	LOCK	BOROUT	LVDOUT	0	WDTCLR3	WDTCLR2	WDTCLR1	WDTCLR0
0xB7	**RSTSR**	POR	RST	WDT	BOR	WKR	0	0	0
0xB8	**IP**	1	PS1	PT2	PS0	PT1	PX1	PT0	PX0
0xB9	**LCDCFG**	PDH	PDL	PTCH	PTCL	PTBH	PTBL	PTAH	PTAL
0xBA	**P02CFG**	P267	P245	P223	P201	P067	P045	P023	P001
0xBB	**P3CFG**	-	T2	T1	T0	INT1	INT0	IRTX1	0
0xBC	**BORCFG**	PRION	WKRST	BORPDM	BORRST	BORVS1	BORVS0	PDM_RC	1
0xBD	**CLKCFG**	WDTS2	WDTS1	WDTS0	WDTEN	PRIP1	PRIP0	SYSCK1	SYSCK0
0xBE	**FMCFG**	DFS2	DFS1	DFS0	0	0	BROMEN	PMLOCK	RSLOCK
0xBF	**SUPDC**	0	PDTPS	PDEMU	PDBOR	PDLVD	PDLCD	PDI2C	PDSPI
0xC0	**SCON1**	SM0_1	SM1_1	SM2_1	REN_1	TB8_1	RB8_1	TI_1	RI_1
0xC1	**SBUF1**	-	-	-	-	-	-	-	-
0xC2	**LCDCLK**	0	FCSET1	FCSET0	DUTY1	DUTY0	0	LCLK1	LCLK0
0xC3	**LCDCR**	0	0	FC	LC	LCCON3	LCCON2	LCCON1	LCCON0
0xC4	**LADR**	0	0	LADR5	LADR4	LADR3	LADR2	LADR1	LADR0
0xC5	**LDAT**	LDAT7	LDAT6	LDAT5	LDAT4	LDAT3	LDAT2	LDAT1	LDAT0
0xC6	**RXCON**	RXCON7	RXCON6	RXCON5	RXCON4	RXCON3	RXCON2	RXCON1	RXCON0
0xC7	**PDMSR**	PDMSR5	PDMSR4	PDMSR3	PDMSR2	PDMSR1	PDMSR0	PDC	PPDC
0xC8	**T2CON**	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2	CP/RL2
0xC9	**TEMPDR**	TPDR7	TPDR6	TPDR5	TPDR4	TPDR3	TPDR2	TPDR1	TPDR0
0xCA	**RCAP2L**	-	-	-	-	-	-	-	-
0xCB	**RCAP2H**	-	-	-	-	-	-	-	-

0xCC	**TL2**	-	-	-	-	-	-	-	-
0xCD	**TH2**	-	-	-	-	-	-	-	-
0xD0	**PSW**	CY	AC	F0	RS1	RS0	OV	F1	P
0xD8	**EICON**	SMOD1	1	EPFI	PFI	WDTI	0	0	0
0xE0	**ACC**	-	-	-	-	-	-	-	-
0xE8	**EIE**	1	1	1	EWD	EX5	EX4	EX3	EX2
0xF0	**B**	-	-	-	-	-	-	-	-
0xF1	**RTCCON**	0	TOUTEN1	TOUTEN0	RTCTEN	TESL	TOUT2	TOUT1	TOUT0
0xF2	**RTCCAL**	CAL7	CAL6	CAL5	CAL4	CAL3	CAL2	CAL1	CAL0
0xF3	**SECCNT**	0	0	SCNT5	SCNT4	SCNT3	SCNT2	SCNT1	SCNT0
0xF4	**ALMR**	0	0	AM5	AM4	AM3	AM2	AM1	AM0
0xF5	**ALHR**	0	0	0	AH4	AH3	AH2	AH1	AH0
0xF6	**FCCON**	BPSEL	0	0	0	0	0	0	RAMMAP
0xF7	**KEYCR**	0	0	0	0	0	0	MODEY	ACKK
0xF8	**EIP**	1	1	1	PWDI	PX5	PX4	PX3	PX2
0xF9	**SECR**	0	0	SEC5	SEC4	SEC3	SEC2	SEC1	SEC0
0xFA	**MINR**	0	0	MIN5	MIN4	MIN3	MIN2	MIN1	MIN0
0xFB	**HRR**	0	0	0	HR4	HR3	HR2	HR1	HR0
0xFC	**DAYR**	0	0	0	DAY4	DAY3	DAY2	DAY1	DAY0
0xFD	**MTHR**	0	0	0	0	MTH3	MTH2	MTH1	MTH0
0xFE	**YRR**	0	YR6	YR5	YR4	YR3	YR2	YR1	YR0
0xFF	**DOWR**	0	0	0	0	0	DOW2	DOW1	DOW0

3.4.2 CPU52 Registers

Table3-8 lists the address, name, windows default and simple function of ATT7025 CPU52 register. Furthermore, the SFRS included in the CPU52 but not included in the standard 8052 SFR space are listed and marked black shadow.

Table 3-8 CPU52 IRAM

Address	Name	Windows dafault	Description
0x81	SP	0x07	Stack pointer
0x82	DPL0	0x00	Data pointer0 low
0x83	DPH0	0x00	Data pointer0 high
0x84	DPL1	0x00	Data pointer1 low
0x85	DPH1	0x00	Data pointer1 high
0x86	DPS	0x00	Data pointer0 select
0x87	PCON	0x30	Program control
0x88	TCON	0x00	Timer control register—see **table 11-3**
0x89	TMOD	0x00	Timer mode register—see **table 11-2**
0x8A	TL0	0x00	Time module 0 low
0x8B	TL1	0x00	Time module 1 low
0x8C	TH0	0x00	Time module 0 high
0x8D	TH1	0x00	Time module 1 low
0x8E	CKCON	0x01	Clock control register—see **table 11-7**
0x8F	SPC_FNC	0x00	DM/PM choose register—see **table 10-3**
0x91	EXIF	0x08	External interrupt flag register—see **table 4-5**
0x92	MPAGE	0x00	Reserved
0x98	SCON0	0x00	Strand 0 control register—see **table 15-8**
0x99	SBUF0	0x00	Serial 0 data buffer register

0xA8	IE	0x00	Interrupt enable register—see table 4-3
0xB8	IP	0x80	Interrupt PRI register—see table 4-4
0xC0	SCON1	0x00	Strand 1 control register—see table 15-9
0xC1	SBUF1	0x00	Serial 1 data buffer register
0xC8	T2CON	0x00	Timer 2 control register—see table 11-5
0xCA	RCAP2L	0x00	Timer 2 capture register low
0xCB	RCAP2H	0x00	Timer 2 capture register high
0xCC	TL2	0x00	Timer 2 low
0xCD	TH2	0x00	Timer 2 high
0xD0	PSW	0x00	Programme state register—see table 3-9
0xD8	EICON	0x40	Extend interrupt control register—see table 4-6
0xE0	ACC	0x00	Accumulator
0xE8	EIE	0xE0	External interrupt enable register—see table 4-7
0xF0	B	0x00	B register
0xF8	EIP	0xE0	External interrupt enable PRI register—see table 4-8

Register decription:

1. ACC

The accumulator is a working register, storing the results of many arithmetic or logical operations. The accumulator is used in more than half of the CPU52 instructions where it is usually referred to as A. The status register (PSW) constantly monitors the number of bits that are set in the accumulator to determine if it has even or odd parity.

2. B

The B register is used by the multiply and divide instructions, MUL AB and DIV AB to hold one of the operands. Since it isn't used for many instructions, it can be used as a scratchpad register like those in the register banks.

3. PSW

The PSW register reflects the status of arithmetic and logical operations through carry, auxiliary carry and overflow flags. The parity flag reflects the parity of the contents of the accumulator, which can be helpful for communication protocols. The PSW bits are described in Table 3-9. The Program Status Word SFR (PSW, 0xD0) is bit addressable:

Table 3-9 Program Status Word (PSW, 0xD0H)

Program Status Word (PSW)			Address: D0H					
	Bit7	6	5	4	3	2	1	Bit0
Read: Write:	CY	AC	F0	RS1	RS0	OV	F1	P
Reset:	0	0	0	0	0	0	0	0

Bit	Description
PSW.7	CY – Carry flag. Set to 1 when the last arithmetic operation resulted in a carry (during addition) or borrow (during subtraction), otherwise cleared to 0 by all arithmetic operations.
PSW.6	AC – Auxiliary carry flag. Set to 1 when the last arithmetic operation resulted in a carry into (during addition) or borrow from (during subtraction) the high order nibble, otherwise cleared to 0 by all arithmetic operations.
PSW.5	F0 – User flag 0. Bit-addressable, general purpose flag for software control .
PSW.4	RS1 – Register bank select bit 1. Used with RS0 to select a register blank in internal RAM.

<table>
<tr><td>PSW.3</td><td>RS0: Register Bank Select Bit 0.
<table>
<tr><td>RS1</td><td>RS0</td><td>Bank Selected</td></tr>
<tr><td>0</td><td>0</td><td>Register bank 0（00H~07H）</td></tr>
<tr><td>0</td><td>1</td><td>Register bank 1（08H~0FH）</td></tr>
<tr><td>1</td><td>0</td><td>Register bank 2（10H~17H）</td></tr>
<tr><td>1</td><td>1</td><td>Register bank 2（18H~1FH）</td></tr>
</table></td></tr>
<tr><td>PSW.2</td><td>OV – Overflow flag. Set to 1 when the last arithmetic operation resulted in a carry (addition), borrow (subtraction), or overflow (multiply or divide). Otherwise, the bit cleared to 0 by all arithmetic operations.</td></tr>
<tr><td>PSW.1</td><td>F1 – User flag 1. Bit-addressable, general purpose flag for software control.</td></tr>
<tr><td>PSW.0</td><td>P – Parity flag. Set to 1 when the modulo-2 sum of the 8 bits in the accumulator is 1 (odd parity), cleared to 0 on even parity.</td></tr>
</table>

4．SP

The stack pointer is a 1-byte register initialized to 0x07 after reset. This register is incremented before PUSH and CALL instructions, causing the stack to begin at location 0x08. The Stack Pointer keeps track of the current address of the top of the stack. .To push a byte of data onto the stack, the stack pointer is incremented and the data is moved to the new top of the stack. To pop a byte of data off of the stack, the top byte of data is moved into the awaiting address and the stack pointer is decremented. The stack resides into the extended internal RAM and the SP register holds the address of the stack into the externded RAM. The advantage of this solution is that the stack is segregated to the extended internal RAM. The use of the general purpose RAM can be limited to data storing and the use of the extended internal RAM limited to the stack pointer. This separation limits the chance of corruption of the data RAM with the stack pointer overflowing in data RAM.

Data can still be stored in extended RAM by using the MOVX command. To change the default starting address for the stack, move a value into the stack pointer, SP.

5．DPTR

The CPU52 employs dual data pointers to accelerate data memory block moves. The standard 8052 data pointer (DPTR) can be manipulated as a 16-bit register (DPTR = DPH, DPL. It is used to address external data RAM or peripherals. These provide memory addresses for internal code and data access.

The ATT7025 includes the standard data pointer as DPTR0 at SFR locations 82h(DPL0) and 83h(DPH0). It is not necessary to modify code to use DPTR0. The ATT7025 adds a second data pointer (DPTR1) at SFR locations 84h and 85h. The SEL bit in the DPTR Select register, DPS (SFR 86h), selects the active pointer. When SEL = 0, instructions that use the DPTR will use DPL0 and DPH0. When SEL = 1, instructions that use the DPTR will use DPL1 and DPH1. SEL is the bit 0 of SFR location 86h. No other bits of SFR location 86h are used.

All DPTR-related instructions use the currently selected data pointer.To switch the active pointer, toggle the SEL bit. The fastest way to do so is to use the increment instruction (INC DPS). This requires only one instruction to switch from a source address to a destination address, saving application code from having to save source and destination addresses when doing a block move. Using dual data pointers provides significantly increased efficiency when moving large blocks of

data.

6．Serial data buffers

ATT7025 has two Serials UART0 and UART1, the serial data buffers SBUF0 and SBUF1 are used to deposit the data UART0 and UART1 want to transmit or already receive. Any SBUF is composed infactly by two independent registers: one is the transmission buffer and another is the receiver buffer. When transmitting data to SBUF, it enters the transmission buffer; When reading data from the SBUF, the data comes from the receive buffer.

7．Timer /counters

The ATT7025 includes two timer/counters (Timer 0 and Timer 1) and an optional third timer/counter (Timer 2). Timer 2 is present when the parameter *timer2* = 1. Each timer/counter can operate as either a timer with a clock rate based on the *clk* pin, or as an event counter clocked by the *t0* pin (Timer 0), *t1* pin (Timer 1), or the *t2* pin (Timer 2). Each timer/counter consists of a 16-bit register that is accessible to software as two SFRs.

• Timer 0 – TL0 and TH0
• Timer 1 – TL1 and TH1
• Timer 2 – TL2 and TH2

8．Other CPU52 registers

IP、IE、EIP、EIE、EXIF、TMOD、TCON、T2CON、RCAP2、SCON0、SCON1、CKCON and PCON registers contain the control and stand bit of interrupt, timer and UART. This registers will be described in the next chapter.

3.4.3 Extended Registers

Beside theCPU52 interior register, the ATT7025 extends plenty of other registers (shown in **table 3-7** except the shadow parts) through SFR. These registers are generally named extended registers.

- Memory control register
  See the **Memory Mapping** and **FLASH** sections for more information.
- System reset register
  See the **System Reset** sections for more information.
- System clock manage register
  See the **Clock** and **Low Power** sections for more information.
- System power manage register
  See the **Power Supply System** and **Low Power** sections for more information
- Low voltage detect register
  See the Power Supply System section for more information.
- System work mode register
  See the Low Power Cost Mode section for more information
- Energy measurement register
  See the **Energy Measurement** sections for more information.
- GPIO register
  See the **GPIO**sections for more information.
- LCD register
  See the **LCD Driver**sections for more information
- RTC register

See the **RTC**sections for more information

- SPI register

  See the **SPI**sections for more information

- I2C register

  See the **I2C**sections for more information

- PWM register

  See the **PWM**sections for more information

- TPS register

  See the **TPS**sections for more information

- KEY register

  See the **KEY**sections for more information

- Hardware breakpoint register

  See the **On-chip ICE Support**sections for more information

- **Bit Write Protect Register**

  Bit protect mode prevents software from directly repairing the register bits protected by code.

Table 3-10 **Bit Write Protect Register** (BWPR, 0x9AH)

Bit Write Protect Register (BWPR)			**Address:**	**9AH**				
	Bit7	**6**	**5**	**4**	**3**	**2**	**1**	**Bit0**
Read:	PASS4	PASS3	PASS2	PASS1	PASS0	BITPS	PMOD1	PMOD0
Write:						x		
Reset:	0	0	0	0	0	0	0	0

Bit	**Description**
BWPR[7:3]	PASS[4:0]: bit write-protect code;PASS[4:0]=11000: Enable PMOD[1:0] write function. PASS[4:0]=10011:enable the write function of all protected bits 。 PASS[4:0]=10001:enable the write function of all RTC protected registers PASS[4:0]=10101:turn off the write function of all RTC protected registers
BWPR.2	BITPS: bit write protect flag;BITPS=1: software can amend all protected bits;BITPS=0: software can not amend all protected bits
BWPR[1:0]	PMOD[1:0]: bit write protect mode choice,PMOD[1:0]=11: bit write protect state can be amended. PMOD[1:0]=00/01/10: bit write protect state can not be amended.

Note:

When PMOD[1:0]=11,write PASS[4:0]=10011 can enable the write function of all protected bits. The bits can be amended by software and the write-enable is turned on here. When PASS[4:0]=10101,it will turn off the write function of all protected bits . The bits can not be amended by software and the write- enable is turned off here.

When enable the write function, it will be turned off automatically after 128 fsys if there is no write function on PASS[4:0] and the BWPR will be reset 00H.

BITPS shows the current write-enable state. If enabled, BITPS=1, or BITPS=0.

PMOD[1:0] can not be amended directly. When PASS[4:0]=11000,the PMOD[1:0] bit can be amended ,or the write function is of no effect.

Registers protected（**Red font in table 3-7**）:

1． RTC registers: includes RTCCAL、SECR、MINR、HRR、DAYR、MTHR、YRR、DOWR;

2． System configuring registers: include BORCFG、CLKCFG、FMCFG;

3. Power supply and clock registers SUPDC;
4. GPIO multiconfiguring register: including LCDCFG、P02CFG、P3CFG.

4 Interrupt System

4.1 Introduction

The ATT7025 provides 13 interrupt sources. There are 7 general interrupts including external int0_n , int1_n, timer interrupt T0, T1, T2 and UART0, UART1. These interrupts reserves the original function of the standard 8052.

The other 6 interrupts are the 6 extend interrupts of CPU52:

- Electricity Measurement Unit Interrupt (IRQ_EMU)
- Real Time Clock Interrupt (IRQ_RTC)
- Keyboard Interrupt (IRQ_KBI)
- I2C or SPI Interrupt (IRQ_SCI)
- LVD or BOR Interrupt (IRQ_LVI)
- On-Chip Debugging Interrupt (IRQ_OCD)

Interrupt system summarized as the following table

Table 4-1 ATT7025 Interrupt System

ATT7025 Interrupt Source	CPU52 Interrupt Source	Function Description	Natual Priority	Interrupt Vector	Interrupt Enable （EA=1）	Interrupt Flags
OCD	pfi	On-Chip Debugging Interrupt, see on-chip ICE support chapter	0	0033h	EICON.5 BPEN	EICON.4 BPACK
INT0	int0_n	External int_0 Interrupt	1	0003h	IE.0	-
T0	TF0	Timer0 Interrupt	2	000Bh	IE.1	TF0
INT1	int1_n	External int_1 Interrupt	3	0013h	IE.2	-
T1	TF1	Timer1 Interrupt	4	001Bh	IE.3	TF1
UART0	TI_0 or RI_0	Send/Receive UART0	5	0023h	IE.4	TI_0 or RI_0
T2	TF2	Interrupt Timer2	6	002Bh	IE.5	TF2
UART1	TI_1 or RI_1	Send/Receive UART1	7	003Bh	IE.6	TI_1 or RI_1
EMU	int2	EMU Interrupt, see EMU chapter	8	0043h	EIE.0 EMUIE	EXIF.4 EMUIF
RTC	int3_n	RTC Interrupt	9	004Bh	EIE.1 RTCIE	EXIF.5 RTCIF
KBI	int4	Keyboard Interrupt, see key KEY chapter	10	0053h	EIE.2 KEYIE	EXIF.6 KEYCR.0
SCI	int5_n	I2C or SPI Interrupt，see I2C and SPI chapter	11	005Bh	EIE.3 SCIIE	EXIF.7 SCIIF
LVI	wdti	LVD or BOR Interrupt，see LVD and BOR chapter	12	0063h	EIE.4 LVIIE	EICON.3 LVIIF

4.2 Registers

Table 4-2 Interrupt System Register List

Address	Name	Reset Value	Function Description
0xA8	IE	0x00	Interrupt Enable Register—see table 4-3
0xB8	IP	0x00	Interrupt Priority Register—see table 4-4
0x91	EXIF	0x08	External Interrupt Flage Register—see table 4-5
0xD8	EICON	0x40	Extended Interrupt Control Register—see table 4-6
0xE8	EIE	0xE0	Extended Interrupt Enable Register—see table 4-7
0xF8	EIP	0xE0	Extended Interrupt Priority Register—see table 4-8
0xA9	EMUIE	0x00	EMU Interrupt Enable Register—see table 9-9
0xB1	EMUIF	0x00	EMU Interrupt Flag Register—see table 9-10
0xAA	RTCIE	0x00	RTC Interrupt Enable Register—see table 12-5
0xB2	RTCIF	0x00	RTC Interrupt Flag Register—see table 12-6
0xAD	KEYIE	0x00	KEY Interrupt Enable Register—table 19-2 or fig 18-3
0xF7	KEYCR	0x00	KEY Control Register—see table 19-1
0xAB	SCIIE	0x00	SCI Interrupt Enable Register—see table 16-3
0xB3	SCIIF	0x08	SCI Interrupt Flag Register—see table 16-4
0xAC	LVIIE	0x00	LVI Interrupt Enable Register—see table 7-10
0xB4	LVIIF	0x00	LVI Interrupt Flag Register—see table 7-11
0xE3	HWBPCR	0x00	Hardware Breakpoint Control Register—see table 22-4

1. Interrupt Enable Register

Table 4-3 Interrupt Enable Register (IE 0xA8H)

Interrupt Enable Register (IE)			Address: A8H					
	Bit7	6	5	4	3	2	1	Bit0
Read: Write:	EA	ES1	ET2	ES0	ET1	EX1	ET0	EX0
Reset:	0	0	0	0	0	0	0	0

Bit	Function Description
IE.7	EA – Global Interrupt Enable. Controls masking of all interrupts except power-fail interrupt. EA = 0 disables all interrupts (EA overrides individual interrupt enable bits). When EA = 1, each interrupt is enabled or masked by its individual enable bit.
IE 6	ES1 – Enable Serial Port 1 Interrupt. ES1 = 0 disables Serial Port 1 interrupts (TI_1 and RI_1). ES1 = 1 enables interrupts generated by the TI_1 or RI_1 flag. ES1 is available only when the extended interrupt unit is implemented. Otherwise, it is read as 0. If the extended interrupt unit is implemented and Serial Port 1 is not implemented (*serial* < 2), ES1 is present but not used.。
IE.5	ET2 – Enable Timer 2 Interrupt. ET2 = 0 disables Timer 2 interrupt (TF2). ET2 = 1 enables interrupts generated by the TF2 or EXF2 flag. If Timer 2 is not implemented (timer2 = 0), ET2 is present but not used.
IE.4	ES0 – Enable Serial Port 0 Interrupt. ES0 = 0 disables Serial Port 0 interrupts (TI_0 and RI_0). ES0 = 1 enables interrupts generated by the TI_0 or RI_0 flag. If Serial Port 0 is not implemented (serial = 0), ES0 is present but not used.
IE.3	ET1 – Enable Timer 1 Interrupt. ET1 = 0 disables Timer 1 interrupt (TF1). ET1 = 1 enables interrupts generated by the TF1 flag

IE.2	EX1 – Enable external Interrupt 1. EX1 = 0 disables external interrupt 1 (int1_n). EX1 = 1 enables interrupts generated by the int1_n pin.
IE.1	ET0 – Enable Timer 0 Interrupt. ET0 = 0 disables Timer 0 interrupt (TF0). ET0 = 1 enables interrupts generated by the TF0 flag.
IE.0	EX0 – Enable External Interrupt 0. EX0 = 0 disables external interrupt 0 (int0_n). EX0 = 1 enables interrupts generated by the int0_n pin

2. Interrupt Priority Register

Table 4-4 Interrupt Priority Register (IP 0xB8H)

Interrupt Priority Register (IP)			Address: B8H					
	Bit7	6	5	4	3	2	1	Bit0
Read:	1	PS1	PT2	PS0	PT1	PX1	PT0	PX0
Write:	X							
Reset:	0	0	0	0	0	0	0	0

Bit	Description
IP.7	Reserved. Read as 1.
IP.6	PS1 – Serial Port 1 Interrupt Priority Control. PS1 = 0 sets Serial Port 1 interrupt (TI_1 or RI_1) to low priority. PS1 = 1 sets Serial Port 1 interrupt to high priority. PS1 is available only when the extended interrupt unit is implemented. Otherwise, it is read as 0. If the extended interrupt unit is implemented and Serial Port 1 is not implemented (serial < 2), PS1 is present but not used.
IP.5	PT2 – Timer 2 Interrupt Priority Control. PT2 = 0 sets Timer 2 interrupt (TF2) to low priority. PT2 = 1 sets Timer 2 interrupt to high priority. If Timer 2 is not implemented (timer2 = 0), PT2 is present but not used
IP.4	PS0 – Serial Port 0 Interrupt Priority Control. PS0 = 0 sets Serial Port 0 interrupt (TI_0 or RI_0) to low priority. PS0 = 1 sets Serial Port 0 interrupt to high priority. If Serial Port 0 is not implemented (serial = 0), PS0 is present but not used.
IP.3	PT1 – Timer 1 Interrupt Priority Control. PT1 = 0 sets Timer 1 interrupt (TF1) to low priority. PT1 = 1 sets Timer 1 interrupt to high priority
IP.2	PX1 – External Interrupt 1 Priority Control. PX1 = 0 sets external interrupt 1 (int1_n) to low priority. PT1 = 1 sets external interrupt 1 to high priority.
IP.1	PT0 – Timer 0 Interrupt Priority Control. PT0 = 0 sets Timer 0 interrupt (TF0) to low priority. PT0 = 1 sets Timer 0 interrupt to high priority.
IP.0	PX0 – External Interrupt 0 Priority Control. PX0 = 0 sets external interrupt 0 (int0_n) to low priority. PT0 = 1 sets external interrupt 0 to high priority.

3. External Interrupt Flag Register

Table 4-5 External Interrupt Flag Register (EXIF 0x91H)

External Interrupt Flag Register (EXIF)			Address: 91H					
	Bit7	6	5	4	3	2	1	Bit0
Read:	IF5	IF4	IF3	IF2	0	0	0	0
Write:					X	X	X	X
Reset:	0	0	0	0	0	0	0	0

Bit	Function
EXIF.7	IE5 – External Interrupt 5 Flag. IE5 = 1 indicates that a falling edge was detected at the int5_n pin. IE5 must be cleared by software. Setting IE5 in software generates an interrupt, if enabled.
EXIF.6	IE4 – External Interrupt 4 Flag. IE4 = 1 indicates that a rising edge was detected at the int4 pin. IE4 must be cleared by software. Setting IE4 in software generates an interrupt, if enabled.

EXIF.5	IE3 – External Interrupt 3 Flag. IE3 = 1 indicates that a falling edge was detected at the int3_n pin. It is generated by RTC. IE3 must be cleared by software. Setting IE3 in software generates an interrupt, if enabled.
EXIF.4	IE2 – External Interrupt 2 Flag. IE2 = 1 indicates that a rising edge was detected at the int2 pin. It is generated by EMU. IE2 must be cleared by software. Setting IE2 in software generates an interrupt, if enabled.
EXIF.3	Reserved. Read as 1.
EXIF.2-0	Reserved. Read as 0.

4. Extend Interrupt Control Register

Table 4-6 Extend Interrupt Control Register (EICON 0xD8H)

EICON			Address: D8H					
	Bit7	6	5	4	3	2	1	Bit0
Read:	SMOD1	1	EPFI	PFI	WDTI	0	0	0
Write:		X				X	X	X
Reset:	0	1	0	0	0	0	0	0

Bit	Function
EICON.7	SMOD1 – Serial Port 1 baud rate doubler enable. When SMOD1 = 1, the baud rate for Serial Port 1 is doubled
EICON.6	Reserved. Read as 1.
EICON.5	EPFI – Enable Power-Fail Interrupt. EPFI = 0 disables power-fail interrupt (pfi). EPFI = 1 enables interrupts generated by the pfi pin. Work with BPEN.
EICON.4	PFI – Power-Fail Interrupt Flag. PFI = 1 indicates a power-fail interrupt was detected at the pfi pin. It is generated by OCD. PFI must be cleared by software before exiting the interrupt service routine. Otherwise, the interrupt occurs again. Setting PFI in software generates a power-fail interrupt, if enabled.
EICON.3	WDTI – Watchdog Timer Interrupt Flag. WDTI = 1 indicates a watchdog timer interrupt was detected at the wdti pin. It is generated by LVI. WDTI must be cleared by software before exiting the interrupt service routine. Otherwise, the interrupt occurs again. Setting WDTI in software generates a watchdog timer interrupt, if enabled.
EICON.2-0	Reserved. Read as 0.

5. Extend Interrupt Enable Register

Table 4-7 Extend Interrupt Enable Register (EIE 0xE8H)

Extend Interrupt Enable Register (EIE)			Address: E8H					
	Bit7	6	5	4	3	2	1	Bit0
Read:	1	1	1	EWDI	EX5	EX4	EX3	EX2
Write:	X	X	X					
Reset:	1	1	1	0	0	0	0	0

Bit	Function
EIE.7-5	Reserved. Read as 1.
EIE.4	EWDI – Enable Watchdog Timer Interrupt. EWDI = 0 disables watchdog timer interrupt (wdti). EWDI = 1 enables interrupts generated by wdti pin.
EIE.3	EX5 – Enable External Interrupt 5. EX5 = 0 disables external interrupt 5 (int5_n , SPI or I2C). EX5 = 1 enables interrupts generated by the int5_n pin.
EIE.2	EX4 – Enable External Interrupt 4. EX4 = 0 disables external interrupt 4 (int4, Key Board).EX4 = 1 enables interrupts generated by the int4 pin.

EIE.1	EX3 – Enable External Interrupt 3. EX3 = 0 disables external interrupt 3 (int3_n, RTC). EX3 = 1 enables interrupts generated by the int3_n pin.
EIE.0	EX2 – Enable External Interrupt 2. EX2 = 0 disables external interrupt 2 (int2, EMU). EX2 = 1 enables interrupts generated by the int2 pin.

6. Extend Interrupt Priority Register (EIP)

Table 4-8 Extend Interrupt Priority Register (EIP) (EIP 0xF8H)

Extend Interrupt Priority Register(EIP)			Address: F8H					
	Bit7	6	5	4	3	2	1	Bit0
Read:	1	1	1	PWDI	PX5	PX4	PX3	PX2
Write:	X	X	X					
Reset:	1	1	1	0	0	0	0	0

Bit	Function
EIP.7-5	Reserved. Read as 1.
EIP.4	PWDI – Watchdog Timer Interrupt Priority Control. WDPI = 0 sets watchdog timer interrupt (wdti) to low priority. PS0 = 1 sets watchdog timer interrupt to high priority.
EIP.3	PX5 – External Interrupt 5 Priority Control. PX5 = 0 sets external interrupt 5 (int5_n) to low priority. PX5 = 1 sets external interrupt 5 to high priority.
EIP.2	PX4 – External Interrupt 4 Priority Control. PX4 = 0 sets external interrupt 4 (int4) to low priority. PX4 = 1 sets external interrupt 4 to high priority.
EIP.1	PX3 – External Interrupt 3 Priority Control. PX3 = 0 sets external interrupt 3 (int3_n) to low priority. PX3 = 1 sets external interrupt 3 to high priority.
EIP.0	PX2 – External interrupt 2 Priority Control. PX2 = 0 sets external interrupt 2 (int2) to low priority. PX2 = 1 sets external interrupt 2 to high priority.

7. Other interruption register

Other interrupt registers will be described in later chapters.

4.3 Interrupt Processing

CPU samples interrupt flag at the C4 time of every machine cycle, while looks up the sampled interrupt in the next machine period. If there is a interrupt flag at the C4 in the previous machine cycle, then it will detect the interrupt and process them according to interrupt priority, the interrupt system will control system transfer to the related interrupt service Routine(ISR). Any of the following 3 terms can lock the response of CPU to the interrupt.

1. CPU is processing the same level or higher level interrupt;
2. The current machine cycle is not the last machine cycle of current running instruction;
3. The current running instruction is returned (RETI) or read/write IP register instruction.

In the 3 terms above, the 2nd ensures running over the current instruction, the 3rd ensures running the next instruction before respond to the interrupt if the current running instruction is RETI or is visiting IE、IP instruction.

Interrupt lookup is executed repeatly in every machine period. The inquired state is the sample flag of the C4 time of the previous machine period. It is worth noticing that if interrupt flag is reset but does not respond for one of the above terms, and the above lock terms is canceld while the interrupt flag is not the reset status, the delayed interrupt will not be responsed and CPU will abandon the inquring results.

When CPU responds the interrupt, first places the responsed priority active trigger, lock the

same level and lower lever interrupt. Then base on the sorts of interrupt sources, under the control of hardware, program shifts to the related vector entrance unit and runs

When a permitted interrupt happens while hardware transfers the ISR, it push the PC's content into stack (but it can not automatically save the content of program status bit PSW) and load the entrance address of responsed ISR into PC. The entrance addresses of the 13 interrupt source service routine are listed in **table 4-1.** Generally, there is a jump instruction arranged at the entrance of the interrupt routine in order to jump to entrance of the user service routine.

If there is no higher interrupt happen. CPU will execute the interrupt service routine completely. The last instruction of interrupt service routine must be the RETI. After CPU executes this instruction over, clear 0 of the reset priority active trigger after responsed interrupt then pull two byte content(interrupt point address) from stack and load it into PC, CPU excutes the interrupted routine over again from the interrupt point.

4.4 Interrupt Enabling

The EA bit in the IE SFR (IE.7) is a global enable for all interrupts except the power-fail interrupt. When EA = 1, each interrupt is enabled/masked by its individual enable bit. When EA = 0, all interrupts are masked. The only exception is the power-fail interrupt, which is not affected by the EA bit. When EPFI = 1, the power-fail interrupt is enabled, regardless of the state of the EA bit.

Table 4-1provides a summary of interrupt sources, flags, enables, and priorities.

4.5 Interrupt Priorities

ATT7025 interruption system has 3 priority levels, OCD has the highest interruption priority, the other 12 interruptions are divided into high priority and low priority by IP and EIP register.

1. OCD can not be interrupted by other interrupts, the other 12 interrupts can be interrupted by high priority interruption sources while high priority sources can not be interrupted by any other interrupt sources(except OCD);

2. One interruption source, no matter high priority or low priority, once gets responsed, can not be interrupted by the same level interrupt source.

When it receives several same level interruptions at the same time, which interruption source gets responsed is decided by internal inquiring sequence. The priority list is layed the same level priority list in **table 4-1** .

It is worth noticing that RTC interrupt、EMU interrupt、SCI interrupt and LVI interrupt are all include several interrupt sources. For example, RTC interrupt flag register includes 8 interrupt flags: alarm clock interrupt, second timer interrupt, timer2 interrupt, timer1 interrupt, day interrupt, hour interrupt, minute interrupt and second interrupt. Users can judge RTC interrupt source via software inquiring mode and clear the 8 interrupt flags in ISR.;

4.6 Interrupt Response Time

Interruption response time is decided by ATT7025 running state. The fastest response time is 5 instruction cycles: detecting interrupt occupys 1 instruction period, LCALL of running to ISR occupys 4 instruction periods. When ATT7025 executes RETI instruction and the program

returned from the interrupt is following MUL or DIV instruction, the interrupt response time is the longest: 13 instruct cycles. Among the 13 cycles, detecting interrupt occupys 1 period, running RETI occupys 3 periods, running MUL or DIV instruction occupys 5 periods and running to LCALL of ISR occupys 4 periods. Then the interrupt response time is 13x4=52 system clock cycles (fsys).

5 Clock

5.1 Introduction

The clock system of ATT7025 has the following characteristics:

- Embedded three sorts clock oscillator circuit;
- Low power consumption design, flexible system clock configuration
- Build in system clock switch protect mechanism
- Clock solution for ammeter application

5.2 Function Description

5.2.1 Clock Oscillator Circuit

The ATT7025 includes three sorts of oscillator circuits:

- Internal RC oscillator circuit
- 32.768KHz low frequency crystal oscillator circuit
- External high frequency crystal oscillator circuit

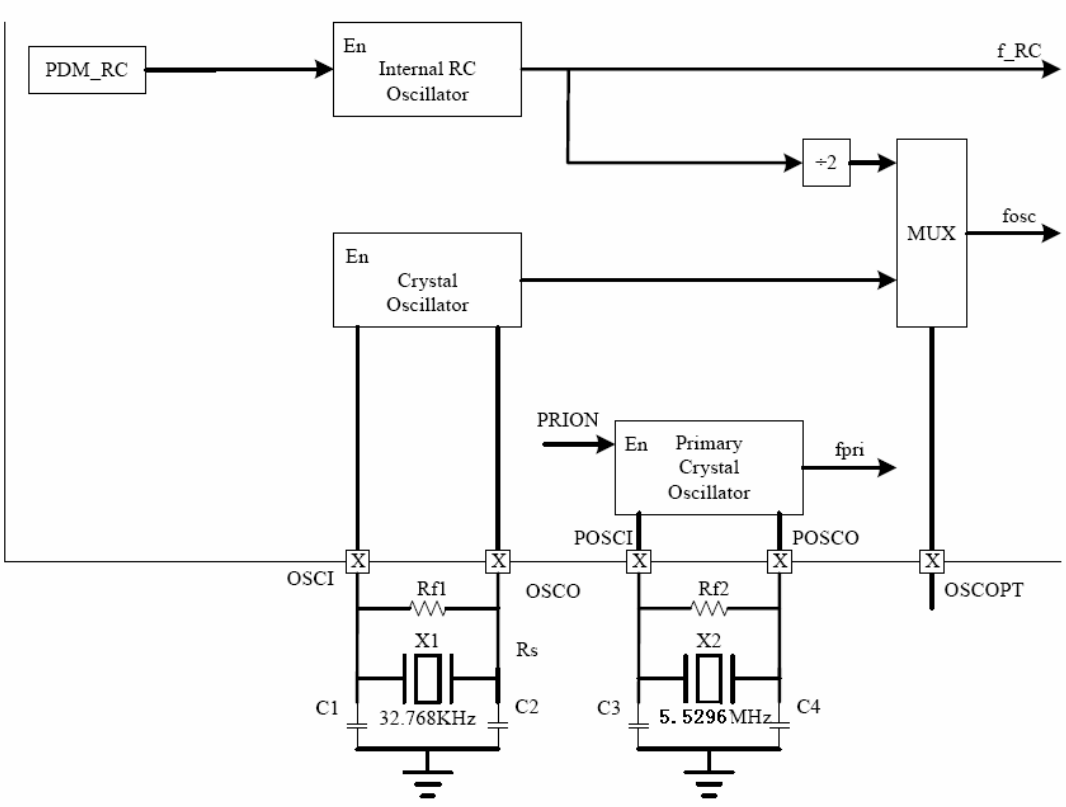


Figure 5-1 Clock oscillator

Low-frequency crystal oscillator circuit is designed for 32.768KHz crystal oscillator, see fig 5-1, OSCI is the crystal oscillator circuit input pin, OSCO is the crystal oscillator circuit output pin, in typical application circuit, X1 recommends 32.768KHz high precision crystal oscillator, C1、C2 select 15PF±10% porcelain capacitance, Rf1 selects 10M precision resistance. After power on reset,low-frequency crystal oscillator circuit starts working, outputs 32.768KHz clock, the oscillator circuit's work is neither affected by reset nor system running mode, low-frequency crystal oscillator circuit provides RTC's clock and also can be the system clock source in power

saving mode.

High-frequency crystal oscillator circuit is designed for 11.0592MHz/5.5296MHz/ 2.7648MHz/1.3824MHz external crystal oscillator, see **figure 5-1,** POSCI is the crystal oscillator circuit input pin, POSCO is the crystal oscillator circuit output pin, in typical application circuit, X2 recommends 5.5296MHz crystal oscillator, C3、C4 select 15PF±10% porcelain capacitance, Rf2 selects 10M precision resistance. External high-frequency crystal oscillator circuit is the clock source in normal mode.

Internal RC oscillator circuit is mainly used as the clock source for WDT, and also can be used as the input of system clock source fosc. Show as in **figure 5-1**, when it is used as system clock source, f_RC dimidiate frequency output is adopted. Fosc is Selected through OSCOPT pin, and OSCOPT Pin Build in Pull-up 30K resistance to VCC, so fosc is derived directly from 32.768KHz crystal oscillator by default; When OSCOPT pin is Pulled down externally, fosc is derived from f_RC, however, fosc is the dimidiate frequency of f_RC.

When user is using RTC, in order to ensure precision time, it is commended to use external 32.768KHZ crystal as the clock source of fosc. When user does not use ATT7025's RTC, internal RC oscillator can be used as the clock source of fosc which can spare external crystal oscillator circuit.

5.2.2 System Clock Generation

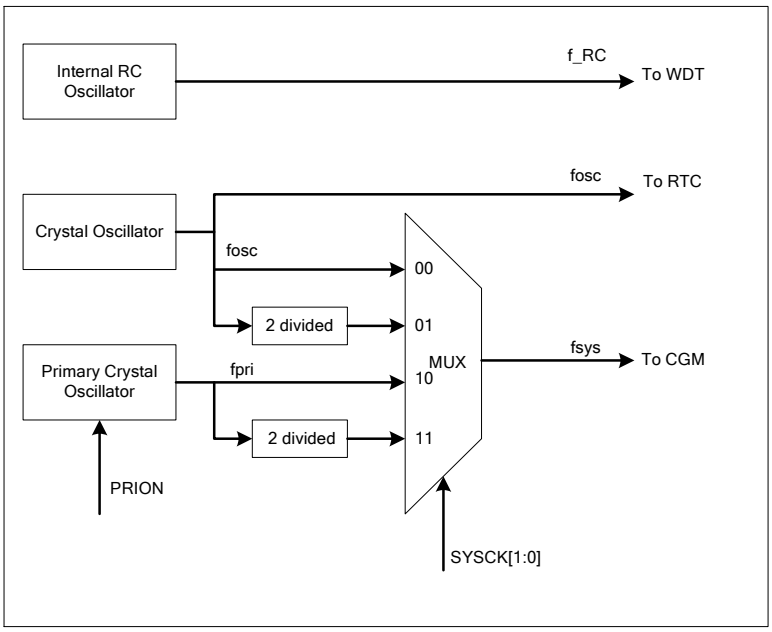


Figure 5-2 Block diagram of system clock generation

Fig 5-2 is the block diagram of system clock creation. As the figure shows, the system has two crystal oscillator circuits: low-frequency oscillator's output frequency is fosc and high-frequency oscillator's output frequency is fpri. The system clock fsys can cofig as fosc、fosc/2、fpri、fpri/2, accordingly.

After power on reset, system in PSM, on-chip low-frequency oscillator circuit starts working, system clock is derived from on-chip low-frequency oscillator circuit fosc, user can modify system clock to fosc、fosc/2 by set up SYSCK[1:0]; When SYSCK[1:0]=00, fsys=fosc; When SYSCK[1:0]=01, fsys=fosc/2.

5.2.2.1 System Clock Switches from Low-Frequency to High-Frequency

After reset, the high-frequency oscillator circuit closes by default, PRION(**table 5-5**) clears zero, but SYSCK1(**table 5-3)** clears zero means select fosc as the system clock. In order to ensure EMU module works at normal frequency, system clock needs to switch low-frequency to high-frequency clock. The switching process is as following:

1. User sets up PRIP1 and PRIP0 register according to external high-frequency crystal frequency, the main input frequencies of high-frequency crystal oscillator are 11.0592MHz, 5.5296MHZ, 2.7648MHz, and 1.3824MHz. Accordingly, PRIP1 and PRIP0 register can be set up according to **table 5-4.**

2. Configure PRION=1, enable high-frequency oscillator circuit.

3. Detect whether LOCK bit (**table 5-6**) is 1, LOCK=1 means high-frequency crystal oscillator is steady; LOCK=0 means high-frequency crystal oscillator is still in startup or is not enabled.

4. Configure SYSCK[1:0](**table 5-3)**, ensure the system clock is fpri or fpri/2. When SYSCK[1:0]=10, fsys=fpri; When SYSCK[1:0]=11, fsys=fpri/2, switch completes.

Here is an example for the switching process:

```
        MOV   9AH,#0C3H
        MOV   9AH,#98H          ;Disable Write protect
        MOV   CLKCFG,#00H       ; PRIIP[1:0]=00
        MOV   0BCH,#91H         ;PRION=1
LOCK:   MOV   A,0B6H
        JNB   ACC.7,LOCK        ;Judge if LOCK=1
        MOV   9AH,#0C3H         ;Disable Write protect
        MOV   9AH,#98H
        MOV   0BDH,#02H         ;sysck[1:0]=10b,fsys switch to fpri
```

The main input frequencies of high-frequency crystal oscillator are 11.0592MHz, 5.5296MHZ, 2.7648MHz, and 1.3824MHz. Then the alterable system clock that is derived from high-frequency oscillator has five frequencies: 11.0592MHz, 5.5296MHz, 2.7648MHz, 1.3824MHz and 0.6912MHz.

5.2.2.2 Build-in Protect Mechanism

In order to ensure the system stabilization when clock is switching, ATT7025 build in protect mechanism for clock switch. User should abide by the following rules when carrying on clock switching:

1． When PRION(**tab 5-5**) is set to 1, PRIP[1:0]**(table 5-4)** can not be changed.

2． When SYSCK1(**table 5-3)**＝1, it means select fpri or fpri/2 as system clock fsys and it can't disable high-frequency oscillator circuit at this moment, namely it can not clear PRION zero.

3． When clear PRION to 0, user can not set SYSCK1 1, i.e. user can not select fpri or fpri/2 as system clock when high-frequency oscillator circuit is disabled.

5.2.2.3 Switch from High-Frequency System Clock to Low-Frequency System Clock

When ATT7025 is powered by battery, system clock needs to switch high-frequency to low-frequency. The switching process is as following:

1． Configure SYSCK [1:0], make sure system clock is fosc or fosc/2. When SYSCK[1:0]=00,

fsys=fosc; When SYSCK[1:0]=01, fsys=fosc/2;

2． Configure PRION=0, disable high-frequency oscillator circuit, system clock switch completed.

The whole switching process is described by the following program:

```
MOV    9AH,#0C3H
MOV    9AH,#98H          ;Disable write protect
MOV    0BDH,#0           ;sysck[1:0]=00b,fsys switch to fosc
MOV    9AH,#0C3H
MOV    9AH,#98H
MOV    0BCH,#01H         ;prion=0
```

5.2.3 Clock solution for the Energy Meter

1．RTC clock

In order to ensure RTC time precision, RTC clock comes from external 32.768KHz low-frequency crystal oscillator circuit, RTC will never be shut up unless power off, mode switch (shift among Normal Mode、PSM、PDM) and clock switch will not affect RTC clock; Besides, RTC can also carry on digital compensation for low-frequency oscillator circuit by setting up crystal compensation register, eliminating affect caused by temperature excursion and power ripple on low-frequency oscillator circuit. The whole output registers (time & calendar), crystal compensation registers will not be disturbed by any reset, in order to ensure the RTC's precision.

2．WDT clock

In order to make sure the system works steadily, ATT7025 provides WDT independent RC oscillator clock source. RC oscillator works all the time either under CPU's PSM or normal mode, internal RC oscillator is controlled by PDM_RC bit(table 5-7) under PDM: when PDM_RC=1, internal RC oscillator opens under PDM, WDT works normally as PDM wake-up; When PDM_RC=0, internal RC oscillator closes, WDT closes under PDM.

3．EMU clock femu and fadc

EMU clock comes from system clock. It can adjust automatically according to external high-frequency crystal frequency.

1）When system clock fsys comes from external low-frequency crystal oscillator frequency, i.e., fsys=fosc or fsys=fosc/2, femu=fsys. EMU doesn't work accurately.

2）When system clock comes from the output of high-frequency oscillator circuit, i.e., fsys=fpri or fsys=fpri/2, the femu and fadc will adjust automatically according to high-frequency oscillator circuit option PRIP[1:0]. As the table below shows:

Table 5-1 EMU Clock Configure

PRIP[1:0]		SYSCK0	fpri	fsys	N	femu=fsys/N	fadc=femu/6
0	0	0	11.0592MHz	11.0592MHz	2	5.5296MHz	921.6 KHz
		1	11.0592MHz	5.5296MHz	1	5.5296MHz	921.6 KHz
0	1	0	5.5296MHz	5.5296MHz	1	5.5296MHz	921.6 KHz
		1	5.5296MHz	2.7648MHz	1	2.7648MHz	460.8 KHz
1	0	0	2.7648MHz	2.7648MHz	1	2.7648MHz	460.8 KHz
		1	2.7648MHz	1.3824MHz	1	1.3824MHz	230.4 KHz
1	1	0	1.3824MHz	1.3824MHz	1	1.3824MHz	230.4 KHz
		1	1.3824MHz	0.6912MHz	1	0.6912MHz	115.2 KHz

5.3 Registers

Table 5-2 System Clock Management Register List

Address	Name	Reset Value	Description
0xBD	CLKCFG	0x00	Clock Configure Register －see **table 5-3,write-protect**
0xBC BORCFG.7	PRION	0	PRION Control Bit－see **table 5-5,,write-protect**
0xB6 SYSSCR.7	LOCK	0	LOCK State Bit－see **table 5-6**
0xBC BORCFG.1	PDM_RC	0	PDM_RC Control Bit－see **table 5-7,write-protect**

1．Clock Configure Register（write-protect ）

Table 5-3 Clock Configure Register（0xBDH,CLKCFG.）

CLKCFG			Address: BDH					
	Bit7	6	5	4	3	2	1	Bit0
Read: Write:	WDTS2	WDTS1	WDTS0	WDTEN	PRIP1	PRIP0	SYSCK1	SYSCK0
Reset:	0	0	0	0	0	0	0	0

Note :PRIP[1:0] is used to configured the input frequency of the high frequency crystal oscillator.

Table 5-4 PRIP[1:0] and fpri corresponding list

fpri	PRIP1	PRIP0
11.0592MHz	0	0
5.5296MHz	0	1
2.7648MHz	1	0
1.3824MHz	1	1

SYSCK[1:0] is used to choose the system clock

SYSCK1	SYSCK0	fsys
0	0	fsys=fosc
0	1	fsys=fosc/2
1	0	fsys=fpri
1	1	fsys=fpri/2

2．PRION Control Bit （ write-protect ）

Table 5-5 PRION control bit（0xBCH,BORCFG.7）

BORCFG			Address: BCH					
	Bit7	6	5	4	3	2	1	Bit0
Read:	PRION	WKRST	BORPDM	BORRST	BORVS1	BORVS0	PDM_RC	1
Write:								X
Reset:	0	0	0	1	0	0	0	1

Note :PRION=1: turn on the circuit function of the high frequency crystal oscillator;PRION＝0: turn off the circuit function of the high frequency crystal oscillator.

3．LOCK Control Bit

Table 5-6 LOCK control bit（0xB6H,SYSSCR.7）

SYSSCR			Address: B6H					
	Bit7	6	5	4	3	2	1	Bit0
Read:	LOCK	BOROUT	LVDOUT	0	0	0	0	0
Write:	x	x	x	X	WDTCLR3	WDTCLR2	WDTCLR1	WDTCLR0
Reset:	0	0	0	0	0	0	0	0

Note : LOCK=1 shows the high frequency crystal oscillator is steady;LOCK=0 shows the high

frequency crystal oscillator is on startup on is not turned on.

4. PDM_RC Control Bit（write-protect）

Table 5-7 PDM_RC control bit

BORCFG			Address: BCH					
	Bit7	6	5	4	3	2	1	Bit0
Read: Write:	PRION	WKRST	BORPDM	BORRST	BORVS1	BORVS0	PDM_RC	X
Reset:	0	0	0	1	0	0	0	0

When PDM_RC=1, the interior surge current is turned on in PDM mode; when PDM_RC=0, the interior surge current is turned off in PDM mode

6 System Reset

6.1 Introduction

The ATT7025 supports 5 types of reset:

- Power-On Reset(POR)
- external /RST pin reset
- WDT Reset(WDTR)
- BrownOut Reset(BOR)
- PDM wake-up reset (WKR)

This chapter will describe POR, external /RST pin reset and WDTR.

when any reset occur,CPU52 program pointer point to 0000H, all registers reset to default value and external pin reset to default status

6.2 Function Description

6.2.1 POR

When power supply imposes on the chip, power on reset will happen. When it happens, system sets up POR flag bit of RSTSR register to 1, clears other reset flag to 0 at the same time. Reading this register can reset register (clear zero after reading), including POR flag.

6.2.2 /RST Pin Reset

When there is low level in external reset pin, system will reset which set RST flag bit in reset status register, reading this register can clear RSTR to zero, including RST flag bit.

/RST pin contain 30K pull-up resistance, when power on, /RST pin is at high level.In order to ensure system stability, user can add external pull-up resistance on /RST pin.

6.2.3 WDTR

Watchdog Timer is a special timer, it count according to RC oscillator's output frequency f_RC, output pulse when counter is overflow, and then Watchdog cause reset. If Watchdog Timer clears to zero before counter overflow, then Watchdog will not cause reset.

The following characteristics were designed in ATT7025 in order to impoving the stability of WDT:

- adopt hardware watchdog design
- Build in RC oscillator provides independent clock for WDT
- WDT can be opened or closed under PDM

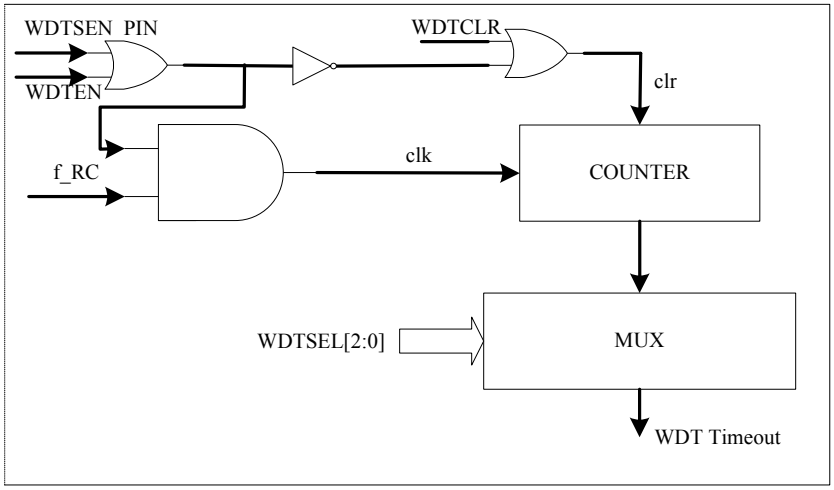


Fig 6-1 block diagram of WDT

Figure 6-1ist the block diagram of WDT. As shown in the figure, WDT adopts comparatively high stable hardware watchdog design. WDT enable bit is determined by both WDTEN bit of SYSCR register and external WDTSEN PIN status. When WDTSEN PIN is pulled up, no matter WDTEN is 0 or 1, WDT enables; When WDTSEN PIN is pulled down,if WDTEN=1, WDT enable, when WDTEN=0, which means disable WDT and furthermore clearing WDT Counter to zero. After reset, the default status of WDTEN bit is 0, the default status of WDTEN PIN is high. Generally, it pushes WDTSEN PIN down when user is in debug mode, and pulls it up in mass production.

It can select WDT value by setting up WDTS[2:0]（**table 6-3**）, timer has 8 options: 31.25ms、62.5ms、125ms、250ms、500ms、1.0s、2.0s、4.0s. WatchDog Timer overflow will result in system reset, the WDTR set WDT bit of reset status register (**table 6-2)**, reading this register can clear this register (clear zero after reading), including WDT flag bit.

Writing 0110 to WDTCLR[3:0](**table 6-5**) can clear WDT to zero. Other writing data is invalid.

Under PDM, the WDT input clock RC oscillator can be selected to be closed (PDM_RC=0) or to be opened (PDM_RC=1) by setting up PDM_RC bit(**table 5-7**) before entering into PDM.

If WDT is closed(PDM_RC=0) before entering into PDM, WDT will clears to zero.In this way, CPU52 start counting from 0 after PDM is waked up. If WDT is opened (PDM_RC=0) before entering into PDM, WDT continues counting until overflow result in WDTR which will wake up and reset CPU52 from PDM.

6.3 Registers

Table 6-1 reset register list

Address	Name	Reset value	Function
0xB7	RSTSR	0x80	Reset flag register－see **table 6-2**
0xBD CLKCFG.7-5	WDTS[2:0]	000	WDT overflow time control bit－see table **6-3**,write-protect
0xBD CLKCFG.4	WDTEN	0	WDT enable bit － see **table 6-4**,,write-protect

0xB6 SYSSCR.3-0	WDTCLR[3:0]	0000	WDT clear control bit－see **table 6-5**

1. Reset flag register

Tale 6-2 Reset flag register (0xB7H,RSTSR)

RSTSR			Address: B7H					
	Bit7	6	5	4	3	2	1	Bit0
Read:	POR	RST	WDT	BOR	WKR	0	0	0
Write:	x	x	x	x	x	x	x	x
Reset:	1	0	0	0	0	0	0	0

Bit	Function
RSTSR.7	POR: power-on reset flag. When power on reset,set the flag POR 1and clear the other flags. This register can be clear (including the POR flag) after reading. Clear after reading.
RSTSR.6	RST: /RST pin reset flag. When the external resetpin /RST has the low voltage pulse wider than 2us, the RST PIN reset is caused and the reset flag bit RST is set 1. Clear to zero after reading.
RSTSR.5	WDT: WDT overflow reset flag. When the WatchDog Timer overflows, the WDT reset is produced and, the WDT reset flag WDT is set 1.Clear to zero after reading.
RSTSR.4	BOR: Brow-out reset flag. When AVCC is lower than the enactment voltage Vborl, the BOR reset is produced and the BOR reset flag BOR of the reset flag register is set 1.Clear to zero after reading.
RSTSR.3	WKR: PDM reset wake up flag. The system can be waked up by int0_n, int1_n, RX0, RX1, RTC, WDT, RST PIN when in PDM mode and then the reset flag register WKR is set to 1.Clear to zero after reading.
RSTSR.2-0	Reserved. Read as 0.

2. WDT overflow time control bit （write-protect）

Table 6-3 WDT overflow time control bit (0xBDH,CLKCFG.7-4)

CLKCFG			Address: BDH					
	Bit7	6	5	4	3	2	1	Bit0
Read: Write:	WDTS2	WDTS1	WDTS0	WDTEN	PRIP1	PRIP0	SYSCK1	SYSCK0
Reset:	0	0	0	0	0	0	0	0

WDTS[2:0] is used to choose the WDT overflow time:

WDTS2	WDTS1	WDTS0	Overflow time
0	0	0	500ms
0	0	1	1.00s
0	1	0	2.00s
0	1	1	4.00s
1	0	0	31.25ms
1	0	1	62.5ms
1	1	0	125ms
1	1	1	250ms

3. WDT enable bit（write-proect）

Table 6-4 WDT enable bit (0xBDH,CLKCFG.4)

CLKCFG			Address: BDH					
	Bit7	6	5	4	3	2	1	Bit0
Read: Write:	WDTS2	WDTS1	WDTS0	WDTEN	PRIP1	PRIP0	SYSCK1	SYSCK0
Reset:	0	0	0	0	0	0	0	0

Note :When the WDTSEN PIN is pulled high,the WDT is enable no matter that WDTEN=0 or

WDTEN=1;when WDTSEN PIN is pulled low,WDTEN=1,enable WDT,WDTEN=0 will turn off WDT count and clear the WDT Counter.

4. WDT clear control bit

Table 6-5 WDT clear control bit (0xB6H,SYSSCR.3-0)

SYSSCR			Address: B6H					
	Bit7	6	5	4	3	2	1	Bit0
Read:	LOCK	BOROUT	LVDOUT	0	0	0	0	0
Write:	x	x	x	x	WDTCLR3	WDTCLR2	WDTCLR1	WDTCLR0
Reset:	0	0	0	0	0	0	0	0

Note: writing 0110 to WDTCLR[3:0] may clear the WDT. Writeing other data is invalid.

7 Power Supply System

7.1 Introduction

The ATT7025 power supply system has the following characteristics:

- External 3.3V single power supply;
- Support Borwn out reset, enhance the power supply system stability;
- Support low voltage detecting, monitor battery voltage in real time.

7.2 Function Description

7.2.1 Power Supply System

The ATT7025 uses external 3.3V single power supply mode. The VCC and GND pins on ATT7025 are the digital power input and digital ground of the digital part of this chip; AVCC and AGND pins are the analog power input and analog ground of the analog part..GND and AGND should be conneted at one point on PCB.

7.2.2 BOR

In order to enhance the stability of power supply system, the ATT7025 build in BOR (Borwm out reset) unit, BOR unit has the following characteristics:

- Support four optional power down voltage thresholds;
- BOR reset or interrupt is alternative;
- Support low power consumption design, BOR working in PDM is optional.

7.2.2.1 Brown Out Reset

BOR circuit detects the voltage on power input pin AVCC, if voltage on AVCC is lower than Vbor, system is forced to reset, the reset flag BOR(**table 6-2**) in reset status register is set, read this register can clear it including the BOR flag (cleared after read).

Clearing PDBOR (**table 7-2**) can enable the BOR detecting circuit. After reset, PDBOR=0, BOR is turned on.

Set BORRST bit (**table 7-3**), BOR is config as power down reset mode. Here, if BOR detects that AVCC is lower than Vborl, then it generates BOR Reset signal and sets BOROUT (**table 7-4**) at the same time.

The BOR detect voltage threshold value can be configured by BORVS[1:0]（**table 7-3**）. The default mode is VCC＝2.15V when power on. It can be set to work in another mode by software, but it has to be configured again after power on. If AVCC is lower than the Vbor value of the set mode, reset signal will be generated until AVCC is higher than Vbor＋100mV, when AVCC is higher than Vbor＋100mV, BOROUT is clear. When VCC drops close to 0V, it will trigger BOR again.

7.2.2.2 BOR Interrupt

When BORRST=0, BOR is used as a BOR interrupt If enable BOR interrupt, once BOROUT changes, such as AVCC drops below Vbor or AVCC raising above Vbor+100mV, BOR interrupt will be triggered. BOR enable interrupt is described in BORIE Control bit(**table 7-5**).

When BOR interrupt occurs, BOR interrupt Flag BORIF is set, then interrupt system switch to BOR Service Routine. (Interrupt vector 0x0063H). Before exiting ISR, users should clear the BOR interrupt with software. The process of interrupt clear is explained in BORIF Control Bit

description (table 7-6).

7.2.2.3 BOR Low Power Consumption Design

In order to reduce the power consumption of PDM, before entering into the PDM mode , PDBOR and BORPDM control bits （table 7-2 and table 7-3) may be used to turn off BOR circuit. If the BOR circuit is turned on before entering PDM mode, the BOR circuit will go on working in PDM mode, If enable BOR interrupt or reset and BOR occur, the CPU52 will exit the PDM mode. If the BOR interrupt and reset occur at the same time, the BOR interrupt will be not triggered since reset has the higher priority than interrupt.

7.2.3 LVD

The embedded LVD circuit of ATT7025 detects the voltage on LVDIN pin or AVCC pin in real time. In energy meter design, the battery voltage is usually connected to LVDIN pin through a resistor used for voltage divider, so that LVD can monitor battery voltage in real time.

LVD has the following characteristics:

- LVD interrupt is selectable;
- Detecting LVDIN pin voltage or AVCC voltage is selectable;
- Support 12 optional AVCC voltage thresholds

The operation of LVD is described as following:

PDLVD control bit (table 8-2) controls LVD, PDLVD =0 indicates turning on LVD unit; PDLVD =1 indicates turning off LVD unit; After reset, PDLVD=0, LVD is turning on.

LVDVS[3:0](table 7-7) configures the threshold of LVD, when LVDVS[3:0]=11XX, LVD monitors the input voltage of LVDIN and the voltage threshold is 1.20V; When LVDVS[3:0]=0000～1011, LVD monitors the voltage of AVCC and the voltage threshold is divided into 12 levels ranging from 2.10V to 3.50V. It Note the relationship between LVDVS[3:0] register and the power monitored power supply threshold of LVD shown in Table 7-8, pay attention that when LVD is turn on, LVDVS[3:0]=11xx and LVDIN is configured as monitor power supply input, P2.4/LVDIN is configured as LVDIN,instead of the I/O port.

When LVDVS[3:0] =0000~1011, AVCC drops below LVD power down threshold, or when LVDVS[3:0]=11XX, the input voltage of LVDIN PIN drops below LVD power down threshold, LVDOUT(table 7-9)=1; when LVDVS[3:0]=0000~1011, AVCC rises above LVD power down threshold, or when LVDVS[3:0]=11XX, the input voltage on LVDIN PIN rises above LVD power down threshold, LVDOUT=0.

LVDIE(table 7-10) enable LVD interrupt, LVDIE and EWDI(SFR 0xE8H, EIE.4) should be use together, if EWDI=0 or LVDIE=0, LVD interrupt is forbidden; If EWDI=1 and LVDIE＝1, enable LVD interrupt. If enable LVD interrupt, then every time LVDOUT changes (AVCC drops or LVDIN drops below threshold and rises above threshold), LVD interrupt will occur.

When LVD interrupt occurs, system will set LVD interrupt flag bit LVDIF(table 7-11). Interrupt system will switch to LVD interrupt service routine (interrupt vector 0x0063H). Before quitting ISR, user need clear LVD interrupt in ISR, see the clear process in LVDIF control bit description.

7.3 Registers

Table 7-1 Power Supply Manage Register List

Address	Name	Reset Value	Description
0xBF SUPDC.4	PDBOR	0	PDBO Control Bit — see **table 7-2, write-protect**
0xBC	BORCFG	0x11	BOR Configure Register—see **table 7-3, write-protect**
0xB6 SYSSCR.4	BOROUT	0	BOROUT Flag Bit—see **table 7-4**
0xAC LVIIE.0	BORIE	0	BOR Interrupt Enable Bit—see**table 7-5**
0xB4 LVIIF.0	BORIF	0	BOR Interrupt Flag Bit—see**table 7-6**
0xB5	LVDCON	0x00	LVD Control Register—see **table 7-7**
0xB6 SYSSCR. 5	LVDOUT	0	LVDOUT Flag Bit—see **table 7-9**
0xAC LVIIE.1	LVDIE	0	LVD Interrupt Enable Bit—see **table 7-10**
0xB4 LVIIF.1	LVDIF	0	LVD Interrupt Flag Bit—see **table 7-11**

1. PDBOR Control Bit （write-protect ）

Table 7-2 PDBOR Control Bit (0xBFH, SUPDC.4)

System Unit Power-Down Control Register (SUPDC)			Address: BFH					
	Bit7	6	5	4	3	2	1	Bit0
Read:	0	PDTPS	PDEMU	PDBOR	PDLVD	PDLCD	PDI2C	PDSPI
Write:	x							
Reset:	0	0	1	0	0	1	1	1

Note: the PDBOR is the control enable bit of BOR in the Normal mode and PSM. PDBOR=0: Turn on the BOR mode in the Normal mode and PSM; PDBOR=1: Turn off the BOR mode in the Normal mode and PSM.

2. BOR Configure Register （write-protect ）

Table 7-3 BOR Configure Register (0xBCH)

BORCFG			Address: BCH					
	Bit7	6	5	4	3	2	1	Bit0
Read:	PRION	WKRST	BORPDM	BORRST	BORVS1	BORVS0	PDM_RC	1
Write:								x
Reset:	0	0	0	1	0	0	0	1

<table>
<tr><th>Bit</th><th>Function</th></tr>
<tr><td>BORCFG.5</td><td>BORPDM: BORPDM is the control enable bit of the BOR in the PDM mode. BORPDM=0:Turn off the BOR module in the PDM mode;BORPDM=1:Turn on the BOR module in the PDM mode;
The detail conditions shows as follow:
<table>
<tr><th>PDBOR</th><th>BORPDM</th><th>The state of the BOR module in Normal mode and PSM mode</th><th>The state of the BOR module in PDM mode</th></tr>
<tr><td>1</td><td>1</td><td>Turned off</td><td>Turned off</td></tr>
<tr><td>1</td><td>0</td><td>Turned off</td><td>Turned off</td></tr>
<tr><td>0</td><td>1</td><td>Turned on</td><td>Turned on</td></tr>
<tr><td>0</td><td>0</td><td>Turned on</td><td>Turned off</td></tr>
</table></td></tr>
<tr><td>BORCFG.4</td><td>BORST: The Reset and Interrupt select Bit of BOR. When BORRST=1,if the</td></tr>
</table>

	AVCC is lower than the Vborl then the BOR reset is caused ; when BORRST=0,if the AVCC is lower than the Vborl or is higher then the Vborh,the BOR interrupt is caused.
BORCFG.3-2	BORVS[1:0]:BOR Voltage threshold Configure Bit When AVCC < BOR voltage threshold, the BOR interrupt or the BOR reset is caused.

BORVS1	BORVS0	BOR Examination Voltage
0	0	2.15 v mode
0	1	2.35 v mode
1	0	2.55 v mode
1	1	2.75 v mode

3. BOROUT Flag Bit

Table 7-4 BOROUT Flag Bit (0xB6H, SYSSCR.4)

SYSSCR			Address: B6H					
	Bit7	6	5	4	3	2	1	Bit0
Read:	LOCK	BOROUT	LVDOUT	0	0	0	0	0
Write:	x	x	x	X	WDTCLR3	WDTCLR2	WDTCLR1	WDTCLR0
Reset:	0	0	0	0	0	0	0	0

Note: BOROUT=1: AVCC is lower than BOR power down threshold; BOROUT=0: AVCC is higher than BOR power down threshold.

4. BOR Interrupt Enable Bit

Table 7-5 BOR Interrupt Enable (0xACH, LVIIE.0)

LVI Interrupt Enable Register (LVIIE)			Address: ACH					
	Bit7	6	5	4	3	2	1	Bit0
Read:	0	0	0	0	0	0	LVDIE	BORIE
Write:	X	X	X	X	X	X		
Reset:	0	0	0	0	0	0	0	0

Note: using combined with the EWDI（SFR 0xE8H,EIE.4）and BORRST control bit; When BORRST=1or EWDI=0 or BORIE=0, BOR interrupt is disable; when BORRST=0, EWDI=1 and L BORIE=1, BOR interrupt is enable.

5. .BOR Interrupt Flag

Table 7-6 BOR Interrupt Flag (0xB4H, LVIIF.0)

LVI Interrupt Flag Register (LVIIF)			Address: B4H					
	Bit7	6	5	4	3	2	1	Bit0
Read:	0	0	0	0	0	0	LVDIF	BORIF
Write:	X	X	X	X	X	X		
Reset:	0	0	0	0	0	0	0	0

Note: Setting the BOR interrupt flag will trigger the BOR interrupt ,The BOR interrupt clear bit and the WDTI flag bit (0xD8H SFR EICON.3）is combined to use . Write 1 into the BORIF and the BORIF is clear. Besides the BORIF, the WDTI is also clear by software. If the software set the WDTI, the LVI Interrupt occurs

6．LVD Control Register

Table 7-7 LVD Control Register (0xB5H, LVDCON)

LVDCON			Address: B5H					
	Bit7	6	5	4	3	2	1	Bit0
Read:	LVDVS3	LVDVS2	LVDVS1	LVDVS0	0	0	0	0
Write:					x	x	x	x
Reset:	0	0	0	0	0	0	0	0

Note: Table 7-8 define the LVD threshold through LVDVS[3:0] configuration.when

LVDVS[3:0]=11XX,LVD monitors the input voltage of the LVDIN PIN and the threshold is 1.20V; when LVDVS[3:0]=0000～1011, LVD monitors the input voltage of the AVCC and the threshold is divided into 12 levels ranging from 2.10V to 3.50V

Table 7-8 LVD Threshold

LVDVS3	LVDVS2	LVDVS1	LVDVS0	LVD Voltage Level
0	0	0	0	AVCC = 2.10 v
0	0	0	1	AVCC = 2.20 v
0	0	1	0	AVCC = 2.30 v
0	0	1	1	AVCC = 2.40 v
0	1	0	0	AVCC = 2.50 v
0	1	0	1	AVCC = 2.65 v
0	1	1	0	AVCC = 2.80 v
0	1	1	1	AVCC = 2.90 v
1	0	0	0	AVCC = 3.05 v
1	0	0	1	AVCC = 3.20 v
1	0	1	0	AVCC = 3.35 v
1	0	1	1	AVCC = 3.50 v
1	1	X	X	LVDIN = 1.20 v

7．LVDOUT Flag Bit

Table 7-9 LVDOUT Flag Bit (0xB6H, SYSSCR.5)

SYSSCR			Address: B6H					
	Bit7	6	5	4	3	2	1	Bit0
Read:	LOCK	BOROUT	LVDOUT	0	0	0	0	0
Write:	x	x	x	x	WDTCLR3	WDTCLR2	WDTCLR1	WDTCLR0
Reset:	0	0	0	0	0	0	0	0

Note:when LVDVS[3:0]=0000～1011,AVCC drops below the power down threshold of LVD,or when LVDVS[3:0]=11XX,the input voltage of the LVDIN PIN drops under the LVD power down threshold,LVDOUT=1;when LVDVS[3:0]=0000～1011,AVCC rises above the LVD power down threshold or when LVDVS[3:0]=11XX,the LVDIN PIN input voltage rises above the LVD power down threshold,LVDOUT=0.

8. LVD Interrupt Enable Bit

Table 7-10 LVD Interrupt Enable Bit (0xACH, LVIIE.1)

LVI Interrupt Enable Register (LVIIE)			Address: ACH					
	Bit7	6	5	4	3	2	1	Bit0
Read:	0	0	0	0	0	0	LVDIE	BORIE
Write:	X	X	X	X	X	X		
Reset:	0	0	0	0	0	0	0	0

Note:using combined with the EWDI（SFR 0xE8H,EIE.4）,when EWDI=0 or LVDIE=0,disable the LVD interrupt;when EWDI=1 and LVDIE＝1, enable the LVD interrupt.

9. LVD Interrupt Flag

Table 7-11 LVD Interrupt Flag (0xB4H, LVIIF.1)

LVI Interrupt Flag Register (LVIIF)			Address: B4H					
	Bit7	6	5	4	3	2	1	Bit0
Read:	0	0	0	0	0	0	LVDIF	BORIF
Write:	X	X	X	X	X	X		
Reset:	0	0	0	0	0	0	0	0

Note：when the system triggers the LVD interrupt, set the LVD interrupt flag LVDIF. The LVD interrupt clear bit and the WDTI flag bit 0xD8H SFR EICON.3）is combined to use . Write 1 into

the LVDIF and the LVDIF is clear. Besides the LVDIF, the WDTI is also clear by software. If the software set the WDTI, the LVI interrupt occurs.

8 Low Power Modes

8.1 Introduction

In order to reduce the system power consumption, the ATT7025 support three operation modes:

- Normal mode
- Power saving mode(PSM)
- Power Down mode (PDM)

The normal mode is suitable for AC power supply. When the AC power shut off, System should switch the normal mode to the power down mode and uses the battery power supply, CPU stop running in the power down mode.

Under the circumstance that saving data when AC power down, or PDM wake-up reset occurs, or the CPU run when using battery power supply (for example: reading the meter when AC power is shut off) and so on, System should switch to the power saving mode.

The ATT7025 support flexible and seamless switching mechanisms between different operation modes through relative register configuration.

The decrease of the system power consumption is mainly determined by the suitable application program design in which the power and clock of the periphery circuit that is not needed for working can be turned off. This charpter provides some application guidelines for reducing power consumption.

8.2 The Operation Modes

8.2.1 Power Saving Mode

The clock management in the PSM

1. In PSM, the system clock comes from the on-chip low frequency crystal oscillator circuit. Users can configure the system clock as fosc or fosc/2 through SYSCK[1:0]（table 5-3）.
2. In PSM,user can select to turn on or turn off the EMU and the ADC clock through configuring PDEMU（table 8-2）.But after turning on the EMU and the ADC clock,the EMU and the ADC clock comes from the system clock（fosc or fosc/2）which cause the EMU works abnormaly. So considering the power conumption and the EMU application, it is not recommend to turn on the EMU and the ADC in PSM. After reset,PDEMU＝1,the EMU and the 3-route ADC clock are turned off.
3. In PSM,user can select to turn on or turn off the TPS, LCD, SPI, and I2C clocks through configuring the PDTPS, PDLCD, PDSPI, and PDI2C control bits of the SUPDC register（table 8-2）. After reset, the control bit of the PDLCD, PDSPI, and PDI2C are 1 and the LCD, SPI, and I2C clocks are turned off. The PDTPS control bit is 0 and the TPS is turned on by default.
4. In PSM,the high frequency oscillator circuit is turned off by default.it is recommed to turn on the high frequency oscillator circuit through setting PRION（table 5-5）only before switching the PSM to the Normal mode.

The power management in PSM:

In PSM,users can choose to turn on or turn off the TPS、ADC、BOR、LVD、LCD module

power through configuring the control bits PDTPS、PDEMU、PDBOR、PDLVD、PDLCD of the SUPDC register （table 8-2）.

After reset, the PDEMU、PDLCD are 1 and the ADC、LCD powers are turned off;the PDTPS、PDBOR、PDLVD are 0 and the TPS、BOR、LVD powers are turned on. It is recommend to turn on BOR in PSM considering the power cost and the application. The TPS、LCD、LVD powers are turned on only when using .

Under the typical test condition ,fsys=32.768KHz,V_{CC}=3.3V, LCD is turned on and the TPS、ADC、BOR、LVD、I2C, SPI are turned off, the system current can fall to 70-80uA.

8.2.2 Normal Mode

The Normal mode is suitable for the AC power supply and is the usual operation mode of the system. In Normal mode, the system clock is provided by high frequency clock ,the CPU is running on full speed and the EMU works normally.

The clock management in Normal mode:

1. In Normal mode,the system clock comes from the on-chip high frequency crystal oscillator circuit and users can configure the syetem clock as fpri、fpri/2 through SYSCK[1:0] （table 5-3）.
2. Considering the energy measure application,user must turn on the clock of the EMU and the ADC to make them work normally through configuring PDEMU（table 8-2）=0
3. In Normal mode,users can select to turn on or turn off the clock of TPS、LCD、SPI、I2C through configuring PDTPS、PDLCD、PDSPI、PDI2C control bits（table 8-2） .

The power management in Normal mode

1. For the energy measurement , user must turn on the EMU and the 1、3 channel ADC through PDEMU（table 8-2）after entering into Normal mode by clock switching. If the anti-tamper function is required,the 2 channel ADC should be turned on through configuring ADC2ON control bit （table 9-47）.
2. In Normal mode,users can select to turn on or to turn off the power of TPS、BOR、LVD、LCD through configuring the PDTPS、PDBOR、PDLVD、PDLCDcontrol bits（table 8-2）,

Under the typical test condition , fsys=5.5MHz,fadc=450KHz, V_{CC}=3.3V,the other modules are at default state .The system power consumption can reach 5～6mA。

8.2.3 Power Down Mode

When the AC power is shut off, the operation mode should switch to the power down mode and the power swith to the battery power supply.

The clock management in PDM:

1. In PDM,the system clock is turned off and the CPU52（including UART and Timer） stop working . The EMU、ADC、SPI、I2C、TPS、38k module stop working for their module clock come from the system clock.

2 . In PDM, Low frequency oscillating circuit still works. And RTC work normally for its clock is provided by fosc.

3 Users can configure the RC Oscillator to be turned on or turned off through PDM_RC control bit（table 5-7）.Whether The WDT is turned on or turned off is determined by the RC Oscillator state.

4 In PDM, the LCD work state is determined by the configuring of the PDLCD（table 8-2） before entering into PDM

The power management in PDM:

1. In PDM, CPU52, Flash, XRAM, ROM, EMU, I2C, SPI, PWM and ICE（on-chip ICE support）are closed. The data in XRAM and EMU are lost,so the user programme should save the important data into SRAM or external E2PROM before entering into PDM; the SFR of CPU52、EMU、I2C、SPI、PWM、ICE(on-chip ICE support） is initialized after the PDM wake-up reset occurs.
2. The PDM_RC control bit can configure the RC Oscillator to be turned on or off before entering PDM. Whether the WDT works in PDM is determined by the RC Oscillator on-off state.
3. In PDM , BOR can be configurde to be turned on or off by PDBOR and BOR_PDM （**table7-3**） before entering into PDM.
4. In PDM, TPS、LVD、LCD powers can be configured to be turned on or off by PDTPS、PDLVD and PDLCD control bits before entering into PDM.
5. In PDM,the power supply of OSC、SRAM、POR、RTC、WDT is normal.

Under the typical test condition, the user programme turns off all the modules that can be closed before entering into PDM, only OSC and RTC are at work ,The system power consumption can drops to 2-3uA。

8.3 Transition between Operating Modes

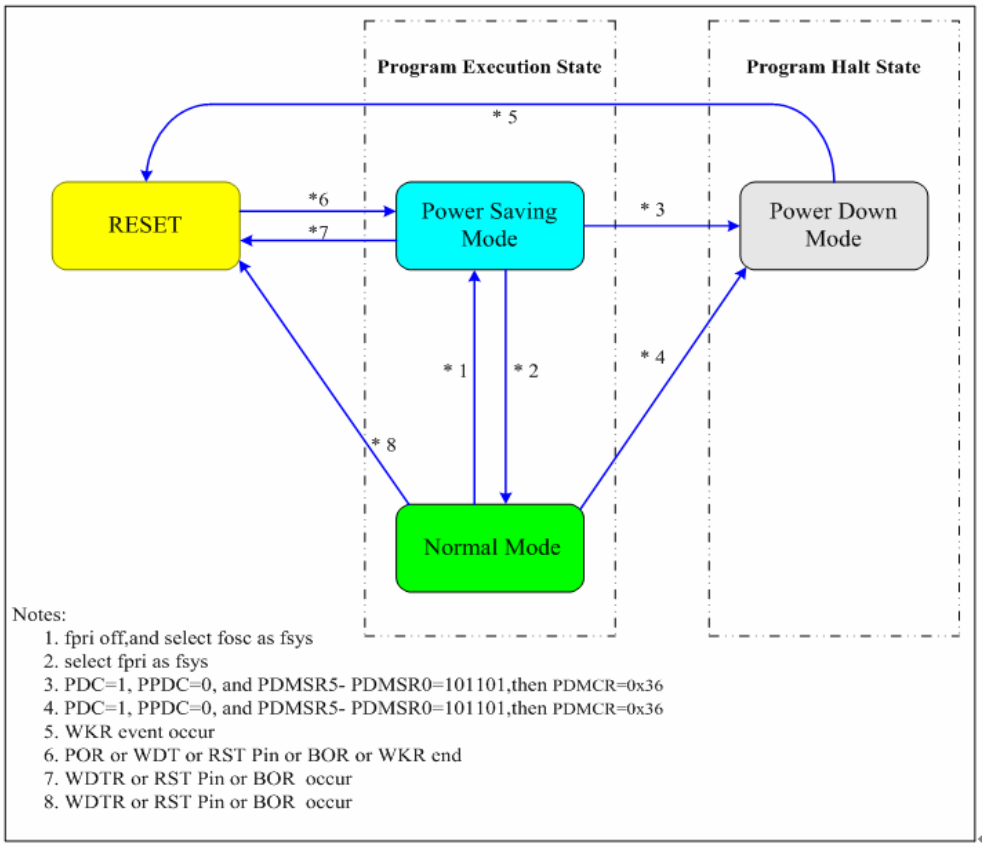


Figure 8-1 Transitioning between operation modes

8.3.1 Normal Mode ->PSM

In AC power supply, the system operate in Normal Mode and the user program needs to

monitor the AC power supply in real time to judge whether it is power down as shown in fig 8-2. If the AC power supply is lower than the setting value, system power supply will automatically switch to external battery supply and shift to PSM mode by software, then enter into PDM mode through configuring in the PSM mode. Or it will go on working in Normal mode.

The switching from Normal mode to PSM mode is completed by the system clock switching from high-frequency clock to low-frequency clock as shown in fig 8-1. The switching is specifically described in chapter 5.2.2.3 Switch from high-frequency system clock to low-frequency system clock

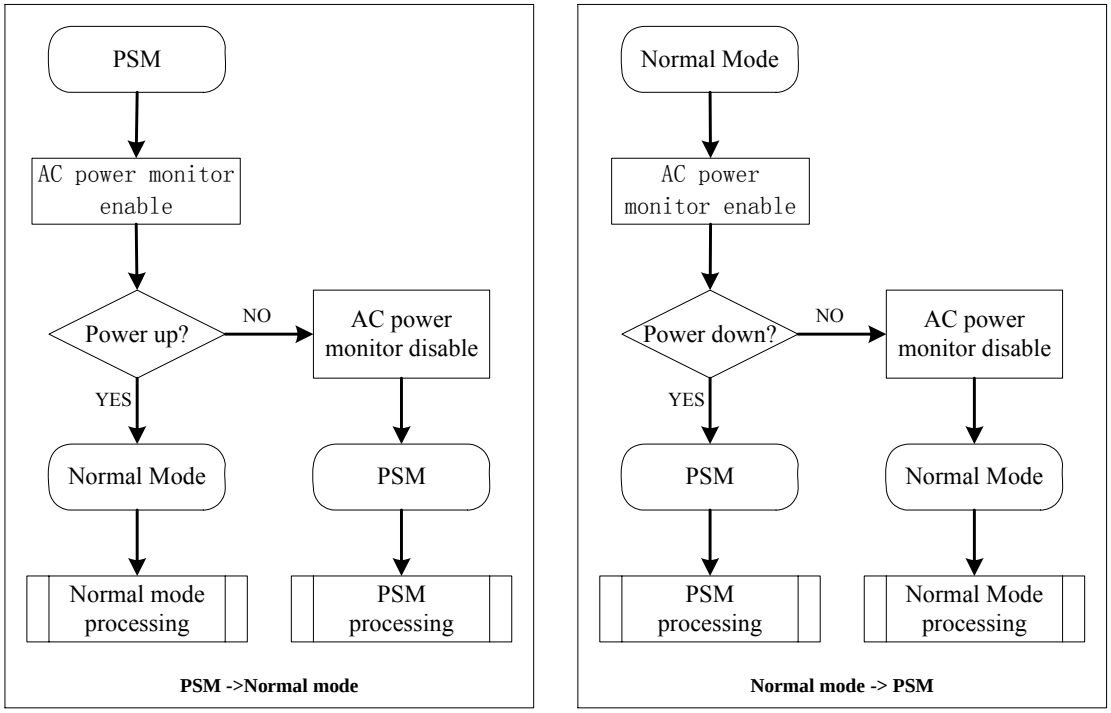


Figure 8-2 PSM<->Normal mode

8.3.2 PSM-> Noraml Mode

In PSM mode, the AC power supply monitor circuit judge whether it is AC power on as shown in fig 8-2. If AC power supply is power on, System will enter into Normal mode. If not ,it will close the AC power supply monitor circuit and go on working in PSM mode ,deal with the relative events and then return to PDM mode.

The switch from PSM to Normal mode is completed by the system clock switch from low-frequency clock to high-frequency clock. The switch is specifically described in 5.2.2.1 switch from low-frequency system clock to high-frequency system clock

8.3.3 PSM or Normal Mode-> PDM

When the AC power supply is down, it needs to store the field date as shown in fig 8-3. When it occurs, the important date of EMU and XRAM is stored, the system will switch from PSM mode to PDM mode by setting PDMSR5-PDMSRO=101101, configuring PDC and PPDC to 1 and 0 respectively and setting PDMCR=0x36.

When date capacity needs to be stored is large, user can store date under high frequency time clock to shorten the time of storing and then switch the Normal mode to PDM mode ,which is similar to the process of switching from PSM mode to PSM mode.

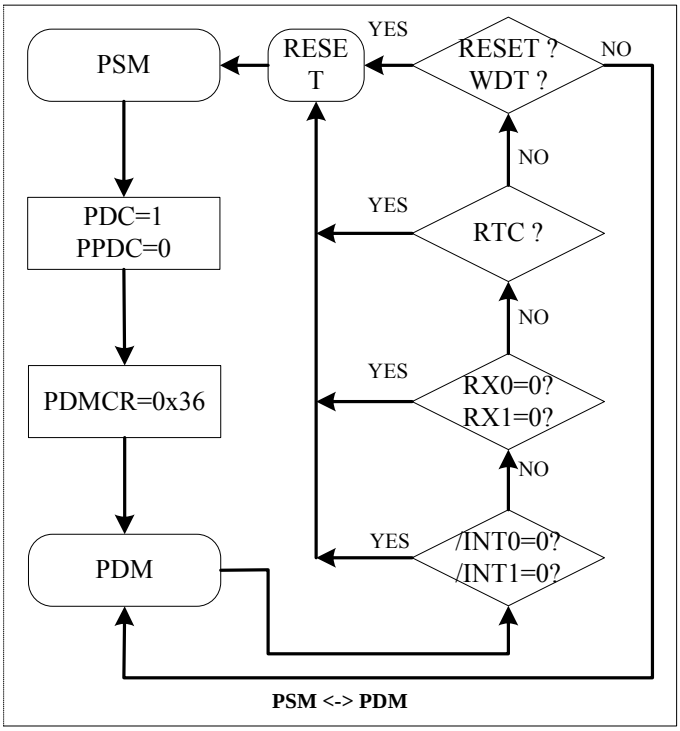


Figure 8-3 PSM<->PDM

8.3.4 PDM -> PSM

PDM can only switch to PSM and it is executed by wake-up reset. There are many wake-up sources include: /INT0 PIN、/INT1 PIN、RX0 PIN、RX1 PIN、RST PIN、WDT overflow reset、RTC interrupt that can generate PDM wake-up reset.

Chip will quit PDM mode when waked up from PDM. After the quit, chip resets firstly and set WKR flag bit of RSTSR register. Similar to Power On Reset, CPU52 runs from 0000H, all register return to reset state except the reset status register.

Users should pay attention to the following rules when waking up PDM mode:

1. RX0 PIN、RX1 PIN must be configured as the input of /int0 or /int1 of CPU52 to ensure wake-up reset function(**15.2.8 Configure RX0/RX1 as The input of /INT0 and /INT1**).For /INT0 PIN、/INT1 PIN、RX0 PIN、RX1 PIN share the /int0 and /int1 resource of CPU52, only two of the four wake-up modes can be applied at the same time. The selection of the four wake-up modes is determined by RXCON register (**table 15-13**).
2. /INT0、/INT1、RX0 are all pulled high in PDM mode and RX1 PIN needs external pull-up resistance to be high. If the wake-up pin voltage determined by RXCON appears low pulse at least 100ns, chip will quit PDM mode. Pay attention that when chip is waked up by /INT0 PIN、/INT1 PIN、RX0 PIN、RX1 PIN, CPU52 will not execute the relative service program of the relative interrupts. Then system is reset, CPU52 executes from reset address 0000H.
3. When using WDT reset to wake up PDM, pay attention that it should set PDM_RC=1 before entering PDM to enable RC oscillator keep normal working in PDM and then WDT can work normally and overflow wake-up reset can be generated in PDM.

4 RTC interrupts includes: alarm clock interrupt, second timer interrtupt, timer2 interrupt, timer1 interrupt, day interrupt, hour interrupt, minute interrupt,second interrupt etc. 8 interrupt sources. When using RTC interrupt wake-up, notice that before entering PDM, mask off needless RTC interrupt sources by configuring RTCIE register (**fig 12-5**).

8.4 Registers

Table 8-1 function mode register list

Address	Name	Reset value	Function
0xBF	SUPDC	0x67	Power and clock management register- see **table 8-2, write-protect**
0xC7	PDMSR	0x00	PDM state register - see **table 8-3**
0xCF	PDMCR	0x00	PDM control register - see **table 8-4**
0xB7 RSTSR.3	WKR	0	Awaken reset flag bit-see **table 8-5**
0xBD	CLKCFG	0x00	Clock configure register - see **table 5-3, write-protect**
0xBC BORCFG.7	PRION	0	PRION control bit - see **table 5-5, write-protect**
0xB6 SYSSCR.7	LOCK	0	LOCK state bit—see **table 5-6**
0xBC BORCFG. 5	BORPDM	0	BORPDM control bit - see **table 7-3, write-protect**
0xBC BORCFG. 1	PDM_RC	0	PDM_RC control bit - see **table 5-7, write-protect**

1. Power and clock management register（write-protect）

Table 8-2 Power and clock management register (0xBFH,SUPDC)

System Unit Power-Down Control Register (SUPDC)			Address: BFH					
	Bit7	6	5	4	3	2	1	Bit0
Read:	0	PDTPS	PDEMU	PDBOR	PDLVD	PDLCD	PDI2C	PDSPI
Write:	X							
Reset:	0	0	1	0	0	1	1	1

Bit	Function
SUPDC.7	Reseved. Read as 0
SUPDC.6	PDTPS:PDTPS =0 indicates turning on the clock and power supply of the temperature sensor mode;PDTPS =1 indicates turning off the clock and power supply of the temperature sensor mode. After reset ,,PDTPS=0,TPS is turned on.
SUPDC.5	PDEMU:PDEMU =0 indicates turning on the clock of the EMU measure unit and the clock and power supply of 3-route ADC;PDEMU =1 indicates turning off the clock of the EMU measure unit and the clock and power supply of 3-route ADC;after reset,PDEMU=1,EMU is turned off.
SUPDC.4	PDBOR:PDBOR =0 indicates turning on the power supply of the BOR unit;PDBOR =1 indicates turning off the power supply of the BOR unit;after reset,PDBOR=0,BOR is turned on.
SUPDC.3	PDLVD:PDLVD =0 indicates turning on the power supply of the LVD unit;PDLVD =1 indicates turning off the power supply of the LVD unit;after reset,PDLVD=0,LVD is turned on.
SUPDC.2	PDLCD:PDLCD =0 indicates turning on the clock and power supply of the LCD unit;PDLCD =1 indicates turning off the clock and power supply of the LCD unit;after reset,PDLCD=1,LCD is turned off.
SUPDC.1	PDI2C:PDI2C =0 indicates turning on the clock of the I2C unit ;PDI2C =1 indicates turning off the clock of the I2C unit;after reset,PDI2C=1, I2C is turn ed off.
SUPDC.0	PDSPI:PDSPI =0 indicates turning on the clock of the SPI unit;PDSPI =1 indicates turning off the clock of the SPI unit;after reset,PDSPI=1, SPI is turned off.

2. PDM status register

Table 8-3 PDM status register(0xC7H,PDMSR)

Power Down Mode Status Register (PDMSR)			Address: C7H					
	Bit7	6	5	4	3	2	1	Bit0
Read: Write:	PDMSR5	PDMSR4	PDMSR3	PDMSR2	PDMSR1	PDMSR0	PDC	PPDC
Reset:	0	0	0	0	0	0	0	0

Bit	Function
PDMSR [7:2]	PDMSR5- PDMSR0:when PDMSR5- PDMSR0=101101,the PDMSR register is valid data. ***Note :if the PDMSR5- PDMSR0 are not valid data ,writing PDMCR=0x36 can not make the system be in power down mode but it will cause the system reset for being considered as Illegal instruments.***
PDMSR[1:0]	PDC and PPDC:when PDMSR5- PDMSR0=101101,by configuring PDC and PPDC as I and o separately and setting PDMCR=0x36,it can be in PDM mode。 ***Note :when PDMSR5- PDMSR0=101101,if PDC is not 1 and PPDC is not 0,configuring PDMCR=0x36 will bring on the** un anticipative **result.***

3. PDM state register

Table 8-4 PDM state register (0xCFH,PDMCR)

Power Down Mode Control Register (PDMCR)			Address: CFH					
	Bit7	6	5	4	3	2	1	Bit0
Read: Write:	PDMCR7	PDMCR6	PDMCR5	PDMCR4	PDMCR3	PDMCR2	PDMCR1	PDMCR0
Reset:	0	0	0	0	0	0	0	0

Explain :when PDMSR register is valid data.,writing 0x36 into PDMCR register can enter PDM.

4. Awaken reset flag bit

Table 8-5 awaken reset flag (0xB7H,RSTSR.3)

RSTSR			Address: B7H					
	Bit7	6	5	4	3	2	1	Bit0
Read:	POR	RST	WDT	BOR	WKR	0	0	0
Write:	X	X	X	X	x	x	x	X
Reset:	1	0	0	0	0	0	0	0

Explain: PDM awaken reset flag WKR. System can be awaken reset by int0_n、int1_n、RX0、RX1、RTC、WDT、RST PIN when in PDM mode. When awaken reset happens, the reset flag WKR is set. Clean after reading

9 Energy measurement

9.1 Introduction

The ATT7025 provides all functions needed to measure energy in single phase energy meters, including active power and active energy, reactive power and reactive energy, apparent power and apparent energy, voltage rms value, current rms value and frequency computation etc., and it supports flexible way for anti-tampering and calibration.

- Less than 0.1% error on active energy over a dynamic range of 1000 to 1
- Less than 0.5% error on reactive energy over a dynamic range of 1000 to 1
- Active power and active energy; reactive power and reactive energy; apparent power and apparent energy
- Rms value for voltage and current
- Voltage frequency mearsuement
- Synchronous sample data of three ADC; active power, reactive power, apparent power waveform data
- Flexible anti-tamper method, the threshold value can be changed through register.
- Flexible no-load threshold level for anti-creep
- Auto-calibration for DC offset
- Various energy accumulating mode
- Provide fast pulse counter register, preventing energe loss when power down.
- Width of pulse output PF/QF/SF is selectable
- Support single phase three wire system
- Zero-crossing interruption
- Reactive power 90° shift phase compensation

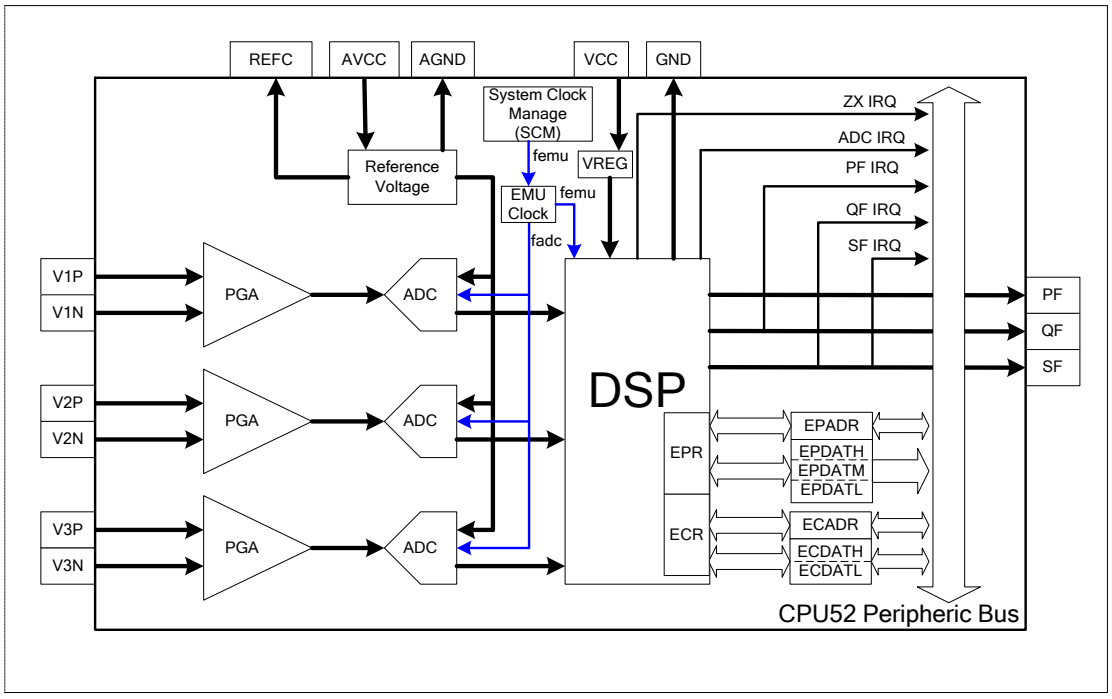


Fig 9-1 Energy Measurement Unit（EMU）

9.2 Function Description

The Energy Measurement Unit (EMU) is composed of three Σ -Δ ADCs, reference circuit, and digital signal precessing unit. The three ADCs complete the sample of two current signals and one voltage signal; The digital signal processing unit completes the measurement function of active power and active energy, reactive power and reactive energy, apparent power and apparent energy, voltage rms value, current rms value and frequency.

The EMU provides high frequency pulse output for calibration, which are pins PF, QF and SF. Calibration parameters and measurement parameters can be accessed through SFR registers; .

The femu is the clock of the EMU and the ADC sample clock (fadc) is femu/6. If femu = 5.5296 MHz, then fadc = 922 KHz.

9.2.1 ADC

The ATT7025 has three sigma-delta ADCs, and each ADC has an anolog PGA (Programmable Gain Amplifier), one 1.25 Vs high stabilization on-chip voltage reference.

PGAs amplify the differential input signals, and the amplified signals are sent to ADC for sampling, which can guarantee measurement linearity at very small input signal. The three ADCs' PGA can be configured independently with register ADCCON(0x58H, table 9-54). The PGA can be set as ×1, ×8, ×16, and ×32.

The signal sampled by the three ADCs can also be amplified as ×1, ×2, ×4, ×8 with register DGAIN(0x5AH, table 9-56) .If the large signals not overflowed, the digital gain amplification can add the effective numbers of the small signal's computation to improve the calculation precision.

The ADC2(the current channel 2) is disabled by default. It can be disabled or enabled independently with bit ADC2ON(0x51H.7, table 9-47).

The ADC2 also has gain calibration registerI2GAIN(0x4AH, table 9-40). It can carry on proportional scaling on ADC2 signal amplitude and can be used in automatic anti-tamper meter.

9.2.2 ADC Sample Output and Power Waveform Output

The ATT7025 opens the three ADC output 16 bit sample data Spl_I1(0x00H, table 9-13), Spl_I2(0x01H, table 9-14), and Spl_U(0x02H，table 9-15) to users, also opens the power waveform data Spl_P(0x03H, table 9-16), Spl_Q(0x04H, table 9-17), and Spl_S(0x05H, table 9-18) used for the energy accumulating to users.

The updated frequency of the sample/waveform data are femu/192, femu/384, femu/768, femu/1536, femu/3072. For example, if femu is choosed as 5.5296 MHz, then the waveform data updated frequency can be choosed as 28.8 kHz, 14.4 kHz, 7.2 kHz, 3.6 kHz, and 1.8 kHz.

Note: Because the waveform data updated frequency can be 28.8 KHz at most, the ADC_IRQ interrupt request can also be 28.8 KHz at most but the CPU working frequency can be 11.0592 MHz at most .The users need to notice whether the CPU procedure has enough time to respond to the interruption.

9.2.3 Active Power, Reactive Power and Apparent Power

The ATT7025 provides active power, reactive power and apparent power output register.

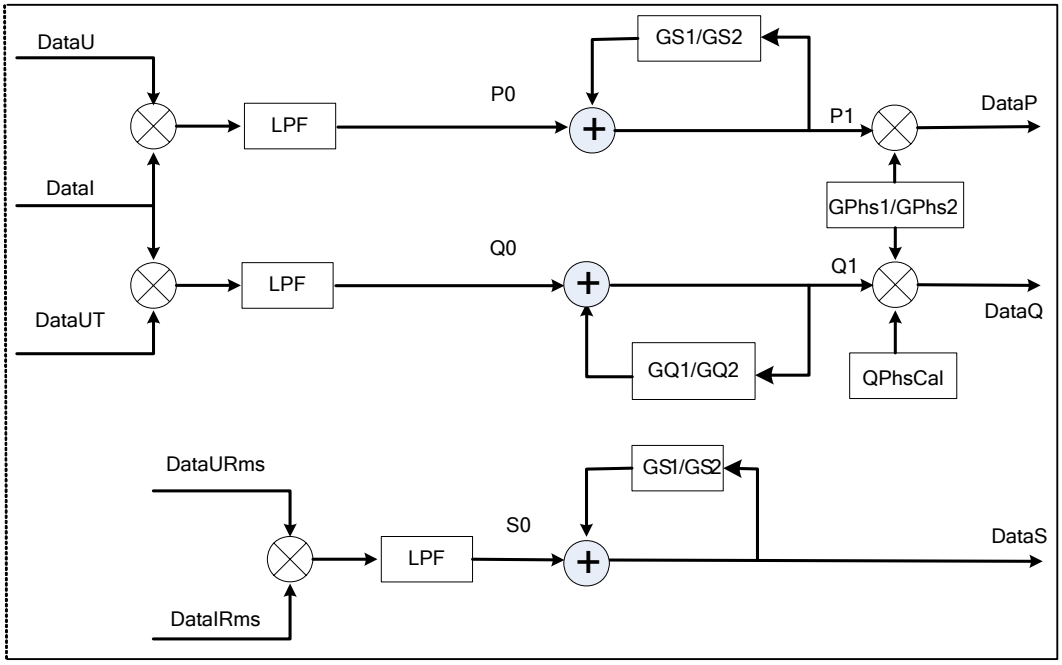


Fig 9-2 Power measurement and compensation

Active power is calculated by low-pass filtering the product of voltage and current.

Reactive power is calculated by low-pass filtering the product of the voltage and current waveforms when the voltage is phase-shifted by 90°.

Apparent power is defined as the product of voltage rms and current rms.

For channel 1 and channel 2 powers, it provides gain calibration and phase calibration.

The performance of 90° phase shifting filter is related with the frequency of input signal and the ADC sample frequency and it can be compensated by reactive power phase shifting register QphsCal(0x49H, table 9-39)). The default value of QphsCal is 0 and the precise 90° phase shifting of input voltage signal at 50Hz can be realized when femu = 5.5296MHz

9.2.4 Rms Value of Voltage and Current

The ATT7025 outputs the rms value of two current channels and one voltage channel in the same time.

The rms value can guarantee less than 0.5% error.

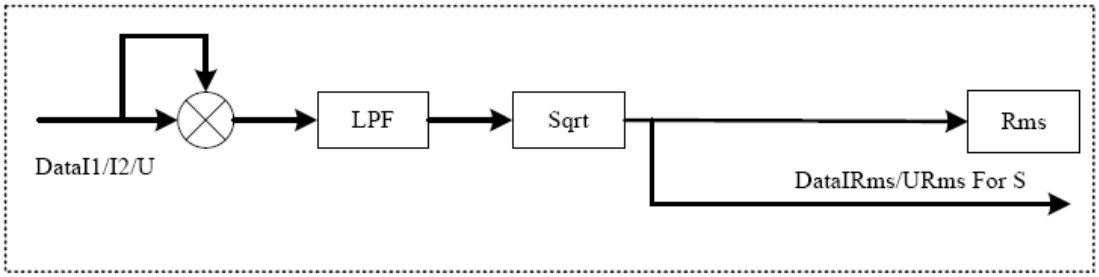


Fig 9-3 rms value caculation

9.2.5 Voltage Frequency Output

It provides voltage frequency output by using the on-chip zero-crossing detection.

The frequency can guarantee 0.01 Hz precision.

9.2.6 Flexible No-load/startup Setup

By configuring register PQStart(0x4EH, table 9-44), users can complete no-load and startup function flexiblely.

When |P|<PQStart, PF will not output pulse.

When |Q|<PQStart, QF will not output pulse.

When (|P| & |Q|)<PQStart, SF will not output pulse.

The NOQLD and NOPLD bits of the status register EMUSR(0x40H, table 9-30) can show whether no-load happens in time, and it is convenient for the user to select the threshold value.

9.2.7 Power Negative Indication

The REVQ and REVP bit of the status register EMUSR(0x40H, table 9-30) can indicate whether the reactive power and active power is negative .

These bits are updated synchronously with the output of PF and QF.

9.2.8 Anti-tamper

It can select the bigger current to measure power through comparing the rms value of the two current channels.

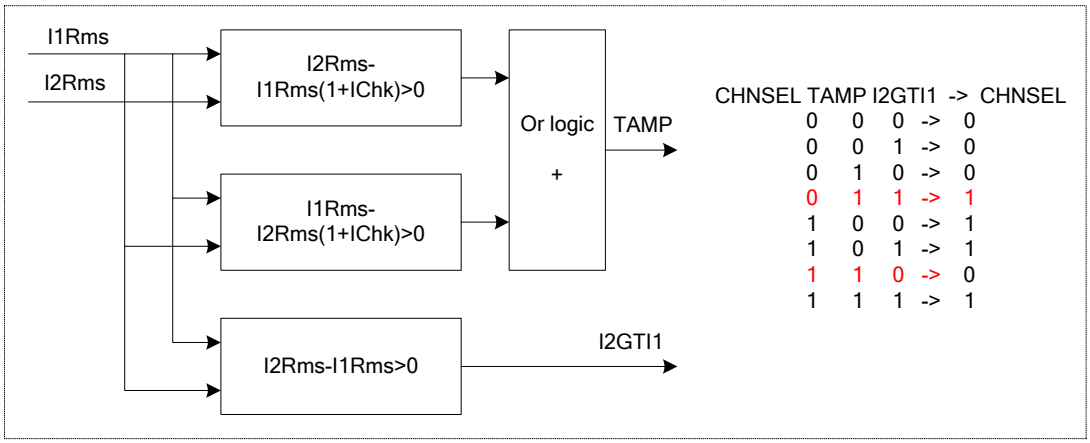


Fig 9-4 Auto anti-tamper scheme

Setting or clearing FLTON(0x52H.5, table 9-48) can enable or disable auto anti-tamper circuit. When FLTON=0, users can select current channel accrording to CHNSEL(0x51H.4, table 9-47). When FLTON=1, auto anti-tamper ciruit is enabled, and EMU selects current channel 1 or channel 2 to measure power automatically according to the users' configuration.

Users can use the vectors summation of two current channel to canculate the power by configuring the register CIADD(0x51H.3, table 9-47).

Through ICHK(0x50H, table 9-50), users can set up the proportion of tampering, e.g, setting up 0x10H, the proportion is 6.25%. When the two channel current difference is equal to or bigger than 6.25%, tampering happens.

When the rms values of the two current channel are both small than the value of ITAMP(0x59H, table 9-55), it will select current channel 1 as default in order to prevent noisy disturbance.

When I2GT1(0x51H.5, table 9-47) is 0, it means I1>I2, otherwise it means I2>I1.

When TAMP(0x51H.6, table 9-47) is 1, it means stealing is happening, namely two current channel rms difference is larger than the threshold value

Automatic anti-tampering setting up steps:

a) Turn on ADC2 through ADC2ON(0x51H.7, table 9-47).

b) Calibrating the output of channel 2 through I2GAIN(0x4AH, table 9-40) to ensure the coherence of the two channel' rms output value when at same input current.

c) Set up ICHK(0x50H, table 9-46) to configure tampering threshold value.

d) Set up ITAMP(0x59H, table 9-55) to configure minimum current for anti-tampering.

e) Set FLTON(0x52H.5, table 9-48), enable auto-tampering.

After automatical anti-tampering is enabled, the CHNSEL and CIADD are read only, and the current channel selection is decided by the results of anti-tampering. Status of anti-tampering can be observed through register bit CHNSEL/TAMP/I2GTI1.

9.2.9 Offset Automatic Calibration and Offset Register

Users can use HPFONU, HPFONI2 and HPFONI1 bits of CHNLCR(0x52H, table 9-48) to decide whether the high-pass filter of the voltage and current channel is on or off respectively. When these bits are 0, it means the high-pass is enabled, otherwise, disabled.

After high-pass filter is disabled, it can carry on offset calibration to sample data through offset registers I1Off(0x4BH, table 9-41), I2Off(0x4CH, table 9-42), and UOff(0x4DH, table 9-43).

Users can complete offset calibration automatically or manually.

When processing offset calibration, the input signal should be 0.

When processing automatic offset calibration, writing 0x01H to AUTODC(0x54H, table 9-50) can quickly complete the automatic offset calibration.After completed, the register is changed to 0x00H. The new offset value is put in calibration register. When processing automatic offset calibration (AUTODC=1), users can't modify offset register. It costs about 0.6s to complete automatic offset calibration when femu is 5.5296 MHz.

When selecting manually calibration offset, users can calculate the offset values with the averaging values of ADC sample data SPL_I1(0x00H, table 9-13), SPL_I2(0x01H, table 9-14), and SPL_U(0x02H, table 9-15).

9.2.10 Energy Register and Pulse Output Unit

The ATT7025 provides active energy register ENERGY_P(0x0DH, table 9-26), reactive energy register ENERGY_Q(0x0EH, table 9-27) , apparent energy register ENERGY_S(0x0FH, table 9-28) and the related pulse output PF,QF and SF in the same time.

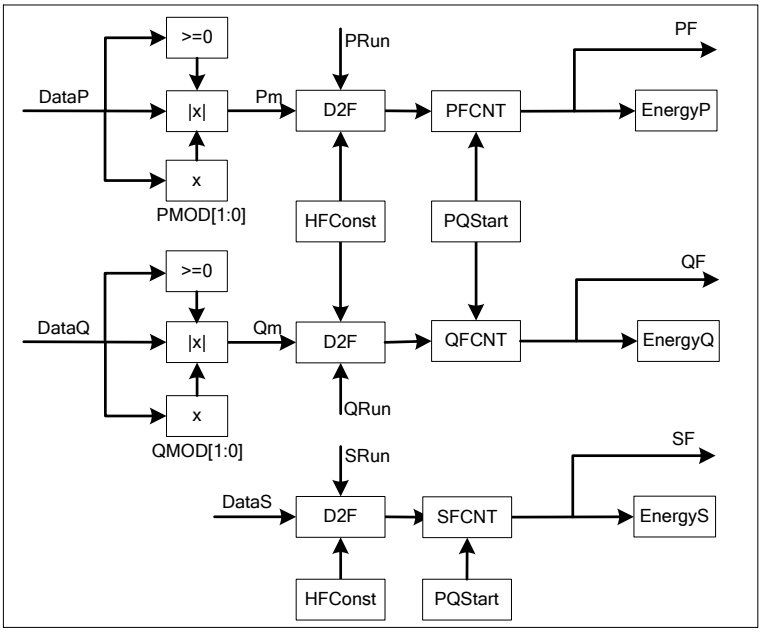


Fig 9-5 Energy measurement and pulse output

The energy can select positive accumulation, absolute accumulation and algebraic accumulation mode through QMOD and PMOD bits in EMCON(0x53H, TABLE 9-49).

The internal power value register accumulates power value and send out an overflow pulse to fast pulse counter register PFCNT(0x55H, TABLE 9-51), QFCNT(0x56H, TABLE 9-52) and SFCNT(0x57H, TABLE 9-53) . Fast pulse counter register accumulates the overflow times. When the absolute counter value in fast pulse counter register is larger than or equal to the configuration of output pulse frequency setup register HFConst(0x4FH, table 9-45), it will send out a CF(PF or QF or SF) pulse and add 1 to the related energy register at the same time.

The ATT7025 opens fast pulse counter register PFCNT/QFCNT/SFCNT to users. Users can prevent lossing energy measurement when power down through reading and writing these registers.

The pulse output pin PF/QF/SF and energy register are controlled by PRun/QRun/SRun and PQStart(0x4EH, table 9-44 in EMCON(0x53H, table 9-49).

When PRun=0 or |P|<PQStart, PF does not output pulse.

When QRun=0 or |Q|<PQStart, QF does not output pulse.

When SRun=0 or |P|&|Q|<PQStart, SF does not output pulse.

Users can select effective logic level of PF/QF/SF by POS（0x52H.6, table 9-48）. When POS is 0, pulse high level is valid.

The PF/QF/SF output satisfies the underneath timing:

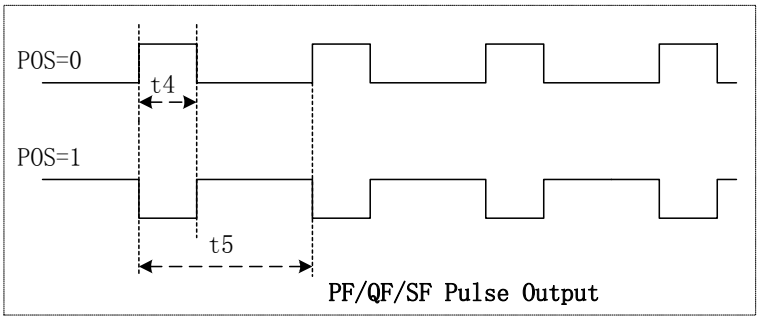


Fig 9-6 pulse output wave

Clock Timing:

Parameter	Index	Unit	Testing condition and notation
t4 t5	90 --	ms S	the output high level pulse of PF/QF/SF the output period of PF/QF/SF

Attention: when the pulse output period is shorter than 180 ms, pulse output is on 50% duty.

ATT7025 can change pulse output width(t4) through setting up CFP[1:0](0x58H.[7:6], table 9-54).

9.2.11 Emu Interrupt System

EMU provides five interruption: PF_IRQ, QF_IRQ, SF_IRQ, ADC_IRQ and ZX_IRQ.

PF_IRQ: when outputting active energe pulse, EMU sends interrupt request to CPU52.

QF_IRQ: when outputting reactive energe pulse, EMU sends interrupt request to CPU52.

SF_IRQ: when outputting apparent energe pulse, EMU sends interruption request to CPU52.

ADC_IRQ: It sends ADC interrupt request to CPU52 periodly based on the selected sample frequency.

ZX_IRQ: when there is zero-crossing in voltage channel, EMU send interrupt request to CPU52. And zero-crossing can select positive crossing or negative crossing by register ZXD(0x53H.7, table 9-49)

ZXD=0: means selecting positive direction crossing signal as interruption dectcting signal.

ZXD=1: means selecting negative direction crossing signal as interruption detecting signal.

The five interruptios of EMU totally use one interruption EMUIF(0xB1H, table 9-10). Users can realize interruption control and management through EMU enable register EMUIE(0xA9H, table 9-9) and EMU interruption flag register EMUIF(0xB1H, table 9-10).

Writing 1 to related bit in EMUIF can clear interrupt flag.

9.3 Registers

EMU includes two kinds of registers. One is SFR register, namely direct register. Users can access directly through SFR address. The other is measurement parameter and calibration register, namely indirect register. Users can only access indirectly through direct register.

9.3.1 SFR registers

Fig 9-1 EMU SFR register list

Address	Name	Byte length	function description
0xD9	ECADR	1	EMU calibration address register
0xDB	ECDATH	1	EMU calibration data register high
0xDA	ECDATL	1	EMU calibration data register low
0xDC	EPADR	1	EMU parameter address register
0xDF	EPDATH	1	EMU parameter data register high
0xDE	EPDATM	1	EMU parameter data register middle
0xDD	EPDATL	1	EMU parameter data register low
0xA9	EMUIE	1	EMU interrupt enable register
0xB1	EMUIF	1	EMU interrupt flag register
0xBF	SUPDC	1	PDEMU control bit

Fig 9-2 EMU Calibration Address Register (ECADR, 0xD9H)

EMU Calibration Address Register (ECADR)			**Address:**	**D9H**				
	Bit7	**6**	**5**	**4**	**3**	**2**	**1**	**Bit0**
Read: / **Write:**	ECADR7	ECADR6	ECADR5	ECADR4	ECADR3	ECADR2	ECADR1	ECADR0
Reset:	0	0	0	0	0	0	0	0

Fig 9-3 EMU Calibration Data High Byte Register (ECDATH, 0xDBH)

EMU Calibration Data High Byte Register (ECDATH)			**Address:**	**DBH**				
	Bit7	**6**	**5**	**4**	**3**	**2**	**1**	**Bit0**
Read: / **Write:**	ECDATH7	ECDATH6	ECDATH5	ECDATH4	ECDATH3	ECDATH2	ECDATH1	ECDATH0
Reset:	0	0	0	0	0	0	0	0

Fig 9-4 EMU Calibration Data Low Byte Register (ECDATAL, 0xDAH)

EMU Calibration Data Low Byte Register (ECDATL)			**Address:**	**DAH**				
	Bit7	**6**	**5**	**4**	**3**	**2**	**1**	**Bit0**
Read: / **Write:**	ECDATL7	ECDATL6	ECDATL5	ECDATL4	ECDATL3	ECDATL2	ECDATL1	ECDATL0
Reset:	0	0	0	0	0	0	0	0

Fig 9-5 EMU Parameter Address Register (EPADR, 0xDCH)

EMU Parameter Address Register (EPADR)			Address: DCH					
	Bit7	6	5	4	3	2	1	Bit0
Read:	EPADR7	EPADR6	EPADR5	EPADR4	EPADR3	EPADR2	EPADR1	EPADR0
Write:								
Reset:	0	0	0	0	0	0	0	0

Fig 9-6 EMU Parameter Data High Byte Register (EPDATH, 0xDFH)

EMU Parameter Data High Byte Register (EPDATH)			Address: DFH					
	Bit7	6	5	4	3	2	1	Bit0
Read:	EPDATH7	EPDATH6	EPDATH5	EPDATH4	EPDATH3	EPDATH2	EPDATH1	EPDATH0
Write:	X	X	X	x	X	X	X	X
Reset:	0	0	0	0	0	0	0	0

Fig 9-7 EMU Parameter Data Middle Byte Register (EPDATM, 0xDEH)

EMU Parameter Data Middle Byte Register (EPDATM)			Address: DEH					
	Bit7	6	5	4	3	2	1	Bit0
Read:	EPDATM7	EPDATM6	EPDATM5	EPDATM4	EPDATM3	EPDATM2	EPDATM1	EPDATM0
Write:	X	X	X	x	X	X	X	X
Reset:	0	0	0	0	0	0	0	0

Fig 9-8 EMU Parameter Data Low Byte Register (EPDATL, 0xDDH)

EMU Parameter Data Low Byte Register (EPDATL)			Address: DDH					
	Bit7	6	5	4	3	2	1	Bit0
Read:	EPDATL7	EPDATL6	EPDATL5	EPDATL4	EPDATL3	EPDATL2	EPDATL1	EPDATL0
Write:	X	X	X	x	X	X	X	X
Reset:	0	0	0	0	0	0	0	0

Fig 9-9 EMU Interrupt Enable Register (EMUIE, 0xA9H)

EMU Interrupt Enable Register (EMUIE)			Address: A9H					
	Bit7	6	5	4	3	2	1	Bit0
Read:	PFIE	QFIE	SFIE	SPLIE	ZXIE	0	0	0
Write:						x	x	x
Reset:	0	0	0	0	0	0	0	0

Only when the related interrupt bit enabled, the interruption flag of 0xB1H can be set.

Fig 9-10 EMU Interrupt Flag Register (EMUIF, 0xB1H)

EMU Interrupt Flag Register (EMUIF)			Address: B1H					
	Bit7	6	5	4	3	2	1	Bit0
Read:	PFIF	QFIF	SFIF	SPLIF	ZXIF	0	0	0
Write:						x	x	x
Reset:	0	0	0	0	0	0	0	0

Setting the related interruption bit can clear the interrupt flag

Eg: If PFIF is set, PFIF is cleared.

Fig 9-11 System Unit Power-Down Control Register (SUPDC, 0xBFH)

System Unit Power-Down Control Register (SUPDC)			Address: BFH					
	Bit7	6	5	4	3	2	1	Bit0
Read:	0	PDTPS	PDEMU	PDBOR	PDLVD	PDLCD	PDI2C	PDSPI
Write:	x							
Reset:	0	0	1	0	0	1	1	1

When write-protect is disabled, PDEMU=0 indicates EMU enabled; PDEMU=1 indicates EMU disabled. From the off status to on status, EMU reset starts.

9.3.2 Indirect registers

It includes the measurement parameter registers and the calibration register.They are all

indirect register, as follows:

1. Emu Parameter Register

These registers can only be read through EPADR and EPDATH/EPDATM/EPDATL registers indirectly.

a、 If EPR register is a 3- byte register, the EPDATH/EPDATM/EPDATL are stored in high, mid, low data bytes respectly.

b、 If EPR register is a 2 -byte register, EPDATM/EPDATL are stored in high and low data bits respectly and EPDATH is an extensive sign bit, e.g. EPDATM.7's extensive bit.

EPR operation regulation:

When writing address register EPADR, the related address measurement data are updated

2. Emu Calibration Register

These registers process indirect write and read operation through ECADR and ECDATH / ECDATL register.

a、 When ECR is a 2 byte data, ECDATH and ECDATL are ECR's high and low byte respectly.

b、 If ECR is a single byte data, the ECDATL is ECR data and the ECDATH byte is ignored.

ECR operation regulation:

a、 When Reading ECR, write address to ECADR register, the related address ECR data is placed in ECDAT for CPU52's reading;

b、 When writing ECR, write address register ECADR first, then high byte data ECDATH (single byte data can ignore such operation), and then low byte data ECDATL. **Note:** For the 16bit writing operation, after writing the low byte data ECDATL, the 16bit data will be written to internal indirect register.

3. ECR register write-protect:

Only when EPADR=10100110(0xA6H), and when writing the ECDATL, can write the ECDAT parameter to the ECR register, otherwise writing is invalid.

After write-protect is turned off, as long as the EPADR register's value is not changed, the write-protect is always turned off.

9.3.2.1 Measurement Parameter Registers List

Table 9-12 EPR register list (Read only)

Adress(EPADR)	Name	Bit length	Function description
00H	Spl_I1	2	ADC sample data of current channel 1
01H	Spl_I2	2	ADC sample data of current channel 2
02H	Spl_U	2	ADC sample data of voltage channel
03H	Spl_P	3	Active Power waveform data
04H	Spl_Q	3	Reactive power waveform data
05H	Spl_S	3	Aparrent power waveform data
06H	Rms_I1	3	rms value of current channel 1
07H	Rms_I2	3	rms value of current channel 12
08H	Rms_U	3	rms value of voltage channel
09H	Freq_U	2	Voltage frequency

0AH	Power_P	3	Activer power
0BH	Power_Q	3	Reactive power
0CH	Power_S	3	Aparrent power
0DH	Energy_P	3	Active energy
0EH	Energy_Q	3	Reactive energy
0FH	Energy_S	3	Aparrent energy
10H	Reserved	0	Reserved
11H	Reserved	0	Reserved
12H	Reserved	0	Reserved
13H	Reserved	0	Reserved
14H	Reserved	0	Reserved
15H	Reserved	0	Reserved
16H	Reserved	0	Reserved
17H	Reserved	0	Reserved
18H	Reserved	0	Reserved
19H	Reserved	0	Reserved
1AH	Reserved	0	Reserved
1BH	Reserved	0	Reserved
1CH	Reserved	0	Reserved
1DH	Reserved	0	Reserved
1EH	Reserved	0	Reserved
1FH	Reserved	0	Reserved

Sample waveform output

Fig 9-13 Current Waveform Register (Spl_I1 0x00H)

Current 1 Waveform Register (Spl_I1)			**Address:**	**00H**			
	Bit15	**14**	**13**	**12 … 3**	**2**	**1**	**Bit0**
Read:	SI1_15	SI1_14	SI1_13	SI1_12…SI1_3	SI1_2	SI1_1	SI1_0
Write:	X	X	X	X	X	X	X
Reset:	0	0	0	0	0	0	0

Fig 9-14 Current Waveform Register (Spl_I2 0x01H)

Current 2 Waveform Register (Spl_I2)			**Address:**	**01H**			
	Bit15	**14**	**13**	**12 … 3**	**2**	**1**	**Bit0**
Read:	SI2_15	SI2_14	SI2_13	SI2_12…SI2_3	SI2_2	SI2_1	SI2_0
Write:	X	X	X	X	X	X	X
Reset:	0	0	0	0	0	0	0

Fig 9-15 Voltage Waveform Register (Spl_U 0x02H)

Votage Waveform Register (Spl_U)			**Address:**	**02H**			
	Bit15	**14**	**13**	**12 … 3**	**2**	**1**	**Bit0**
Read:	SU_15	SU_14	SU_13	SU_12…SU_3	SU_2	SU_1	SU_0
Write:	X	X	X	X	X	X	X
Reset:	0	0	0	0	0	0	0

Current, voltage sample value is of twos complement, and it is 16 bit practical ADC sample data output. Its updated frequency is determined by SPL (See ECR register 0x51H), and 28KHz at most.

Fig 9-16 Active Power Waveform Register (Spl_P 0x03H)

Active Power Waveform Register (Spl_P)			**Address:**	**03H**			
	Bit23	**22**	**21**	**20 … 3**	**2**	**1**	**Bit0**
Read:	SP_23	SP_22	SP_21	SP_20…SP_3	SP_2	SP_1	SP_0
Write:	X	X	X	X	X	X	X
Reset:	0	0	0	0	0	0	0

Fig 9-17 Reactive Power Waveform Register (Spl_Q 0x04H)

Reactive Power Waveform Register (Spl_Q)			Address: 04H				
	Bit23	22	21	20 … 3	2	1	Bit0
Read:	SQ_23	SQ_22	SQ_21	SQ_20…SQ_3	SQ_2	SQ_1	SQ_0
Write:	X	X	X	X	X	X	X
Reset:	0	0	0	0	0	0	0

Fig 9-18 Apparent Power Waveform Register (Spl_S 0x05H)

Apparent Power Waveform Register (Spl_S)			Address: 05H				
	Bit23	22	21	20 … 3	2	1	Bit0
Read:	SS_23	SS_22	SS_21	SS_20…SS_3	SS_2	SS_1	SS_0
Write:	X	X	X	X	X	X	X
Reset:	0	0	0	0	0	0	0

Power waveform sample value is twos complement, 24 bit data. The updated frequency is determined by SPL (See ECR register 0x51H), and 28KHz at most.

rms value output:

Fig 9-19 Current 1 Rms Register (I1Rms 0x06H)

Current 1 Rms Register (I1Rms)			Address: 06H				
	Bit23	22	21	20 … 3	2	1	Bit0
Read:	I1S23	I1S22	I1S21	I1S20…I1S3	I1S2	I1S1	I1S0
Write:	X	X	X	X	X	X	X
Reset:	0	0	0	0	0	0	0

Fig 9-20 Current 2 Rms Register (I2Rms 0x07H)

Current 2 Rms Register (I2Rms)			Address: 07H				
	Bit23	22	21	20 … 3	2	1	Bit0
Read:	I2S23	I2S22	I2S21	I2S20…I2S3	I2S2	I2S1	I2S0
Write:	X	X	X	X	X	X	X
Reset:	0	0	0	0	0	0	0

Table9-21 Voltage Rms Register (URms 0x08H)

Voltage Rms Register (Urms)			Address: 08H				
	Bit23	22	21	20 … 3	2	1	Bit0
Read:	US23	US22	US21	US20…US3	US2	US1	US0
Write:	X	X	X	X	X	X	X
Reset:	0	0	0	0	0	0	0

Rms is 24 bit unsigned data.

If the register value is RMSreg, the real effective value is RMS, and conversion coefficient is Krms, then

RMS＝RMSreg×Krms

Thereinto, Krms is calculated when the basic input.

Attention: the coefficient of rms value of voltage and two current channels is respective.

Example:

If the input basic current of current channel 1 is 5A, average value of RMSreg is 0x039580 (234880), then

Kp＝5/234880＝2.1287466×10^(-5)

If RMSreg reads 0x10000(65536), then the rms value I1rms is

I1rms＝65536×Kp＝1.3951A

Rms value updated at a speed of femu/1572864. E.g., if femu=5.5296MHz, then the speed of rms value updated is 3.5Hz, i.e. 3.5 times/s.

Voltage frequency measurement:

Fig 9-22 Voltage Frequency Register (UFREQ 0x09H)

Voltage Frequency Register (UFREQ)			Address: 09H				
	Bit15	14	13	12 … 3	2	1	Bit0
Read:	Ufreq15	Ufreq14	Ufreq13	Ufreq12…Ufreq3	Ufreq2	Ufreq1	Ufreq0
Write:	X	X	X	X	X	X	X
Reset:	1	1	1	1	1	1	1

Frequency is 16 bit unsigned data:

f=femu/6/UFREQ

E.g., if femu=5529600Hz, UFREQ=18350, then, the measured real frequency is:

f=5529600/6/18350=50.2Hz。

The updated period of voltage frequency is about 0.7 second.

Power parameter output:

Fig 9-23 Active Power Register (PowerP 0x0AH)

Active Power Register (PowerP)			Address: 0AH				
	Bit23	22	21	20 … 3	2	1	Bit0
Read:	AP23	AP22	AP21	AP20…AP3	AP2	AP1	AP0
Write:	X	X	X	X	X	X	X
Reset:	0	0	0	0	0	0	0

Fig 9-24 Reactive Power Register (PowerQ 0x0BH)

Reactive Power Register (PowerQ)			Address: 0BH				
	Bit23	22	21	20 … 3	2	1	Bit0
Read:	RP23	RP22	RP21	RP20…RP3	RP2	RP1	RP0
Write:	X	X	X	X	X	X	X
Reset:	0	0	0	0	0	0	0

Fig 9-25 Apparent Power Register (PowerS 0x0CH)

Apparent Power Register (PowerS)			Address: 0CH				
	Bit23	22	21	20 … 3	2	1	Bit0
Read:	SP23	SP22	SP21	SP20…SP3	SP2	SP1	SP0
Write:	X	X	X	X	X	X	X
Reset:	0	0	0	0	0	0	0

Power parameter PowerP, PowerQ and PowerS are twos complement, 24 bit data, thereinto, the msb is sign bit.

Assume the data in register is PowerP, then the Preg for calculation is

Preg＝PowerP　　if PowerP<2^23

Preg=PowerP-2^24　　if PowerP>=2^23

Assume the displayed active power is P, and conversion coefficiency is Kpqs

then P＝Preg×Kpqs

Kpqs is calculated when basic input.

The coefficiency of reactive power and apparent power is equal to active power coefficiency Kpqs.

Example: When inputing 1000w active power, the average value of PowerP is 0x00C9D9(51673), then

Kpqs＝1000/51673=0.01935

When the value is 0xFF4534, the representative power value is:

P=Kpqs*Preg=0.01935*(-47820)＝ -925.3 w

(Preg＝PowerP－2^24=-47820)

Power parameter is updated at frequency femu/1572864; e.g. if femu=5.5296MHz, then power updated frequency is 3.5Hz, namely 3.5 times per second.

Energy parameter output:

Fig 9-26 Active Energy Register (EnergyP 0x0DH)

Active Energy Register (EnergyP)			Address: 0DH				
	Bit23	22	21	20 … 3	2	1	Bit0
Read:	EP23	EP22	EP21	EP20…EP3	EP2	EP1	EP0
Write:	X	X	X	X	X	X	X
Reset:	0	0	0	0	0	0	0

Fig 9-27 Reactive Energy Register (EnergyQ 0x0EH)

Reactive Energy Register(EnergyQ)			Address: 0EH				
	Bit23	22	21	20 … 3	2	1	Bit0
Read:	EQ23	EQ22	EQ21	EQ20…EQ3	EQ2	EQ1	EQ0
Write:	X	X	X	X	X	X	X
Reset:	0	0	0	0	0	0	0

Fig 9-28 Apparent Energy Register (EnergyS 0x0FH)

Apparent Energy Register(EnergyS)			Address: 0FH				
	Bit23	22	21	20 … 3	2	1	Bit0
Read:	ES23	ES22	ES21	ES20…ES3	ES2	ES1	ES0
Write:	X	X	X	X	X	X	X
Reset:	0	0	0	0	0	0	0

Energy register is unsigned data, the register value of EnergyP/EnergyQ/EnergyS represent the accumulation of PF/QF/SF pulse. The energy minimum unit of the register is 1/EC kWh. Thereinto, EC is meter constant.

Example: meter costant is 3200imp/kWh, when the register's value is 0x001000(4096), then the representive energy is

E＝4096/3200＝1.28 kWh

9.3.2.2 Calibration register list

Fig 9-29 ECR register list: (Read/Write)

Adress(ECADR)	Name	Byte length	Function description
40H	EMUSR	1	EMU status register
41H	GP1	2	Active power gain calibration of channel 1
42H	GQ1	2	Reactive power gain calibration of channel 1
43H	GS1	2	Apparent power gain calibration of channel 1
44H	GPhs1	2	Phase calibration of channel 1
45H	GP2	2	Active power gain calibration of channel 2
46H	GQ2	2	Reactive power gain calibration of channel 2
47H	GS2	2	Apparent power gain calibration of channel 2
48H	GPhs2	2	Phase calibration of channel 2
49H	QPhsCal	1	Reactive phase compensation
4AH	I2Gain	2	Gain calibration of current channel 2
4BH	I1Off	2	offset calibration of current channel 1
4CH	I2Off	2	offset calibration of current channel 2
4DH	UOff	2	offset calibration of voltage channel
4EH	PQStart	2	startup power threadhold
4FH	HFConst	2	Output pulse frequency configure
50H	ICHK	1	check current configure
51H	ADCCFG	1	ADC configure register
52H	CHNLCR	1	current channel control
53H	EMCON	1	Energy measurement control register
54H	AutoDC	1	Automatic offset calibration
55H	PFCnt	2	fast active power counter

56H	QFCnt	2	fast reactive power counter
57H	SFCnt	2	fast apparent pulse counter
58H	ADCCON	1	ADC channel gain
59H	ITAMP	2	current tamper
5AH	DGAIN	1	channel digital gain
5BH	Reserved	0	Reserved
5CH	Reserved	0	Reserved
5DH	Reserved	0	Reserved
5EH	Reserved	0	Reserved
5FH	Reserved	0	Reserved

Fig 9-30 EMU Status Register(EMUSR 0x40H)

EMU Status Register (EMUSR)			Address: 40H					
	Bit7	6	5	4	3	2	1	Bit0
Read:	SEOF	PEOF	QEOF	0	NoQLd	NoPLd	REVQ	REVP
Write:				X	X	X	X	X
Reset:	0	0	0	0	0	0	0	0

REVP: Negative active power indication, when negative active power is detected, then the bit is 1. When positive active power is detected again, then the bit is 0. It is updated when PF sends out a pulse.

REVQ: Negative reactive power indication, when negative reactive power is detected, then the bit is 1. When positive reactive power is detected again, then the bit is 0. It is updated when QF sends out a pulse.

NoPLd: When active power is less than startup power, NoPLd is set to 1; When active power is bigger than/equal to startup power, NoPLd is reset to 0.

NoQLd: When reactive power is less than startup power, NoPLd is set to 1; When reactive power is bigger than/equal to startup power, NoPLd is reset to 0.

QEOF: Reactive energy register overflow flag, write 1 to clear

PEOF: Active energy register overflow flag, write 1 to clear

SEOF: Apparent energy register overflow flag, write 1 to clear

Power correction:

Fig 9-31 Active Power Gain 1 Register (GP1 0x41H)

Active Power Gain 1 Register (GP1)			Address: 41H				
	Bit15	14	13	12 … 3	2	1	Bit0
Read:	GP1_15	GP1_14	GP1_13	GP1_12…GP1_3	GP1_2	GP1_1	GP1_0
Write:							
Reset:	0	0	0	0	0	0	0

Fig 9-32 Reactive Power Gain 1 Register (GQ1 0x42H)

Reactive Power Gain 1 Register (GQ1)			Address: 42H				
	Bit15	14	13	12 … 3	2	1	Bit0
Read:	GQ1_15	GQ1_14	GQ1_13	GQ1_12…GQ1_3	GQ1_2	GQ1_1	GQ1_0
Write:							
Reset:	0	0	0	0	0	0	0

Fig 9-33 Apparent Power Gain 1 Register (GS1 0x43H)

Apparent Power Gain 1 Register (GS1)			Address: 43H				
	Bit15	14	13	12 … 3	2	1	Bit0
Read:	GS1_15	GS1_14	GS1_13	GS1_12…GS1_3	GS1_2	GS1_1	GS1_0
Write:							
Reset:	0	0	0	0	0	0	0

Fig 9-34 Phase Calibration 1 Register (GPhs1 0x44H)

Phase Calibration 1 Register (GPhs1)			Address: 44H				
	Bit15	14	13	12 … 3	2	1	Bit0
Read: Write:	GPS1_15	GPS1_14	GPS1_13	GPS1_12…GPS1_3	GPS1_2	GPS1_1	GPS1_0
Reset:	0	0	0	0	0	0	0

Fig 9-35 Active Power Gain 2 Register (GP2 0x45H)

Active Power Gain 2 Register (GP2)			Address: 45H				
	Bit15	14	13	12 … 3	2	1	Bit0
Read: Write:	GP2_15	GP2_14	GP2_13	GP2_12…GP2_3	GP2_2	GP2_1	GP2_0
Reset:	0	0	0	0	0	0	0

Fig 9-36 Reactive Power Gain 2 Register (GQ2 0x46H)

Reactive Power Gain 2 Register (GQ2)			Address: 46H				
	Bit15	14	13	12 … 3	2	1	Bit0
Read: Write:	GQ2_15	GQ2_14	GQ2_13	GQ2_12…GQ2_3	GQ2_2	GQ2_1	GQ2_0
Reset:	0	0	0	0	0	0	0

Fig 9-37 Apparent Power Gain 2 Register (GS2 0x47H)

Apparent Power Gain 2 Register (GS2)			Address: 47H				
	Bit15	14	13	12 … 3	2	1	Bit0
Read: Write:	GS2_15	GS2_14	GS2_13	GS2_12…GS2_3	GS2_2	GS2_1	GS2_0
Reset:	0	0	0	0	0	0	0

Fig 9-38 Phase Calibration 2 Register (GPhs2 0x48H)

Phase Calibration 2 Register (GPhs2)			Address: 48H				
	Bit15	14	13	12 … 3	2	1	Bit0
Read: Write:	GPS2_15	GPS2_14	GPS2_13	GPS2_12…GPS2_3	GPS2_2	GPS2_1	GPS2_0
Reset:	0	0	0	0	0	0	0

0x41H~0x48H registers are all in binary complement form, the highest bit is sign bit. Specific definitions see Calibration process.

Fig 9-39 Reactive Power Phase Calibration Register (QPhsCal 0x49H)

Reactive Power Phase Calibration Register (QPhsCal)			Address: 49H					
	Bit7	6	5	4	3	2	1	Bit0
Read: Write:	QPC7	QPC6	QPC5	QPC4	QPC3	QPC2	QPC1	QPC0
Reset:	0	0	0	0	0	0	0	0

Reactive phase compensation register also is binary complement form, the highest bit is sign bit.

When femu is 5.5MHz, write 0 to this register. **When femu is 2.7 MHz, write 80H to this register.**

Current Channel 2 gain setup:

Fig 9-40 Current 2 Gain Register (I2Gain 0x4AH)

Current 2 Gain Register (I2Gain)			Address: 4AH				
	Bit15	14	13	12 … 3	2	1	Bit0
Read:	I2G15	I2G14	I2G13	I2G12…I2G3	I2G2	I2G1	I2G0

Write:							
Reset:	0	0	0	0	0	0	0

Channel 2 current gain register is in binary complement form, the highest bit is character bit. Specific definition see Calibration process。

Channel current offset calibration register:

Fig 9-41 Current 1 Offset Register (I1Off 0x4BH)

Current 1 Offset Register (I1Off)			**Address:**	**4BH**			
	Bit15	**14**	**13**	**12 … 3**	**2**	**1**	**Bit0**
Read: / **Write:**	I1OS15	I1OS14	I1OS13	I1OS12…I1OS3	I1OS2	I1OS1	I1OS0
Reset:	0	0	0	0	0	0	0

Fig 9-42 Current 2 Offset Register (I2Off 0x4CH)

Current 2 Offset Register (I2Off)			**Address:**	**4CH**			
	Bit15	**14**	**13**	**12 … 3**	**2**	**1**	**Bit0**
Read: / **Write:**	I2OS15	I2OS14	I2OS13	I2OS12…I2OS3	I2OS2	I2OS1	I2OS0
Reset:	0	0	0	0	0	0	0

Fig 9-43 Voltage Offset Register (UOff 0x4DH)

Voltage Offset Register (UOff)			**Address:**	**4DH**			
	Bit15	**14**	**13**	**12… 3**	**2**	**1**	**Bit0**
Read: / **Write:**	UOS15	UOS14	UOS13	UOS12…UOS3	UOS2	UOS1	UOS0
Reset:	0	0	0	0	0	0	0

0x4BH~0x4DH register is binary complement form, the highest bit is sign bit.

The minimum unit is identical with the minimum unit of the ADC output 16 bit data. Offset calibration is only actived when high-pass filter is disenabled.

No-load and startup:

Fig 9-44 Start Power Threshold Setup Register (PQStart 0x4EH)

Start Power Threshold Setup Register (PQStart)			**Address:**	**4EH**				
	Bit15	**14**	**13**	**12 … 7**	**6**	**5…2**	**1**	**Bit0**
Read: / **Write:**	PQS15	PQS 14	PQS 13	PQS 12…PQS 7	PQS 6	PQS 5…PQS 2	PQS 1	PQS 0
Reset:	0	0	0	0	1	0	0	0

PQStart is 16 bits unsigned character.The low 16 bit of the absolute value of P/Q (PowerP 0x0AH / PowerQ 0x0BH) compare with PQStart[15:0]:

|P|<PQStart, PF does not output pulse.

|Q|<PQStart, QF does not output pulse.

|P|&|Q|<PQStart, SF does not output pulse。

Pulse Frequency:

Fig 9-45 High Frequency Impulse Const Register (HFConst 0x4FH)

High Frequency Impulse Const Register (HFConst)			**Address:**	**4FH**				
	Bit15	**14**	**13**	**12 … 8**	**7**	**6…2**	**1**	**Bit0**
Read:	0	HFC14	HFC13	HFC12…HFC8	HFC7	HFC6…HFC2	HFC1	HFC0
Write:	X							
Reset:	0	0	0	0	1	0	0	0

HFConst is 16-bit unsigned character (the msb is invalid), and compare with the absolute value of fast pulse counter register 0x55H~0x57H. If it is lager than or equal to HFConst, then related PF/QF/SF output a pulse.

The default value of HFConst is 0x0080。

Anti-tampering threshold value setup:

Fig 9-46 Check Current Rms Register (IChk 0x50H)

Check Current Rms Register (IChk)			Address: 50H					
	Bit7	6	5	4	3	2	1	Bit0
Read: / Write:	ICHK7	ICHK6	ICHK5	ICHK4	ICHK3	ICHK2	ICHK1	ICHK0
Reset:	0	0	0	1	0	0	0	0

Anti-tampering threshold current register is in binary form, the range is [0, +1).

ICHK=ICK7*2^{-1}+ ICK6*2^{-2}+ ICK5*2^{-3}+ …+ ICK2*2^{-6}+ ICK1*2^{-7}+ ICK0*2^{-8}

Default value: 0.0625, namely 6.25%.

After starting automatic anti-tampering scheme, when the relative difference between current 1 and 2 larger than IChk, then larger current channel will be selected automatically to measure power and energe, and set TAMP to 1 at the meantime. If current 2 is larger than current 1, then set I2GTI1 to 1.

ADC sample:

Fig 9-47 ADC Config Register (ADCCFG 0x51H)

ADC Config Register (ADCCFG)			Address: 51H					
	Bit7	6	5	4	3	2	1	Bit0
Read:	ADC2ON*	TAMP	I2GTI1	CHNSEL*	CIADD*	SPL2	SPL1	SPL0
Write:		X	X					
Reset:	0	0	0	0	0	0	0	0
Reset:	0	0	0	0	0	0	0	0

ADC2ON: ADC2ON is set means the current channel 2 ADC is enabled; ADC2ON is clear means the current channel 2 ADC is disabled, ADC constantly output 0. When FLTON=1, namely auto anti-tampering enabled, ADC2ON is read only; Only when FLTON=0, ADC2ON can be read and writed.

TAMP: =1 means tampering happened, I1Rms>I2Rms*(1+IChk) or I2Rms>I1Rms*(1+IChk).

=0 means tampering did not happen, the relative difference between I1Rms and I2Rms is less than the IChk range.

I2GTI1: =1 means I2Rms>I1Rms； =0 means I2Rms≤I1Rms.

Attention: TAMP and I2GTI1 bit is valid only when FLTON=1, or it keeps reset value.

CIADD: =1 means two current channels in summation mode, used with CHNSEL. Under current summation model, it uses the calibration register of channel 1. When FLTON=1, namely start auto anti-tampering scheme, CIADD reads only; Only if FLTON=0 CIADD can be read and writed.

CHNSEL: =0 current channel 1 for power measure.

=1 current channel 2 for power measure.

When FLTON=1, start auto anti-tampering scheme, CHNSEL's status is determined by anti-tampering result, and CHNSEL is read only.

When FLTON=0, CHNSEL and CIADD can write and read.

FLTON	CIADD	CHNSEL	Work mode

1	R(constantly 0)	(internal decide)	Auto anti-tampering
0	0	0	current channel 1 for measurement
0	0	1	current channel 2 for measurement
0	1	X	current summation model

SPL[2:0]: waveform update frequency selection, when femu=5.5296MHz, selected frequency is as follows:

SPL2	SPL1	SPL0	Waveform update frequency
0	0	0	1.8k Hz (femu/3072)
0	0	1	3.6k Hz (femu/1536)
0	1	0	7.2k Hz (femu/768)
0	1	1	14.4k Hz (femu/384)
1	x	x	28.8k Hz (femu/192)

When femu=2.7648MHz/1.3824MHz/0.6912MHz, selected waveform updated frequency is proportional to the value in the table above.

Channel configuration:

Fig 9-48 Current Channel Control Register (CHNLCR 0x52H)

Current Channel Control Register (CHNLCR)			**Address:** **52H**					
	Bit7	**6**	**5**	**4**	**3**	**2**	**1**	**Bit0**
Read:	0	POS	FLTON	X	X	HPFONU	HPFONI2	HPFONI1
Write:	X							
Reset:	0	0	0	0	0	0	0	0

POS:

POS=0: means PF/QF/SF is high level valid;

POS=1: means PF/QF/SF is low level valid

FLTON:

FLTON=0: disable auto anti-tampering scheme.

FLTON=1: enable auto anti-tampering scheme

HPFONI2/I1/U:

HPFON=0: enable digital high-pass filter

HPFON=1: disable digital high-pass filter

Energy measurement:

Fig 9-49 Energy Measure Control Register (EMCON 0x53H)

Energy Measure Control Register (EMCON)			**Address:** **53H**					
	Bit7	**6**	**5**	**4**	**3**	**2**	**1**	**Bit0**
Read:	ZXD	SRun	QRun	Prun	QMOD1	QMOD0	PMOD1	PMOD0
Write:								
Reset:	0	1	1	1	0	0	0	0

ZXD:

ZXD=0: means select upward zero-crossing as zero-crossing interruption detecting signal

ZXD=1: means select downward zero-crossing as zero-crossing interruption detecting signal

PMOD[1:0]: active energy accumulation mode selection

PMOD1	PMOD0	Accumulation power Pm
0	0	Pm=DataP
0	1	DataP≧0,Pm=DataP; DataP<0,Pm=0
1	0	Pm=|DataP|
1	1	Pm=DataP

QMOD[1:0]:reactive energy accumulation mode selection

QMOD1	QMOD0	Accumulation power Qm
0	0	Qm=DataQ
0	1	DataQ≧0,Qm=DataQ; DataQ<0,Qm=0
1	0	Qm=|DataQ|
1	1	Qm=DataQ

PRun: Active Energy accumulation enable

PRun=0: disable measurement; PRun=1: enable measurement

QRun: Reactive Energy accumulation enable

QRun=0: disable measurement; QRun=1: enable measurement

SRun: Apparent Energy accumulation enable

SRun=0: disable measurement; SRun=1: enable measurement

Offset calibration:

Fig 9-50 Auto Offset Calibration Register (AutoDC 0x54H)

Auto Offset Calibration Register (AutoDC)			Address: 54H					
	Bit7	6	5	4	3	2	1	Bit0
Read:	0	0	0	0	0	0	0	AUTO
Write:	X	X	X	X	X	X	X	
Reset:	0	0	0	0	0	0	0	0

AUTO=1: enable auto offset calibration, after calibration is completed, AUTO is cleared automatically.

Fast pulse counter:

Fig 9-51 Active Energy Counter Register (PFCNT 0x55H)

Active Energy Counter Register (PFCNT)			Address: 55H				
	Bit15	14	13	12 … 3	2	1	Bit0
Read: Write:	PFC15	PFC14	PFC13	PFC12…PFC3	PFC2	PFC1	PFC0
Reset:	0	0	0	0	0	0	0

Fig 9-52 Reactive Energy Counter Register (QFCNT 0x56H)

Reactive Energy Counter Register (QFCNT)			Address: 56H				
	Bit15	14	13	12 … 3	2	1	Bit0
Read: Write:	QFC15	QFC14	QFC13	QFC12…QFC3	QFC2	QFC1	QFC0
Reset:	0	0	0	0	0	0	0

Fig 9-53 Apparent Energy Counter Register (SFCNT 0x57H)

Apparent Energy Counter Register (SFCNT)			Address: 57H				
	Bit15	14	13	12 … 3	2	1	Bit0
Read: Write:	SFC15	SFC14	SFC13	SFC12…SFC3	SFC2	SFC1	SFC0
Reset:	0	0	0	0	0	0	0

In order to prevent lossing energy in power down, MCU reads register PFCnt/QFCnt/SFCnt's values back and save them when power down, then rewrite these values in PFCnt/QFCnt/SFCnt next time when power up.

When the value of fast pulse counter register PFCnt/QFCnt/SFCnt is bigger than/equal to HFconst, the related PF/QF/SF will output a pulse and register's value of energy register 0x0DH~0x0FH adds 1, accordingly.

Channel Gain Selection::

Fig 9-54 ADC Channel Gain Register (ADCCON 0x58H)

ADC Channel Gain Register (ADCCON)			Address: 58H					
	Bit7	6	5	4	3	2	1	Bit0
Read: Write:	CFP1	CFP0	PGA3	PGA2	PGA1	PGA0	UPGA1	UPGA0
Reset:	0	0	0	0	0	0	0	0

Pulse width selection register, namely the t4 parameter of pulse output, see PF/QF/SF timing.

If femu=5.5296MHz, then:

CFP[1:0]	00	01	10	11
t4	90ms	90/2=45ms	90/4=22.5ms	90/8=11.25ms

if femu=2.7648MHz，then:

CFP[1:0]	00	01	10	11
t4	180ms	180/2=90ms	180/4=45ms	180/8=22.5ms

if femu=1.3824MHz，then:

CFP[1:0]	00	01	10	11
t4	360ms	360/2=180ms	360/4=90ms	360/8=45ms

if femu=0.6912MHz，then:

CFP[1:0]	00	01	10	11
t4	720ms	720/2=360ms	720/4=180ms	720/8=90ms

UPGA[1:0]:

UPGA1	UPGA0	Voltage channel gain
0	0	PGA=1
0	1	PGA=8
1	0	PGA=16
1	1	PGA=32

PGA[3:0]:

PGA1	PGA0	Current channel 1	PGA3	PGA2	Current channel 2
0	0	PGA=1	0	0	PGA=1

0	1	PGA=8	0	1	PGA=8
1	0	PGA=16	1	0	PGA=16
1	1	PGA=32	1	1	PGA=32

Attention: the current, voltage channel gain mentioned here is the channel gain of ADC anolog part.

Stealing dectecting current threshold:

Fig 9-55 Tamper Current Register (ITAMP 0x59H)

Tamper Current Register (ITAMP)			Address: 59H				
	Bit15	14	13	12…3	2	1	Bit0
Read: Write:	ITAMP15	ITAMP14	ITAMP13	ITAMP12…ITAMP3	ITAMP2	ITAMP1	ITAMP0
Reset:	0	0	0	0	0	0	0

ITAMP[15:0] compares with the high 16 bits of current rms register. After enable auto anti-tampering scheme, when the rms current value of channel 1 and 2 is both lower than ITAMP, constantly select channel 1 as effective input, bit TAMP, I2GTI1 and CHNSEL all are 0.

Channel digital gain:

Fig 9-56 Channel Digital Gain Register (DGAIN 0x5AH)

Channel Digital Gain Register (DGAIN)			Address: 5AH					
	Bit7	6	5	4	3	2	1	Bit0
Read:	0	0	DGI3	DGI2	DGI1	DGI0	DGU1	DGU0
Write:	X	X						
Reset:	0	0	0	0	0	0	0	0

This register is similar with channel gain selection, but the gain is realized by amplifying the digital signal after ADC, with the multiple of 1/2/4/8.

DGU[1:0]:

DGU 1	DGU 0	Voltage digital gain
0	0	DG=1
0	1	DG=2
1	0	DG=4
1	1	DG=8

DGI[3:0]:

DGI1	DGI0	Current channel 1 digital gain	DGI3	DGI2	Current channel 2 digital gain
0	0	DG=1	0	0	DG=1
0	1	DG=2	0	1	DG=2
1	0	DG=4	1	0	DG=4
1	1	DG=8	1	1	DG=8

9.4 Calibration Process

Take calibration with standard meter as example.

1. HFConst configure

   when femu＝5.5296MHz,

   HFConst＝1.244*Vu*Vi*10^11/(EC*Un*Ib)

   Vu: voltage of voltage channel (pin voltage ×PGA gain) under basic voltage input

   Vi: voltage of current channel (pin voltage ×PGA gain) under basic current input

   Un: basic input voltage

   Ib: basic input current

   EC: meter constant

   If femu is of other values, then HFConst's value alters proportionally.

2. Channel 1 active, reactive and apparent gain calibration

   When calibration basic input is needed, and power factor is equal to 1.

   Known:

   The displayed error on standard meter is err

   Calculation formula:

$$Pgain = \frac{-err}{1+err}$$

   If Pgain>=0, then GP1= INT [Pgain*2^{15}]

   Else Pgain<0, then GP1=INT [2^{16}+Pgain*2^{15}]

   Note: INT: get the result's integer

   Write the calculated GP1 value to GQ1 and GS1 at the meantime.

3. channel 1 phase calibration

   Process phase compensation after gain is calibrated (STEP 2). Calibration at power factor 0.5L.

   Known:

   The displayed error on standard meter at 0.5L is err

$$\theta = \frac{-err}{1.732}$$

   If $\theta \geq 0$, then $GPhs = \theta * 2^{15}$

   Else $\theta < 0$, $GPhs = 2^{16} + \theta * 2^{15}$

4. current channel 2 gain calibration(required at anti-tampering scheme)

   When anti-tampering scheme enalbed, it needs to compare the two channels' rms current value, so under the same current inputing, the register value of rms current channel 1 and 2 should be the same.

   Through current channel 2 gains adjustments register I2GAIN(0x4AH, table 9-40), in the similar input current signal,the two rms current register value can be kept consistent.

   When input the same current, the current channel 1 rms register value is I1rms, the current

channel 2 rms register value is I2rms, then

Gain＝I1rms/I2rms - 1

If Gain>=0，I2Gain=Gain*2^15

If Gain<0，I2Gain＝Gain*2^15+2^16

5. The channel 2 gain and phase calibration

The channel 2 gain and phase calibration is similar to the channel 1.

For example:

Suppose to design a meter: 220v (Un), 5A (Ib), 3,200 (EC). The current channel 1 sampling uses 350μΩ shunt. The analog channel gain is 16 times; The voltage uses the divide resistance input and the analog channel gain is 1 time. The voltage value of the on- chip pin is 0.22v; Chooses femu=5.5296MHz/2,

1. Calculate HFConst

Vu＝0.22v

Vi＝5*0.00035*16＝0.028v

HFConst= [1.244*Vu*Vi*10^11/(EC*Un*Ib)]/2

= [1.244*0.220*0.028*10^11/(3200*220*5)]/2

=108.85

HFConst is 0x6C(108)。Write the data into the register HFConst(0x4FH, table 9-45)

2. Gain Calibration

The power source outputs signal with 220v, 5A and the power factor is 1. The error shown in the standard table is 3.8%

Then

Pgain＝-0.038/(1+0.038)=-0.0366

It is less than 0 and must be transformed into the twos complement, then

-0.0366*2^15+2^16=0xFB50H

Write 0xFB50H into registers GP1(0x41H, table 9-31)/GQ1(0x42H, table9-32)/GS1(0x43H, Table9-33) at the same time to complete the Gain Calibration

3. Phase calibration

After completing the Gain Calibration, changes the power factor to 0.5L, the standard meter display error is -0.4%, then

θ=-(-0.004)/1.732=0.0023

Gphs1=0.0023*2^15=75.3

Gphs1 is 0x4BH，write the data into the angle revise regiser Gphs1(0x44H, table 9-34).

10 FLASH

10.1 Introduction

The ATT7025 provides high-dependability, programmable 8-bit flash memory that physically partitioned into three parts: a 8K bytes data memory, a 24K bytes code memory and a 64 bytes information memory.The main feature of the Flash memory is:

- Endurance: at least 500,000 cycles - Data memory and Info memory;
- Endurance:at least 20,000 cycles- code memory.
- Data Retention:more than 100 years at 25℃.
- Access time:50ns（max）
- Page erase capbility:
  1） Data memory 64bytes/page
  2） Code memory 512bytes/page
  3） Information memory 64bytes/page
- Page erase time:
  1）Data memory:2ms(min)
  2）Code memory:20ms(min)
- Mass Erase time:200ms（min）
- Byte programme time:40us（min）
  1) Data memory: 40us（min）
  2) Code memory:20us (min)
- Support write protection for code memory

10.2 Function

10.2.1 PS1 Flash Memory Read Operation

PS1 flash can be read through the PS1MAP（table 10-4）control bit.

When PS1MAP=0, the PS1 can not be accessed directly. If the addresses of 8000H-803FH were read directly , the result 00H would be returned. The access must be processed through FCADR（table 10-5）和FCDAT（table 10-6）**register.** When address is written into FCADR register, the data of the address can be readed from FCDAT. Only the 64 Bytes data in 8000H-803FH can be readed through FCADR and FCDAT.

Note: this two register don't support write operation.

When PS1MAP=1,PS1 flash is Mapping to 8000H-803FH and can be accessed directly by using the instruction MOVC.

10.2.2 Flash Memory Mass Erase Operation

When FOP[1:0] （table 10-4）=11, the Mass erase can be executed by using the instruction MOVX.

Flash memory consists of three parts:a 8K bytes data memory, a 24K bytes code memory and a 64 bytes bytes information memory. All of the conditions of MASS Erase are shown as below:

1. When WRS（table 10-3）=1, the instruction MOVX point to the PM address space if both PMLOCK（table 10-2）and RSLOCK（table 10-2）are set to 1 , PM flash write-protection fuction

is turned off:.On this condition:

1）24K bytes code memory is mapped to PM in addresses 0000H-5FFFH, when using the instruction MOVX to write data to PM space which addresses is located in 0000H-5FFFH,the entire 24k bytes code memory will be mass erased.

2）If DFS[2:0]（table 10-2）＝0xx,8K bytes data memory is mapped to PM in addresses 6000H-7FFFH,and using the instruction MOVX to write data to memory space which address is located in 6000H-7FFFH,the 8k bytes data memory will be erased.

3）If PS1MAP（table 10-4）=1,64 bytes information memory is mapped to PM in addresses 8000H-803FH,When using the instruction MOVX to write data to memory space which address is located in 8000H-803FH,the 64 bytes information memory will be entire erased.

2．When WRS（table 10-3）=1 and PMLOCK（table 10-2）=0 or RSLOCK（table 10-2）=0, PM flash write-protection is enable,MASS Erase operation is forbidden.

3．When WRS（table 10-3）=0, DFS[2:0]（table 10-2）＝111,8K data memory is mapping to DM in addresses 4000H-5FFFH.When using the instruction MOVX to write data to memory space which address is located in 4000H-5FFFH, the 8K bytes data memory will be mass erased.

The status bit BUSY（table 10-4）is set to 1 at the beginning of mass erase and is cleared automatically after mass erase is completed. FOP[1:0]（table 10-4）also return to 00 state automatically after MASS erase is completed. The Mass erase operation times is at least 200ms.

10.2.3 Flash Memory Page Erase Operation

When FOP[1:0]（table 10-4）=10, the Page erase can be executed by using the instruction MOVX, the page which the instruction MOVX acessed will be erased.

Physically, Flash memory has been paginated as follows: Data memory is 64bytes per page;Code memory is 512bytes per page;Information memory is 64bytes per page,actually 64 bytes Information memory can be dealed with as one page. Correspondingly, The PAGE Erase operation has several conditions as follows:

1.When WRS=1（table 10-3）,code memory can be page erased by using the instruction MOVX , if PMLOCK（table 10-2）=1 and RSLOCK（table 10-2）=1 the flash write-protect function is turn off:On this condition:

1）24K bytes code memory is mapped to PM space that is located in address 0000H-5FFFH, When using the instruction MOVX to write data to memory space which address is located in 0000H-5FFFH , the corresponding page of 24K bytes code memory (512bytes/ page) can be erased.

2）If DFS[2:0]（table 10-2）＝000,8K bytes data memory is mapped to PM in addresses 6000H-7FFFH,when using the instruction MOVX to write data to memory space which address is located in 6000H-7FFFH ,the corresponding page of 8K bytes data memory (64bytes/ page) can be erased.

3）If PS1MAP（table 10-2）=1,64 bytes information memory is mapped to PM 8000H-803FH,When using the instruction MOVX to write data to memory space which address is located in 8000H-803FH, the 64 bytes information memory can be erased.

2．When WRS=1, but PMLOCK=0, PM Flash write-protect function is enabled, Page Erase operation is forbidden..

3．When WRS=1, PMLOCK=1, but RSLOCK=0, wirte protection of the former 4K bytes of PM is enable. The former 4K bytes of PM can not be erased while the other pages are similar to

situation 1.

4．When WRS=0, the operating address of the instruction MOVX is DM space. If DFS[2:0] ＝ 111,8K bytes data memory is mapped to DM space that is located in address 4000H-5FFFH,when using the instruction MOVX to write data to memory space which address is located in 4000H-5FFFH, the corresponding page of 8K bytes data memory (64bytes/ page) is erased.

BUSY status bit（**table 10-4**）is set to 1 at the beginning of page erase operation and is cleared automatically when page erase is completed. FOP[1:0] （**table 10-4**）also return to 00 state automatically when page erase is completed.

NOTE: when multipage erase is wanted, FOP[1:0] must be reloaded before erasing the next page.

The Page erase time:Data memory/information memory:2ms(min);Code memory:20ms(min).

10.2.4 Flash Memory Byte Program Operation

When FOP[1:0] （**table 10-4**）=01,byte program operation can be completed using the instruction MOVX ,such as MOVX @DPTR,A or MOVX @Ri,A etc.Byte program operation also has several conditions as follows:

1．When WRS=1（**table 10-3**）,the acessing address of the instruction MOVX is PM space, If PMLOCK（**table 10-2**）=1 and RSLOCK（**table 10-2**）=1, write protection for flash memory is disable.On this condition:

1）24K code memory is mapped to PM space that is located in address 0000H-5FFFH,When using the instruction MOVX to write data to memory space which address is located in 0000H-5FFFH, the code memory can be byte programmed.

2）When DFS[2:0] （**table 10-2**）＝000,8K data memory is mapping to PM 6000H-7FFFH,when MOVX address is located in PM 6000H-7FFFH, the corresponding 8K data memory byte can be programmed.

3）When PS1MAP（**table 10-2**）=1,64 bytes information memory is mapping to PM 8000H-803FH,when MOVX address is PM 8000H-803FH,the corresponding information memory byte can be programmed.

2．When WRS=1, but PMLOCK=0, PM Flash write-protect function is enable and byte program operation is abate.

3．When WRS=1, PMLOCK=1, but RSLOCK=0, the write-protect function of the former 4K of PM is enable. The former 4K of PM page can not be byte programmed while the other pages are similar to situation 1.

4．When WRS=0, MOVX points to DM space.If DFS[2:0]＝111,8K data memory is mapping to DM 4000H-5FFFH.If MOVX address is in DM 4000H-5FFFH, the corresponding 8K data memory byte is programmed.

BUSY status bit（**table 10-4**）is set to 1 at the beginning of byte Program and is cleared automatically after programming is completed. FOP[1:0] （**table 10-4**）also return to 00 state automatically after programming is completed.

NOTE: FOP[1:0] must be restore to 01h before programming the next byte.The byte programe time is 40us（min）.

10.2.5 PM Flash Write-protection

Configure the PMLOCK bit and the RSLOCK bit of FMCFG(**table 10-4**)register can control the PM Flash write-protect function. When PMLOCK=1, the erase/byte program function of PM Flash in UAM mode is enable.When PMLOCK=0 the PM Flash is in read-only mode and can not be amended. When RSLOCK=1, if PMLOCK=1 at the same time, the erase/byte program function of the former 4K PM Flash is enable. When RSLOCK=0,No matter PMLOCK=1 or 0,the former 4K PM Flash is in read-only mode and cannot be amended.

Note: the PMLOCK and the RSLOCK is only in effect to the PM Flash.

10.3 Registers

Table 10-1 FLASH register list

address	name	reset value	function
0xBE	FMCFG	0x00	Flash memory configure register —see **table 10-2**,write-protect
0x8F	SPC_FNC	0x00	DM/PM select register—see **table 10-3**
0xE9	FMCON	0x00	Flash memory control register—see **table 10-4**
0xEE	FCADR	0x00	PS1 Flash Address Register—see **table 10-5**
0xEF	FCDAT	0x00	PS1 Flash Data Register—see **table 10-6**

1. Flash memory configure register（write-protect）

Table 10-2 Flash memory configure register (0xBEH, FMCFG)

FMCFG			Address: BEH					
	Bit7	6	5	4	3	2	1	Bit0
Read:	DFS2	DFS1	DFS0	0	0	BROMEN	PMLOCK	RSLOCK
Write:				X	X			
Reset:	0	0	0	0	0	0	0	0

Bit	Function
FMCFG[7:5]	DFS[2:0] :when DFS[2:0]=111,8K-bytes Data Flash Memory is mapping in DM address space:4000-5FFFH; when DFS[2:0]=0xx,Data Flash Memory is mapping to PM address space:6000-7FFFH;After reset,DFS[2:0]=000,Code Flash and Data Flash build up continuous 32K program memory, the address is 0000-7FFFH.
FMCFG.1	PMLOCK:PMLOCK=1,in the UAM mode , the PM Flash erase/wrie function is enable. PMLOCK=0,in the UAM mode,the PM Flash is in read-only mode and cannot be amended. ***NOTE:****the PMLOCK and the RSLOCK is only in effect to the PM Flash*
FMCFG.0	RSLOCK:In the UAM mode,if RSLOCK=1,at the same time PMLOCK=1,then the erase/write function of the former 4K PM Flash is enable. RSLOCK=0:in the UAM mode,even if PMLOCK=1,the former 4K

DFS2	DFS1	DFS0	Size assignment		Address assignment	
			PM	DM	PM	DM
0	x	x	32K	0K	0000-7FFF	0000
1	1	1	24K	8K	0000-5FFF	4000-5FFF
Others			x	x	Reserved	Reserved

NOTE:If configure the DFS[2:0] as the value except 0xx and 111 , the

	PM Flash is in read-only mode and cannot be amended. ***NOTE:****the PMLOCK and the RSLOCK is only in effect to the PM Flash*

2. DM/PM choose register

Table 10-3 DM/PM choose register (0x8FH, SPC_FNC)

SPC_FNC			Address: 8FH					
	Bit7	6	5	4	3	2	1	Bit0
Read:	0	0	0	0	0	0	0	WRS
Write:	X	X	X	X	X	X	X	
Reset:	0	0	0	0	0	0	0	0

Note :when processing the mass erase、page erase and byte programe functions on the Flash,the WRS is used for distinguish between the address of the DM flash and the address of the PM flash;WRS=0 shows the DM Flash can be amended, WRS=1 shows the PM Flash Can not be amended.

3. Flash memory control register

Table 10-4 Flash visit control register (0x8FH, SPC_FNC)

Flash Memory Control Register (FMCON)			Address: E9H					
	Bit7	6	5	4	3	2	1	Bit0
Read:	PS1MAP	FOP1	FOP0	0	0	BUSY	SPMOD	0
Write:				X	X	X	X	X
Reset:	0	0	0	0	0	0	0	0

Bit	Function
FMCON.7	PS1MAP:PS1MAP=1:PS1 Flash Memory is mapping to 8000H-803FH address space;PS1MAP=0:the PS1 read function can be processed through the register FCADR and FCDAT.
FMCON[6:5]	FOP[1:0]:FOP[1:0]=00,be in Flash read-only mode;FOP[1:0]=01,MOVX will perform the Flash write function ;FOP[1:0]=10,MOVX will perform the FlashPage erase function ; FOP[1:0]=11,MOVX will perform the Flash mass erase function ;
FMCON[4:3]	Reserved.
FMCON.2	BUSY:BUSY=1: Flash is in the process of erase/byte program.,;BUSY=0:showthe Flash is free and can be operated.
FMCON.1	See on-chip ICE chapter
FMCON.0	Reserver

4. PS1 Flash Address Register

Table 10-5 PS1 Flash Address Register (0xEEH,FCADR)

PS1 Flash Address Register (FCADR)			Address: EEH					
	Bit7	6	5	4	3	2	1	Bit0
Read:	FCADR7	FCADR6	FCADR5	FCADR4	FCADR3	FCADR2	FCADR1	FCADR0
Write:								
Reset:	0	0	0	0	0	0	0	0

Note: when PS1MAP=0,read the data of the corresponding address through FCDAT after writing the address into the FCADR. Only the read function is provided.

5. PS1 Flash Data Register

Table 10-6 PS1 Flash Data Register (0xEFH,FCDAT)

PS1 Flash Data Register (FCDAT)			Address: EFH					
	Bit7	6	5	4	3	2	1	Bit0
Read:	FCDAT7	FCDAT6	FCDAT5	FCDAT4	FCDAT3	FCDAT2	FCDAT1	FCDAT0
Write:	X	X	X	x	X	X	X	X
Reset:	0	0	0	0	0	0	0	0

Note :This register is used with the FCADR.

10.4 One Way to Write Data Flash

ATT7025's 8K Data Flash can replace EEPROM as the data memory. The programs include Data Flash page erase and byte program operation. One simple way via Monitor ROM routines to write data flash is provided. In UAM mode, the entrance address is 0xffd9h. Before the routines are accessed, the global interrupt should be closed.

The programme of page erase and byte program operation:

```
MOV     9AH,#0C3H                ; Write-protection off
MOV     9AH,#9BH
ORL     0BEH,#04H                ; Boot Rom routines can be accessed

PUSH    IE                       ; Save EA scene
CLR     EA                       ; Close global interrupt
MOV     8FH,#000H                ; Select Data Flash
MOV     DPTRH0,#40H              ; High address of page erase
MOV     DPTRL0,#01H              ; Low address of page erase
ORL     0E9,#40H                 ; Select Data Flash for page erase
MOV     A,#0FFH
LCALL   0FFD9H                   ; Use Monitor Rom routines for page erase
MOV     8FH,#000H                ; Select Data Flash
MOV     DPTRH0,#40H              ; Give Data Flash address
MOV     DPTRL0,#01H
MOV     A,#0AAH                  ; Give write data
ORL     0E9,#20H                 ; enable flash write operation
LCALL   0FFD9H                   ; Use Monitor Rom routines for byte program
POP     IE                       ; resume EA scene
```

Note: Data Flash is 64bytes per page. Every byte address located in the page can be the page address. The address is in DPTR register, and the write data is in A register.

11 Timer/ Counters

11.1 Introduction

The ATT7025 has three 16-bit timer/ counters: Timer 0, Timer 1, and Timer 2. All three can be configured to operate either as timers or as event counters.

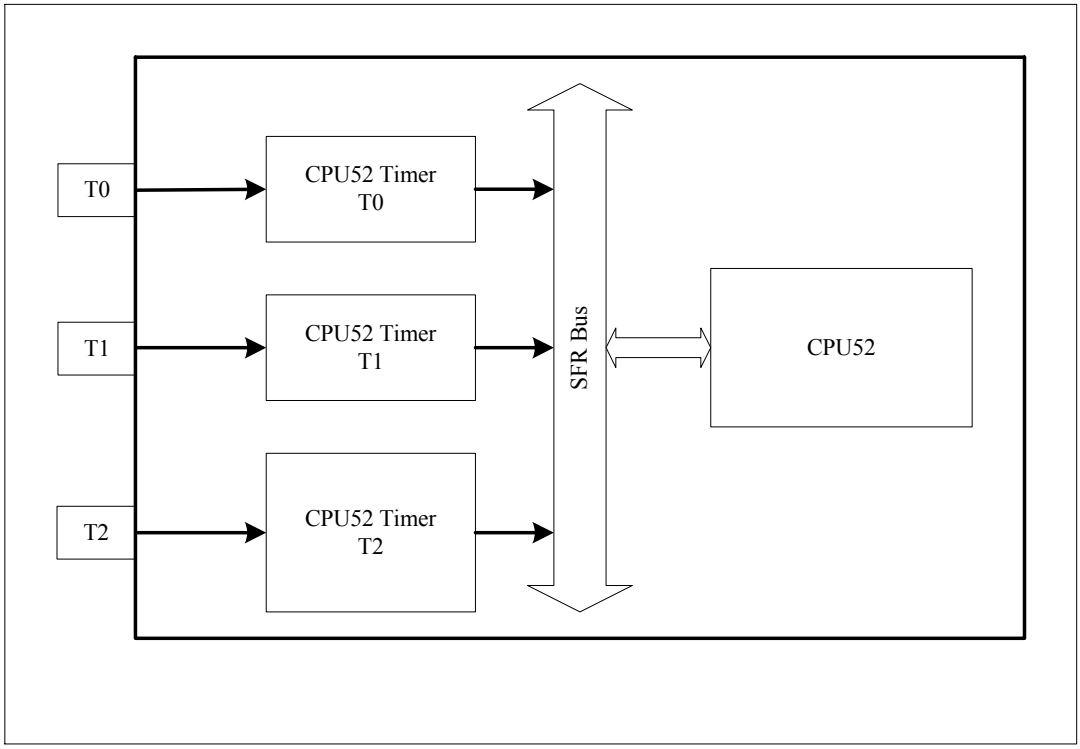


Figure 11-1 ATT7025 timer/ counters

Each timer/counter consists of two 8-bit registers: THx and TLx (x = 0, 1, or 2).

Timer0:TL0 and TH0

Timer1:TL1 and TH1

Timer2:TL2 and TH2

11.2 Timer0 and Timer1

Timers 0 and 1 each operate in four modes, as controlled through the TMOD SFR(table 11-2) and the TCON SFR (table 11-3). The four modes are:

• 13-bit timer/counter (mode 0)

• 16-bit timer/counter (mode 1)

• 8-bit counter with auto-reload (mode 2)

• Two 8-bit counters (mode 3, Timer 0 only)

11.2.1 Registers

Table 11-1 Timer0 and Timer1 register list

address	name	reset	description
0x8A	TL0	0x00	timer0/counter low 8 bit
0x8B	TL1	0x00	Timer1/counter low 8 bit
0x8C	TH0	0x00	timer0/counter high 8 bit
0x8D	TH1	0x00	timer0/counter high 8 bit

0x88	TCON	0x00	timer control register
0x89	TMOD	0x00	timer mode register

Table 11-2 Timer0 and Timer1Mode Rigister(TMODE 0x89H)

Timer0 and Timer1 Mode Register (TMODE)			**Address:**	**89H**				
	Bit7	**6**	**5**	**4**	**3**	**2**	**1**	**Bit0**
Read: **Write:**	GATE	$C/\overline{T}$	M1	M0	GATE	$C/\overline{T}$	M1	M0
Reset:	0	0	0	0	0	0	0	0

bit	**description**
TMOD.7	GATE – Timer 1 gate control. When GATE = 1, Timer 1 will clock only when int1_n = 1 and TR1 (TCON.6) = 1. When GATE = 0, Timer 1 will clock only when TR1 = 1, regardless of the state of int1_n. （see **fig 11-2**）。
TMOD. 6	C/T – Counter/Timer select. When C/T = 0, Timer 1 is clocked by clk/4 or clk/12, depending on the state of T1M (CKCON.4). When C/T = 1, Timer 1 is clocked by the t1 pin.
TMOD.5	M1 – Timer 1 mode select bit 1.
TMOD. 4	M0 – Timer 1 mode select bit 0, decoded as: M1 | M0 | mode | explain 0 | 0 | 0 | 13-bit counter 0 | 1 | 1 | 16-bit counter 1 | 0 | 2 | 8-bit counter with auto-reload 1 | 1 | 3 | Two 8-bit counters
TMOD.3	GATE – Timer 0 gate control. When GATE = 1, Timer 0 will clock only when int0_n = 1 and TR0 (TCON.4) = 1. When GATE = 0, Timer 0 will clock only whenTR0 = 1, regardless of the state of int0_n. （see **fig 11-2**）。
TMOD.2	C/T – Counter/Timer select. When C/T = 0, Timer 0 is clocked by clk/4 or clk/12, depending on the state of T0M (CKCON.3). When C/T = 1, Timer 0 is clocked by the t0 pin.
TMOD.1	M1 – Timer 0 mode select bit 1.
TMOD.0	M0 – Timer 0 mode select bit 0, decoded as: M1 | M0 | mode | explain 0 | 0 | 0 | 13-bit counter 0 | 1 | 1 | 16-bit counter 1 | 0 | 2 | 8-bit counter with auto-reload 1 | 1 | 3 | Two 8-bit counters

Table 11-3 Timer0 and Timer1 Control Register (TCON 0x88H)

Timer0 and Timer1 Control Register (TCON)			**Address:**	**88H**				
	Bit7	**6**	**5**	**4**	**3**	**2**	**1**	**Bit0**
Read: **Write:**	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
Reset:	0	0	0	0	0	0	0	0

bit	**function**
TCON.7	TF1 – Timer 1 overflow flag. Set to 1 when the Timer 1 count overflows and cleared when the CPU vectors to the interrupt service routine.
TCON.6	TR1 – Timer 1 run control. Set to 1 to enable counting on Timer 1.

TCON.5	TF0 – Timer 0 overflow flag. Set to 1 when the Timer 0 count overflows and cleared when the CPU vectors to the interrupt service routine.
TCON.4	TF0 – Timer 0 overflow flag. Set to 1 when the Timer 0 count overflows and cleared when the CPU vectors to the interrupt service routine.

11.2.2 Function Description

11.2.2.1 Mode0

Mode 0 operation, illustrated in Figure 11-2, is the same as Timer 0 and Timer 1. In mode 0, the timer is configured as a 13-bit counter that uses bits 0–4 of TL0 (or TL1) and all 8 bits of TH0 (or TH1). The timer enable bit (TR0/TR1) in the TCON SFR starts the timer. The C/T bit selects the timer/counter clock source, *clk* or *t0/t1*.

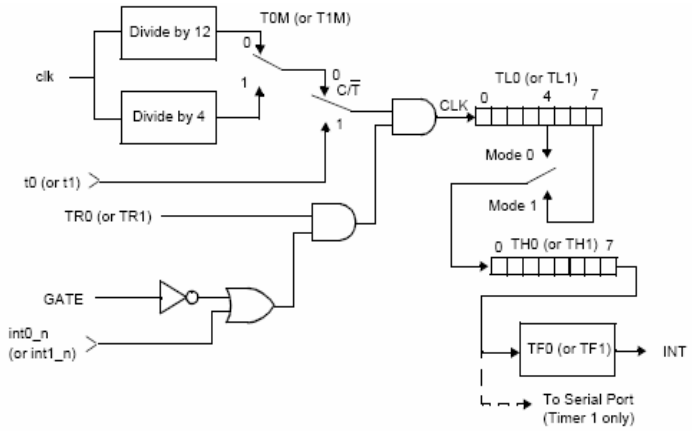


Figure 11-2 Timer 0/1 – Modes 0 and 1

The timer counts transitions from the selected source as long as the GATE bit is 0, or the GATE bit is 1 and the corresponding interrupt pin (*int0_n* or *int1_n*) is deasserted. When the 13-bit count increments from 1FFFh (all ones), the counter rolls over to all zeros, the TF0 (or TF1) bit is set in the TCON SFR, and the *t0_out* (or *t1_out*) pin goes high for one clock cycle. The upper 3 bits of TL0 (or TL1) are indeterminate in mode 0 and must be masked when the software evaluates the register.

11.2.2.2 Mode1

Mode 1 operation is the same for Timer 0 and Timer 1. In mode 1, the timer is configured as a 16-bit counter. As illustrated in Figure 11-2, all 8 bits of the LSB register (TL0 or TL1) are used. The counter rolls over to all zeros when the count increments from FFFFh. Otherwise, mode 1 operation is the same as mode 0.

11.2.2.3 Mode2

Mode 2 operation is the same for Timer 0 and Timer 1. In mode 2, the timer is configured as an 8-bit counter, with automatic reload of the start value. The LSB register (TL0 or TL1) is the counter and the MSB register (TH0 or TH1) stores the reload value. As illustrated in fig 11-3, mode 2 counter control is the same as for mode 0 and mode 1. However, in mode 2, when TL*n* increments from FFh, the value stored in TH*n* is reloaded into TL*n*.

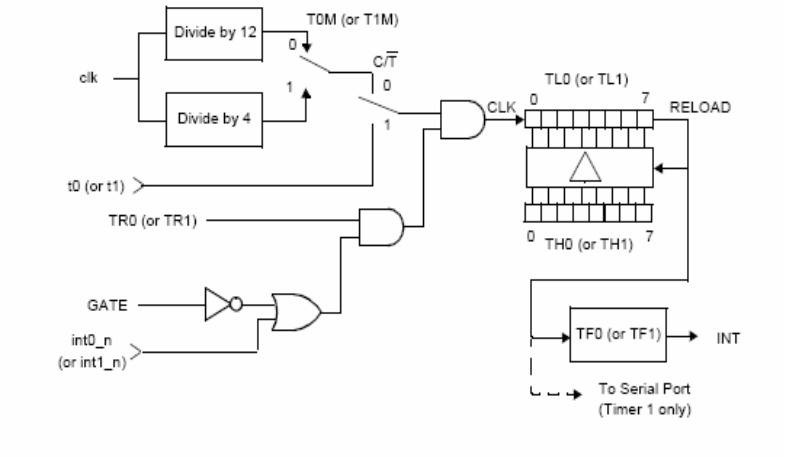


Figure11-3 Timer 0/1 – Mode 2

11.2.2.4 Mode3

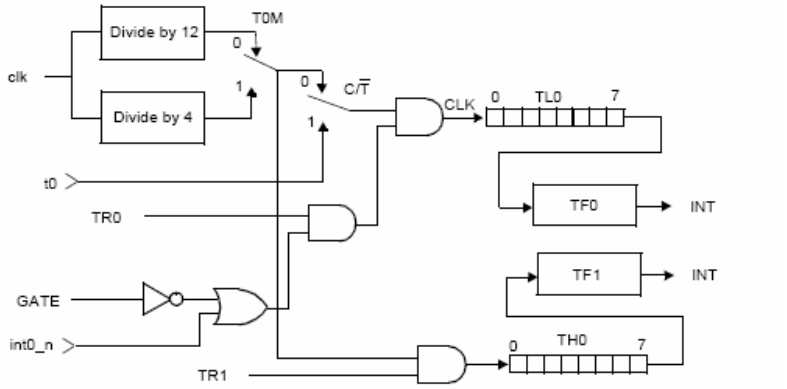


Figure 11-4 Timer 0 – Mode 3

In mode 3, Timer 0 operates as two 8-bit counters and Timer 1 stops counting and holds its value.

As shown in Figure 11-4, TL0 is configured as an 8-bit countercontrolled by the normal Timer 0 ontrol bits. TL0 can either count *clk* cycles (divided by 4 or by 12) or high-to-low transitions on *t0*, as determined by the C/T bit. The GATE function can be used to give counter enable control to the *int0_n* signal. TH0 functions as an independent 8-bit counter. However, TH0 can only count *clk* cycles (divided by 4 or by 12). The Timer 1 control and flag bits (TR1 and TF1) are used as the control and flag bits for TH0. When Timer 0 is in mode 3, Timer 1 has limited usage because Timer 0 uses the Timer 1 control bit (TR1) and interrupt flag (TF1). Timer 1 can still be used for baud rate generation and the Timer 1 count values are still available in the TL1 and TH1 registers. Control of Timer 1 when Timer 0 is in mode 3 is through the Timer 1 mode bits. To turn Timer 1 on, set Timer 1 to mode 0, 1, or 2. To turn Timer 1 off, set it to mode 3. The Timer 1 C/T bit and T1M bit are still available to Timer 1. Therefore, Timer 1 can count *clk*/4, *clk*/12, or high-to-low transitions on the *t1* pin. The Timer 1 GATE function is also available when Timer 0 is in mode 3.

11.3 Timer2

Timer 2 runs only in 16-bit mode and offers several capabilities not available with Timers 0 and 1. The modes available with Timer 2 are:

• 16-bit timer/counter

• 16-bit auto-reload timer/counter

• Baud rate generator

11.3.1 Registers

The SFRs associated with Timer 2 are:

• T2CON – SFR C8h (**table 11-5)**

• RCAP2L – SFR CAh – Used to capture the TL2 value when Timer2 is configured for capture mode, or as the LSB of the 16-bit reload value when Timer 2 is configured for auto-reload mode.

• RCAP2H – SFR CBh – Used to capture the TH2 value when Timer2 is configured for capture mode, or as the MSB of the 16-bit reload value when Timer 2 is configured for auto-reload mode.

• TL2 – SFR CCh – Lower 8 bits of the 16-bit count.

• TH2 – SFR CDh – Upper 8 bits of the 16-bit count.

Table 11-4 Timer2 Control Register (T2CON 0xC8H)

Timer2 Control Register (T2CON)			**Address:** C8**H**					
	Bit7	**6**	**5**	**4**	**3**	**2**	**1**	**Bit0**
Read:	TF2	0	RCLK	TCLK	0	TR2	$C/\overline{T2}$	0
Write:		x			x			x
Reset:	0	0	0	0	0	0	0	0

bit	**description**
T2CON.7	TF2 – Timer 2 overflow flag. Hardware will set TF2 when Timer 2 overflows from FFFFh. TF2 must be cleared to 0 by the software. TF2 will only be set to a 1 if RCLK and TCLK are both cleared to 0. Writing a 1 to TF2 forces a Timer 2 interrupt if enabled.
T2CON.6	. Reserved. Reset is 0.
T2CON.5	RCLK – Receive clock flag. Determines whether Timer 1 or Timer 2 is used for Serial Port 0 timing of received data in serial mode 1 or 3. RCLK =1 selects Timer 2 overflow as the receive clock. RCLK = 0 selects Timer 1 overflow as the receive clock.
T2CON.4	TCLK – Transmit clock flag. Determines whether Timer 1 or Timer 2 is used for Serial Port 0 timing of transmit data in serial mode 1 or 3. TCLK =1 selects Timer 2 overflow as the transmit clock. TCLK = 0 selects Timer 1 overflow as the transmit clock.
T2CON.3	. Reserved. Reset is 0. Change this bit will has the uncertain result
T2CON.2	TR2 – Timer 2 run control flag. TR2 = 1 starts Timer 2. TR2 = 0 stops Timer 2
T2CON.1	C/T2 – Counter/timer select. C/T2 = 0 selects a timer function for Timer 2. C/T2 = 1 selects a counter of falling transitions on the t2 pin. When used as a timer, Timer 2 runs at 4 clocks per increment or 12 clocks per increment as programmed by CKCON.5, in all modes except baud rate generator mode. When used in baud rate generator mode, Timer 2 runs at 2 clocks per increment, independent of the state of CKCON.5.
T2CON.0	Reserved. Reset is 0,Change this bit will has the uncertain result.

Table 11-5 Timer2 Mode Control Summary

RCLK	TCLK	TR2	Timer2 mode
0	0	1	16-bit timer/counter with auto-reload
1	x	1	Baud rate generator

x	1	1	Baud rate generator

11.3.2 Function Description

11.3.2.1 16-Bit Timer/Counter Mode

Fig 11-5 illustrates how Timer 2 operates in timer/counter mode with the optional capture feature. The C/T2 bit determines whether the 16-bit counter counts *clk* cycles (divided by 4 or 12), or high-to-low transitions on the *t2* pin. The TR2 bit enables the counter. When the count increments from FFFFh, the TF2 flag is set, and *t2_out* goes high for one *clk* cycle.

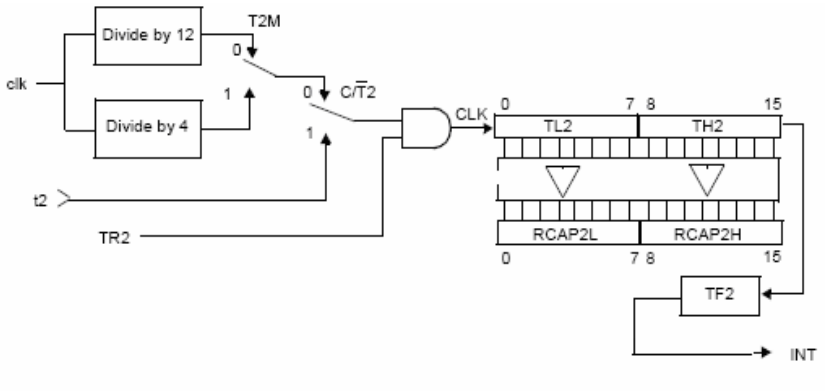


Figure 11-5 Timer 2 – Timer/Counter with Capture

11.3.2.2 16-Bit Timer/Counter Mode with Auto-Reload

When CP/RL2 = 0, Timer 2 is configured for the auto-reload mode illustrated in Figure 11-6. Control of counter input is the same as for the other 16-bit counter modes. When the count increments from FFFFh, Timer 2 sets the TF2 flag and the starting value is reloaded into TL2 and TH2. The software must preload the starting value into the RCAP2L and RCAP2H registers. When Timer 2 is in auto-reload mode, a reload can be forced by a high-to-low transition on the *t2ex* pin, if enabled by EXEN2 = 1.

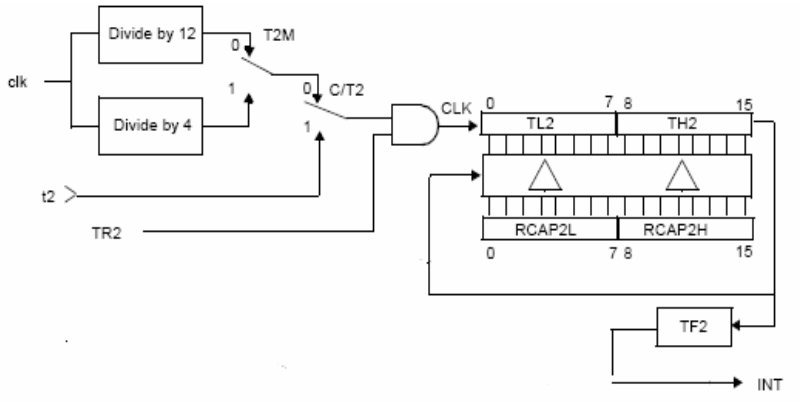


Figure 11-6 Timer 2 – Timer/Counter with Auto-Reload

11.3.2.3 Baud Rate Generator Mode

Setting either RCLK or TCLK to 1 configures Timer 2 to generate baud rates for Serial Port 0 in serial mode 1 or 3. In baud rate generator mode, Timer 2 functions in auto-reload mode. However,

Instead of setting the TF2 flag, the counter overflow generates a shift clock for the serial port

function. As in normal auto-reload mode, the overflow also causes the preloaded start value in the RCAP2L and RCAP2H registers to be reloaded into the TL2 and TH2 registers. When either TCLK = 1 or RCLK = 1, Timer 2 is forced into auto-reload operation, regardless of the state of the CP/RL2 bit. When operating as a baud rate generator, Timer 2 does not set the TF2 bit. In this mode, a Timer 2 interrupt can only be generated by a high-to-low transition on the *t2ex* pin setting the EXF2 bit, and only if enabled by EXEN2 = 1.

The counter time base in baud rate generator mode is *clk*/2. To use an external clock source, set C/T2 to 1 and apply the desired clock source to the *t2* pin.

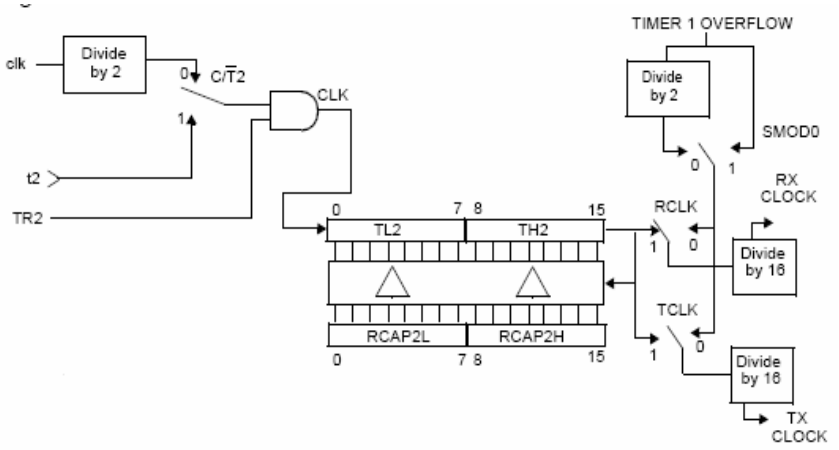


Figure 11-7 Timer 2 – Baud Rate Generator Mode

11.4 Timer Rate Control

The default timer clock scheme for the ATT7025 timers is 12 *clk* cycles per increment, the same as in the standard 8051. However, in the ATT7025, the instruction cycle is 4 *clk* cycles. Using the default rate (12 clocks per timer increment) allows existing application code with real-time dependencies, such as baud rate, to operate properly. However, applications that require fast timing can set the timers to increment every 4 *clk* cycles by setting bits in the Clock Control register (CKCON) at SFR location 8Eh (see Table 11-6).

Table 11-6 Clock Control Register (CKCON 0x8EH)

Clock Control Register (CKCON)			**Address:** 8E**H**					
	Bit7	**6**	**5**	**4**	**3**	**2**	**1**	**Bit0**
Read:	0	0	T2M	T1M	T0M	0	0	0
Write:	x	x				x	x	x
Reset:	0	0	0	0	0	0	0	0

bit	function
CKCON.7,6	Reserved.Reset is 0
CKCON.5	T2M – Timer 2 clock select. When T2M = 0, Timer 2 uses clk/12 (for compatibility with 80C32); when T2M = 1, Timer 2 uses clk/4. This bit has no effect when Timer 2 is configured for baud rate generation.
CKCON.4	T1M – Timer 1 clock select. When T1M = 0, Timer 1 uses clk/12 (for compatibility with 80C32); when T1M = 1, Timer 1 uses clk/4.
CKCON.3	T0M – Timer 0 clock select. When T0M = 0, Timer 0 uses clk/12 (for compatibility with 80C32); when T0M = 1, Timer 0 uses clk/4.

12 RTC

12.1 Function

The RTC provides real time clock and calendar functions with automatic leap year adjustments. Other functions include alarm interrupt and periodic interrupts.

The RTC module can't be turned off and can be active in low power mode.

For the veracity of the RTC, all of the RTC output registers (Time&Calendar) and RTC clock Calibration Register can't be reset

12.1.1 Features

• Provide time and Calendar function. The output registers consist of second, minute, hour, day, week, month, and year.

• Day counter with automatic month and leap year adjustment

• 7 periodical interrupts

• 1 clock interrupt

• The output frequency before Calibration is 1024/32768Hz

• The output frequency after Calibration is 1/2/4/8/32/128Hz

12.1.2 Clock Calibration

The external 32.768 KHz crystal is used as the clock source of the RTC module. Calibration is provided to compensate the crystal frequency variations and the temperature drift.

Register RTCCAL(0xF2H) can calibrate the crystal oscillator, which can ensure the internal clock number per minute is equal to the number of the standard 32768Hz.

The TOUT pin is needed for calibration. First, when TOUT[2:0]=111, TOUT pin will output the crystal frequency before calibration. Second, the frequency is tested by high accuracy frequency meter and the calibration value is calculated. Third, the variations value RTCCAL (0xF2H) is saved to FLASH and will be written to the register after power-up. Last, the calibration effect can also be judged by testing the ouput frequency of the TOUT pin when TOUT[2:0] is configured as the frequency after calibration.

RTC calibration is done 5 times per minute, equal to 1 times per 12s. (The calibration period is not recurrent, but the calibration point per minute is recurrent.)

The RTCCAL (0xF2H) represents to increase or decrease N low frequency oscillator clock time per calibration. Increasing the time, the RTC time displayed will slow down; decreasing the time, the RTC time displayed will quicken.

CAL7 is a sign bit. CAL7=0 means decreasing time, here N=[CAL6:CAL0]. CAL7=1 means increasing time, here N=~[CAL6:CAL0]+1. The resolution is 1/(32768*12) = 1/0.393216 ppm=2.54ppm.

For example, the RTCCAL register value 0x02H means decreasing two low frequency oscillator clocks time per calibration, and the dispayed time will slow down 2/32768=61μs per calibration.

The RTCCAL=0xaf=1010_1111 means increasing oscillator clocks time per calibration because the highest bit is 1. The number of clocks is the bit-wise negation operation of low 7 bit 0x2f, ie. 0x52(81). So the displayed time will quicken 81/32768=0.002471923828125s per calibration.

Table 12-1 RTCCAL operation example

RTCCAL	RTCCAL binary	increase/decrease	Number
0x00	0_000_0000	**decrease**	000_0000=0x00=00
0x01	0_000_0001	**decrease**	000_0001=0x01=01
0x50	0_101_0000	**decrease**	101_0000=0x50=80
0x51	0_101_0001	**decrease**	101_0001=0x51=81
0x7f	0_111_1111	**decrease**	111_1111=0x7f=127
0x80	1_000_0000	increase	~(000_0000)+1=000_0000=0x00=00
0x81	1_000_0001	increase	~(000_0001)+1=111_1111=0x7f=127
0x82	1_000_0010	increase	~(000_0010)+1=111_1110=0x7e=126
0xaf	1_010_1111	increase	~(010_1111)+1=101_0001=0x51=81
0xb0	1_011_0000	increase	~(011_0000)+1=101_0001=0x50=80
0xfe	1_111_1110	increase	~(111_1110)+1=000_0010=0x02=2
0xff	1_111_1111	increase	~(111_1111)+1=000_0001=0x01=1

12.1.3 Time and Calendar

The ATT7025 provides second, minute, hour, day, month, year and week output registers. Calendar functions are provided by these registers. The roll over of the day counter is automatically adjusted for the month and leap years. The setting for the year counter ranges from January 1, 2000 to December 31, 2099.

Week needs initialization processing. After the initialization, the register is updated with the day.

12.1.4 RTC Register Write-protect

When Calibrating the time and calendar, all the time counter will not stop. Counters continue to accumulate if registers have been modified. Because the counters doesn't stop when calibration, possible carry must be considerd.

The output registers of RTC(SECR, MINR, HRR, DAYR, MTHR, YRR and DOWR） are write-protected and can not be reset.

After write-protect function is turned off, writing is only valid in 128 cycle time, equel to 32 single-cycle instruments at most. So the configuration process can not be broke by interrupt. If the time can't be guaranteed, EA should be turned off first and be turned on after configuration. Also the process can be divided into two or more steps, only needing to turn off write-protect function in every step.

For example, the configuration of Second Register (0F9H) show as below:

```
CLR     EA                  ;
MOV     BWPR, #0C3H         ; slect write enable mode
MOV     BWPR, #08BH          ;enable RTC-proctec-reg write
MOV     0F9H,#010H           ; config RTC SECR
…                           ; other RTC config operation,
MOV     BWPR, #0A8H         ; close RTC reg writing;
                            ; may neglect, it will be closed in 128 cpu clk
SETB    EA
```

(BWPR is 09AH)

Configuration registers include RTCCON, RTCCAL, SECCNT, ALMR, ALHR, RTCIE, and RTCIF. RTCCAL is the write-protect register and can not be reset. The others are normal registers , which can be reset and is not write-protect registers.

12.1.5 Interrupt

The RTC has 8 interrupts, sharing the MCU IRQ_RTC interrupt. These interrupts enabled are controlled by the RTCIE (AAH) and the interrupt flags are in the RTCIF(B2H).

The detailed interrupts include the following:

ALMF: Alarm Interrupt Flag

This clearable, read-only bit is set when the value in the RTC hour and minute counters matches the value in the alarm hour and alarm minute registers. When the ALMIE bit is set, ALMF generates a CPU interrupt request.

In normal operation, clear the ALMF bit by reading RTCIF with ALMF set and then reading the alarm hour register (ALHR).

SCNTF: second timer interrupt Flag

This clearable, read-only bit is set when the value in the second counter matches the value in SECCNT register. When the SCNTIE bit is set, SCNTF generates a CPU interrupt request.

In normal operation, clear the SCNTF bit by reading RTCIF with SCNTF set and then reading the Second Counter Overflow register (SECCNT).

RTC2F: timer 2 interrupt Flag

This clearable, read-only bit is set every 0.25s or 0.0625s. When the RTC2IE bit is set, RTC2F generates a CPU interrupt request.

In normal operation, clear the RTC2F bit by reading RTCIF with RTC2F set and then reading the Month register (MTHR).

RTC1F: timer 1 interrupt Flag

This clearable, read-only bit is set every 0.5s or 0.125s. When the RTC1IE bit is set, RTC1F generates a CPU interrupt request.

In normal operation, clear the RTC1F bit by reading RTCIF with RTC1F set and then reading the Year register (YRR).

DAYF: day interrupt Flag

This clearable, read-only bit is set every increment of the day counter. When the DAYIE bit is set, DAYF generates a CPU interrupt request.

In normal operation, clear the DAYF bit by reading RTCIF with DAYF set and then reading the Day register (DAYR).

HRF: hour interrupt Flag

This clearable, read-only bit is set every increment of the hour counter. When the HRIE bit is set, HRF generates a CPU interrupt request.

In normal operation, clear the HRF bit by reading RTCIF with HRF set and then reading the Hour register (HRR).

MINF: minute interrupt Flag

This clearable, read-only bit is set every increment of the minute counter. When the MINIE bit is set, MINF generates a CPU interrupt request.

In normal operation, clear the MINF bit by reading RTCIF with MINF set and then

reading the Minute register (MINR).

SECF: second interrupt Flag

This clearable, read-only bit is set every increment of the second counter. When the SECIE bit is set, SECF generates a CPU interrupt request.

In normal operation, clear the SECF bit by reading RTCIF with SECF set and then reading the Second register (SECR).

The notes of RTC interrupt clear:

RTC uses the low frequency oscillator clock (32.768kHz) as the clock. When clearing the interrupt, one clock period (30.6us) wait is needed.

Correct process of interrupt clear is as below:

1. Clear RTC IF (0xB2) flag (need 30.6us wait time);
2. Clear CPU INT3_N flag.

Wait time can be realized in two ways:

1. Add nop command;
2. Wait RTC IF flag until it is cleared.

12.2 Registers

table 12-2 register list

Address	Name	Byte length	Function
F1H	RTCCON	1	RTC Control register
F2H	RTCCAL	1	RTC Clock Calibration register, write-protect
F3H	SECCNT	1	RTC Second Counter Overflow Register
F4H	ALMR	1	Alarm Minute Register
F5H	ALHR	1	Alarm Hour register
F9H	SECR	1	RTC Second Register, write-protect
FAH	MINR	1	RTC Minute register, write protect
FBH	HRR	1	RTC Hour register, write protect
FCH	DAYR	1	RTC Day register, write protect
FDH	MTHR	1	RTC Month register, write protect
FEH	YRR	1	RTC Year register, write protect
FFH	DOWR	1	RTC Week register, write protect
AAH	RTCIE	1	RTC Interrupt Enable Register
B2H	RTCIF	1	RTC Interrupt Flag Register
9AH	BWPR	1	RTC Write-protect register

Table 12-3 RTC Control Register

RTC Control Register (RTCCON)			Address: F1H					
	Bit7	6	5	4	3	2	1	Bit0
Read:	0	TOUTEN1	TOUTEN0	RTCTEN	TESL	TOUT2	TOUT1	TOUT0
Write:	X							
Reset:	0	0	0	0	0	0	0	0

RTCTEN: RTC second counter enable

RTCTEN=0: Second counter disabled

RTCTEN=1: Second counter enabled, overflow will produce the SECCNT interrupt

TESL: RTC timer 1/2 clock select

TRSL=0: timer 1 interrupt is choosed as 0.5s; timer 2 interrupt is choosed as 0.25s.

TRSL=1: timer 1 interrupt is choosed as 0.125s; timer 2 interrupt is choosed as 0.0625s.

TOUTEN[1:0]:

When TOUTEN[1:0] =00, the TOUT outputs the logic 0; =01, the TOUT outputs the logic 1;

When TOUTEN[1:0] =10 or 11, see the TOUT[2:0].

TOUT[2:0]:

Select the output frequency of the TOUT pin

TOUT2	TOUT1	TOUT0	TOUT	TOUT2	TOUT1	TOUT0	TOUT
0	0	0	1Hz	1	0	0	32Hz
0	0	1	2Hz	1	0	1	128Hz
0	1	0	4Hz	1	1	0	1024Hz
0	1	1	8Hz	1	1	1	32.768KHz

Table 12-4 RTC Calibration Register (write-protect)

RTC Calibration Register (RTCCAL)			Address: F2H					
	Bit7	6	5	4	3	2	1	Bit0
Read: / Write:	CAL7	CAL6	CAL5	CAL4	CAL3	CAL2	CAL1	CAL0
Reset:	0	0	0	0	0	0	0	0

Table 12-5 RTC Interrupt Enable Register

RTC Interrupt Enable Register (RTCIE)			Address: AAH					
	Bit7	6	5	4	3	2	1	Bit0
Read: / Write:	ALMIE	SCNTIE	RTC2IE	RTC1IE	DAYIE	HRIE	MINIE	SECIE
Reset:	0	0	0	0	0	0	0	0

1: enabled to generate interrupt

0: not disenabled to generate interrupt

Table 12-6 RTC Interrupt Flag Register

RTC Interrupt Flag register (RTCIF)			Address: B2H					
	Bit7	6	5	4	3	2	1	Bit0
Read:	ALMF	SCNTF	RTC2F	RTC1F	DAYF	HRF	MINF	SECF
Write:	x	X	x	x	x	X	x	x
Reset:	0	0	0	0	0	0	0	0

Table 12-7 RTC Second Counter Overflow Register

Second Counter Register (SECCNT)			Address: F3H					
	Bit7	6	5	4	3	2	1	Bit0
Read:	0	0	SCNT5	SCNT4	SCNT3	SCNT2	SCNT1	SCNT0
Write:	x	X						
Reset:	0	0	u	u	u	U	u	u

Table 12-8 Alarm Minute Register

Alarm Minute Register (ALMR)			Address: F4H					
	Bit7	6	5	4	3	2	1	Bit0
Read:	0	0	AM5	AM4	AM3	AM2	AM1	AM0
Write:	x	X						
Reset:	0	0	u	u	u	U	u	u

Range: 0-59. Writing a value other than 0 to 59 to this register has no effect.

Table 12-9 Alarm Hour Register

Alarm Hour Register (ALHR)			Address: F5H					
	Bit7	6	5	4	3	2	1	Bit0
Read:	0	0	0	AH4	AH3	AH2	AH1	AH0

Write:	x	X	x					
Reset:	0	0	0	u	u	U	u	u

Range: 0-23. Writing a value other than 0 to 23 to this register has no effect.

Table 12-10 RTC Second Register (write-protect)

Second Register (SECR)			**Address:**	**F9H**				
	Bit7	**6**	**5**	**4**	**3**	**2**	**1**	**Bit0**
Read:	0	0	SEC5	SEC4	SEC3	SEC2	SEC1	SEC0
Write:	x	X						
Reset:	0	0	u	u	u	U	u	u

Range: 0-59. Writing a value other than 0 to 59 to this register has no effect.

Tale 12-11 RTC Minute Register (write-protect)

Minute Register (MINR)			**Address:**	**FAH**				
	Bit7	**6**	**5**	**4**	**3**	**2**	**1**	**Bit0**
Read:	0	0	MIN5	MIN4	MIN3	MIN2	MIN1	MIN0
Write:	x	X						
Reset:	0	0	u	u	U	U	u	U

Range: 0-59. Writing a value other than 0 to 59 to this register has no effect.

Table 12-12 RTC Hour Register (write-protect)

Hour Register (HRR)			**Address:**	**FBH**				
	Bit7	**6**	**5**	**4**	**3**	**2**	**1**	**Bit0**
Read:	0	0	0	HR4	HR3	HR2	HR1	HR0
Write:	x	X	x					
Reset:	0	0	0	u	u	U	u	U

Range: 0-23. Writing a value other than 0 to 23 to this register has no effect.

Table 12-13 RTC Day Register (write-protect)

Day Register (DAYR)			**Address:**	**FCH**				
	Bit7	**6**	**5**	**4**	**3**	**2**	**1**	**Bit0**
Read:	0	0	0	DAY4	DAY3	DAY2	DAY1	DAY0
Write:	X	X	x					
Reset:	0	0	0	u	u	U	u	u

Range: 1-28/29/30/31. Writing a value that is not valid for the month and year to this register has no effect.

Table 12-14 RTC Month Register (write-protect)

Month Register (MTHR)			**Address:**	**FDH**				
	Bit7	**6**	**5**	**4**	**3**	**2**	**1**	**Bit0**
Read:	0	0	0	0	MTH3	MTH2	MTH1	MTH0
Write:	x	X	x	x				
Reset:	0	0	0	0	u	U	u	u

Range: 0-12. Writing a value other than 0 to 12 has no effect.

Table 12-15 RTC Year Register (write-protect)

Year Register (YRR)			**Address:**	**FEH**				
	Bit7	**6**	**5**	**4**	**3**	**2**	**1**	**Bit0**
Read:	0	YR6	YR5	YR4	YR3	YR2	YR1	YR0
Write:	X							
Reset:	0	U	U	u	u	U	u	u

Valid range: 0-99. The largest data is 127. Writing a value other than 0 to 127 has no effect.

Table 12-16 RTC Week Register (write-protect)

Day-Of-Week Register (DOWR)			**Address:**	**FFH**				
	Bit7	**6**	**5**	**4**	**3**	**2**	**1**	**Bit0**

Read:	0	0	0	0	0	DOW2	DOW1	DOW0
Write:	x	X	x	x	X			
Reset:	0	0	0	0	0	U	u	u

Range: 0-6. Writing a value other than 0 to 6 to this register has no effect.

Table 12-17 RTC Write-protect register

Bit Write Protect Register (BWPR)			**Address:**	**9AH**				
	Bit7	**6**	**5**	**4**	**3**	**2**	**1**	**Bit0**
Read:	PASS4	PASS3	PASS2	PASS1	PASS0	BITPS	PMOD1	PMOD0
Write:						x		
Reset:	0	0	0	0	0	0	0	0

When PMOD[1:0]=11,PASS[4:0]=10011 can enable the writing function of all protected bits, and these bits can be modified by software. When PASS[4:0]=10101, the writing function of all protected bits will be disabled, and These bits can not be modified by software.

It will be disabled automatically after 128 fsys clock cycle if no writing on PASS[4:0] to disable the function, and the BWPR will be reset to 00H.

BITPS shows the current write-enable state. If enabled, BITPS=1, or else BITPS=0.

PMOD[1:0] can not be modified directly. Only when PASS[4:0]=11000, the PMOD[1:0] bits can be modified.

RTC Registers protected list: RTCCAL, SECR, MINR, HRR, DAYR, MTHR, YRR, DOWR.

PMOD[1:0]:bit-protect mode select

PMOD[1:0]=11: Can modify the bit-protect state

PMOD[1:0]=00/01/10: Can not modify the bit-protect state

BITPS:bit-protect state flag

BITPS=1: Software can modify all protected bits

BITPS=0: Software can not modify all protected bits

PASS[4:0]:bit-protect password

PASS[4:0]=11000: writing PMOD[1:0] enabled

PASS[4:0]=10011: writing all protected bits enabled

PASS[4:0]=10001: writing all RTC protected registers enabled

PASS[4:0]=10101: writing all protected registers and bits disabled

12.3 Low-Power Modes

RTC module is always active in all operating modes.

12.4 I/O Signal

The RTC has Real Clock Calibration output pin TOUT, shared with PWM. It can be used to test the clock signal of before Calibration and after Calibration .

13 LCD Driver

13.1 Introduction

The LCD (liquid crystal display) driver module can drive a maximum of 41 Segments and 4 Commons, features include the following:

- Software programmable driver segment configurations
  - 40 Segments * 4 Commons (160)
  - 41 Segments * 3 Commons (123)
  - 41 Segments * 1 Commons (41)
- Adjustable LCD drive voltage
- 1/3 Bias
- Static、1/3、1/4 Duty

13.2 Function

The LCD driver module uses a 1/3 biasing method. The LCD power is supplied by the VLCD pin. Voltages VLCD1, VLCD2, and VLCD3 are generated by an internal resistor ladder.

The LCD data registers, LBUF0-LBUF41（table 13-12）, control the LCD segments' ON/OFF. When a logic 1 is written to a SxCy bit, the corresponding SEGx and COMy segment will turn ON. When a logic 0 is written, the segment will turn OFF.

When the LCD driver module is disabled (PDLCD(0xBFH.2, table 13-7)), the LCD display will be OFF, all SEG and COM drivers have the same potential as VCC. The resistor ladder and analog circuit is turned off and the LCD clock is stopped.

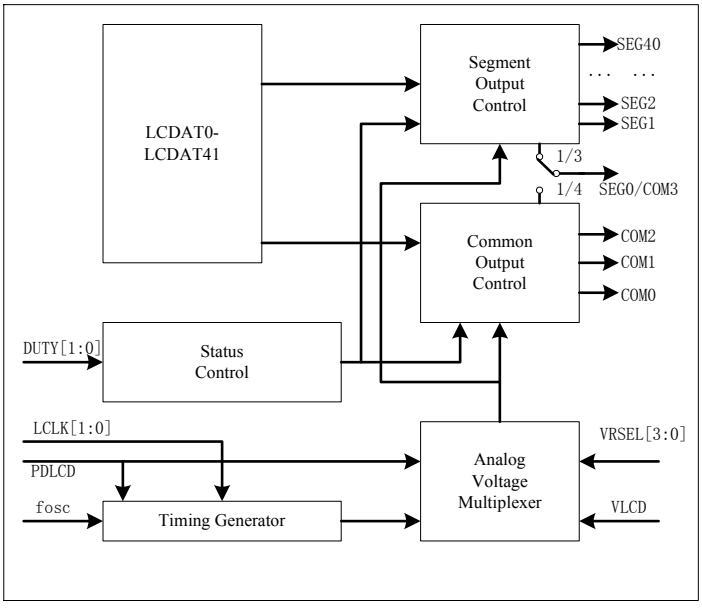


Figure 13-1 LCD Block Diagram

13.2.1 Pin Name Conventions

Table 13-1 LCD **Pin Name Conventions**

LCD pin name	Function pin name	Chip pin name
COM0-COM2	--	COM0 - COM2
COM3/SEG0	--	COM3/SEG0
SEG1-SEG8	PA0-PA7	SEG1/PA0 - SEG8/PA7
SEG9-SEG16	PB0-PB7	SEG9/PB0 - SEG16/PB7
SEG17-SEG24	PC0-PC7	SEG17/PC0 - SEG24/PC7
SEG25-SEG32	PD0-PD7	SEG25/PD0 - SEG32/PD7
SEG33-SEG40	P0.0-P0.7	SEG33/P0.0 - SEG40/P0.7

The LCD pins are shared with I/O pins, and can be configured by LCDCFG (0xB9H, table 13-13)/ P02CFG (0xBAH, table 13-14) register.

13.2.2 LCD Drive Voltage

The voltage VLCD is connected to VLCD pin and must not exceed VCC. VLCD1, VLCD2, and VLCD3 are internal bias voltages for the LCD driver waveforms.

- VLCD=VCC
- VLCD1=2/3*(VLCD-Vbias)
- VLCD2=1/3*(VLCD-Vbias)
- VLCD3=Vbias

The VLCD3 bias voltage, Vbias, is controlled by the LCD contrast control bits, VRSEL[3:0](0xC3H[3:0], table 13-9).

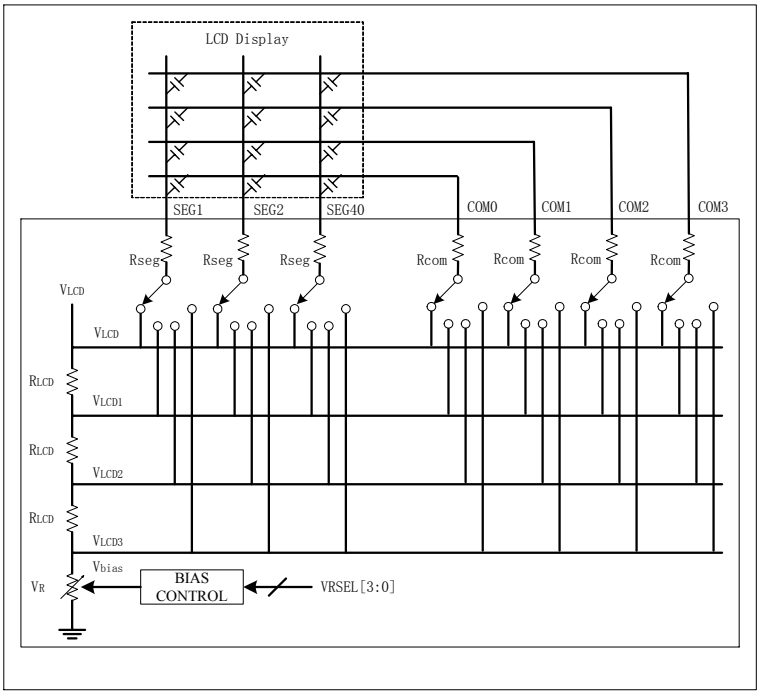


Figure 13-2 **LCD drive Schematic (1/4 Duty, 1/3 Bias)**

13.2.3 LCD DUTY

The setting of the LCD output waveform duty is dependent on the number of COMMON drivers required. Three LCD duties are available:

- DUTY[1:0](0xC2H.[4:3], table 13-8)=00: Static---COM0 is used only

- DUTY[1:0]=01: 1/3 duty---COM0、COM1、COM2 are used.
- DUTY[1:0]=1x: 1/4 duty---COM0、COM1、COM2、COM3 are used.

1．Static Duty output waveform

COM1/2/3 are not used. 1FRAME is equal to the cycle of LCD waveform base clock.

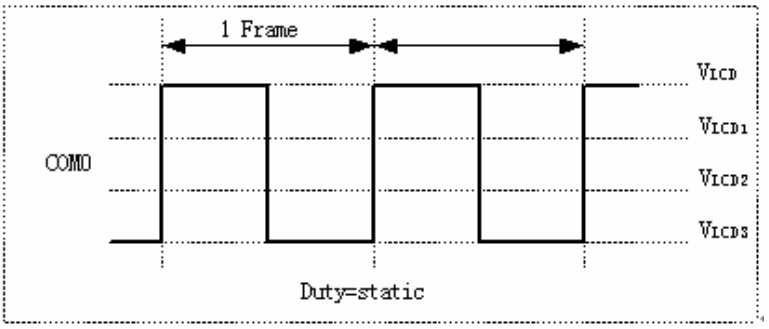
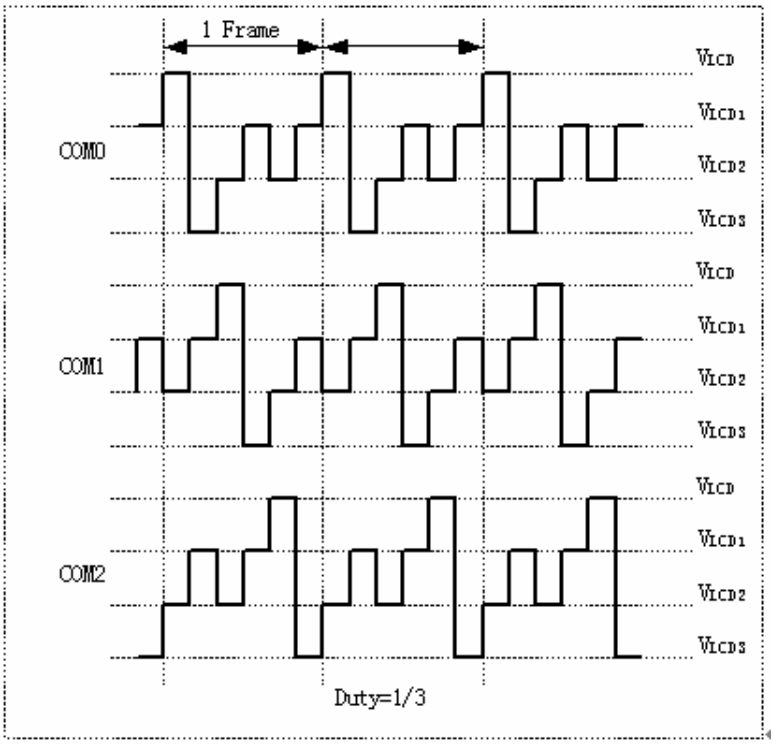


Figure13-3 LCD Static Duty output waveform

2．1/3 Duty output waveform

COM3 is not used. 1FRAME is equal to 3 cycles of LCD waveform base clock.



Tigure 13-4 LCD 1/3 Duty output waveform

3．1/4 Duty output waveform

COM0/1/2/3 is used. 1FRAME is equal to 4 cycles of LCD waveform base clock

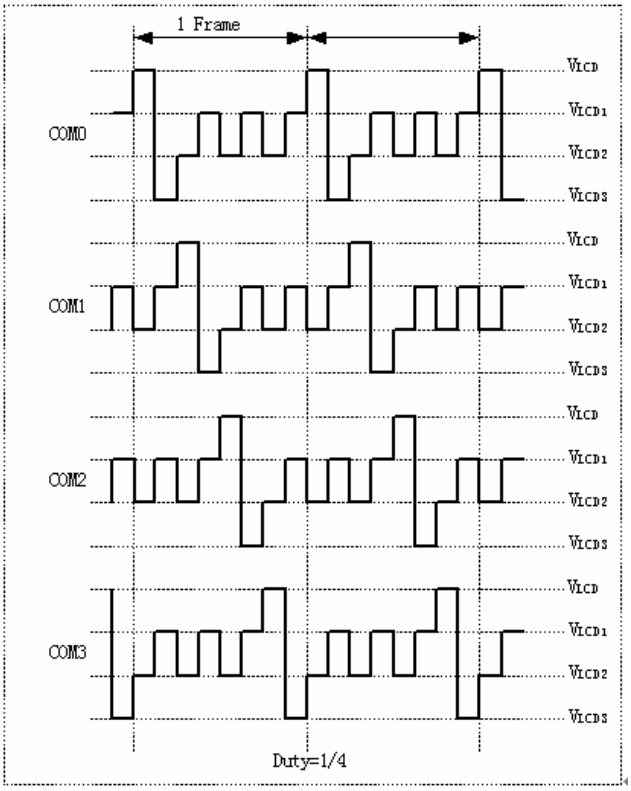


Figure 13-5 LCD 1/4 Duty output waveform

13.2.4 LCD Waveform Base Clock Selection

The LCD driver module use the fosc as the reference clock. This clock is divided to produce the LCD waveform base clock, flcd, by configuring the register bits LCLK(0xC2H[1:0], table 13-8).

Table 13-2 LCD waveform base clock and fram frequency

LCLK		Divide Ratio	flcd (Hz)	ffrm (Hz)		
LCLK1	LCLK0			Static	1/3	1/4
0	0	128	256	256	85.3	64
0	1	256	128	128	42.7	32
1	0	512	64	64	21.3	16
1	1	1024	32	32	10.7	8

LCD frame frequency, ffrm=flcd*duty.

For example: when 1/3 duty,ffrm=flcd/3.

13.2.5 LCD Contrast Control

The contrast of the connected LCD panel can be adjusted by configuring the VRSEL[3:0] bits in the LCD control register. The VRSEL[3:0] bits provide a 16-step contrast control, which adjusts the bias voltage in the resistor ladder for LCD voltage, VLCD3. The relative voltages, VLCD1 and VLCD2, are altered accordingly.

Setting VRSEL[3:0](0xC3H[3:0], table 13-9)=0000 chooses the maximum Contrast; Setting VRSEL[3:0]=1111 chooses the minmum Contrast.

Table 13-3 LCD Contrast

VRSEL3	VRSEL2	VRSEL1	VRSEL0	Bias Volatge (% of VLCD)
0	0	0	0	0.6

0	0	0	1	2.9
0	0	1	0	5.2
0	0	1	1	7.4
0	1	0	0	9.6
0	1	0	1	11.6
0	1	1	0	13.5
0	1	1	1	15.3
1	0	0	0	17.2
1	0	0	1	18.8
1	0	1	0	20.5
1	0	1	1	22.0
1	1	0	0	23.6
1	1	0	1	25.0
1	1	1	0	26.4
1	1	1	1	27.7

13.2.6 LCD Fast Charge and Low Current

The default value for each of the bias resistors, RLCD, in the resistor ladder is approximately 37kΩ at VLCD = 3V. Lowering this current is possible by setting the LC(0xC3H.4, table 13-9) bit in the LCD control register, switching the RLCD value to 146kΩ.

Setting the FC(0xC3H.5, table 13-9) bit in the LCD control register selects the fast charge mode. The RLCD value is set to 37kΩ (for high current) for a fraction of time for each LCD waveform switching edge, and then back to 146kΩ for the steady state period. The duration of the fast charge time is set by configuring the FCSET[1:0] (0xC2H.[6:5], table 13-8) bits in the LCD clock register.

Table 13-4 Resistor Ladder Selection

FC	LC	Action
X	0	RLCD=37KΩ
0	1	RLCD=146KΩ
1	1	Fast charge mode

Table 13-5 Fast Charge Duty Cycle Selection

FCSET1	FCSET0	Fast charge duty cycle
0	0	In each flcd/2 period, each bias resistor is reduced to 37 KΩ for a duration of flcd/32
0	1	In each flcd/2 period, each bias resistor is reduced to 37 KΩ for a duration of flcd/64
1	0	In each flcd/2 period, each bias resistor is reduced to 37 KΩ for a duration of flcd/128
1	1	Not used

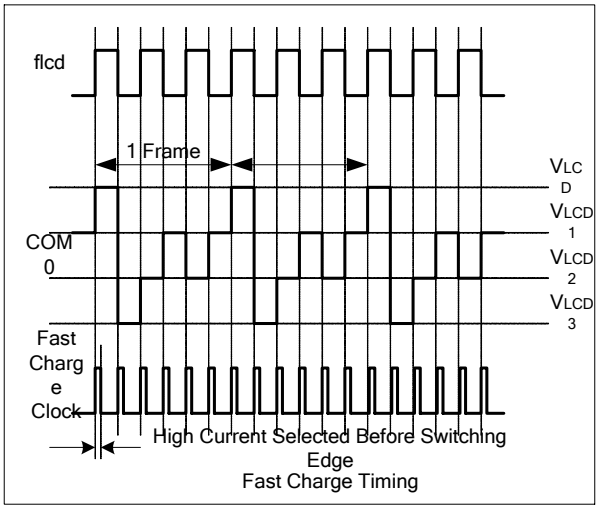


Figure 13-6 Fast Charge Timing

13.2.7 SEGMENT Output Waveform

1．Static Duty

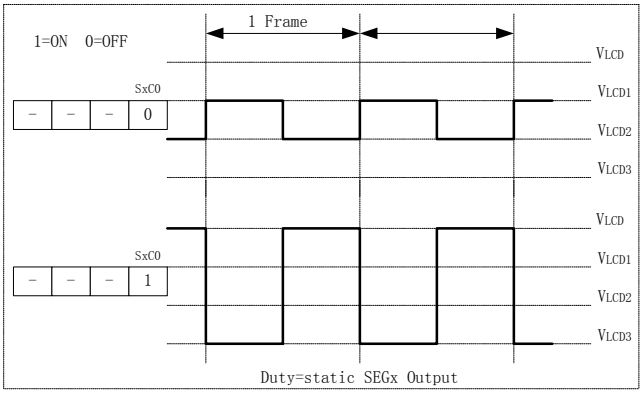


Figure 13-7 Static SEGMENT output waveform

2． 1/3 Duty

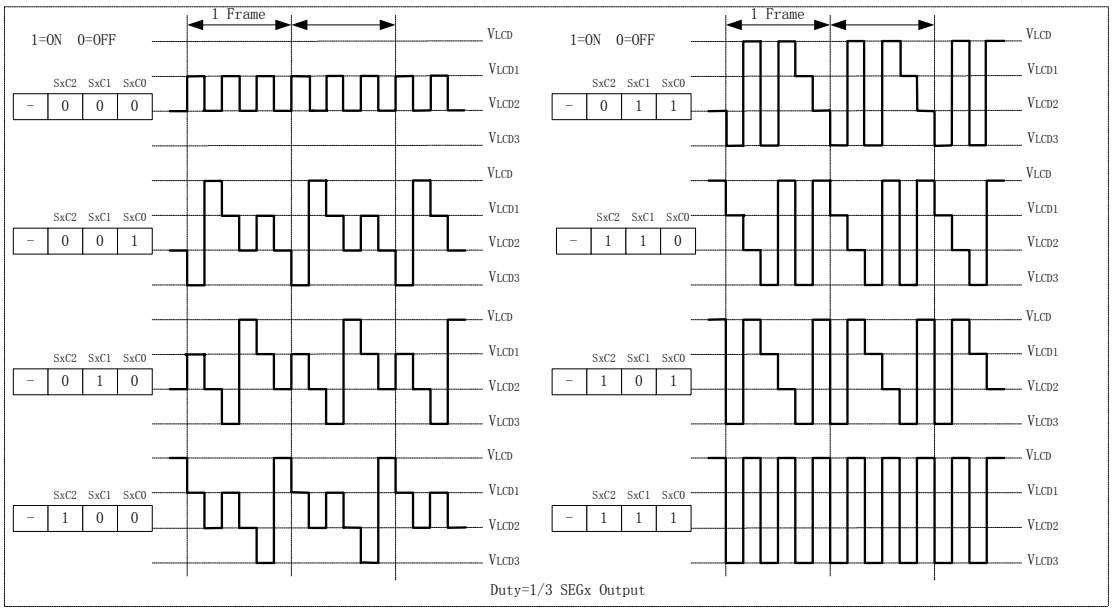
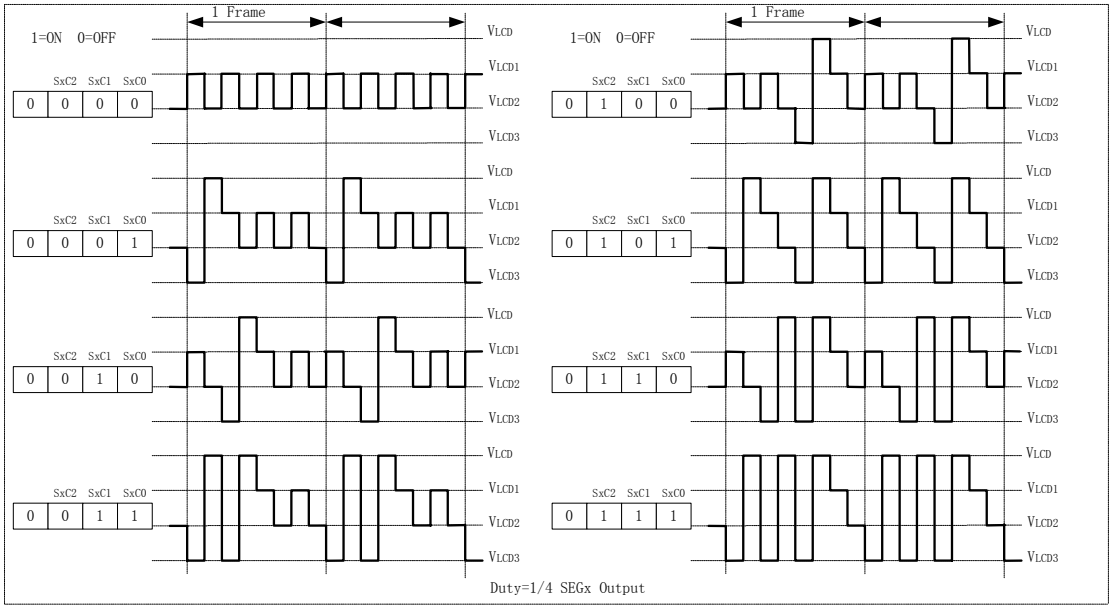


Figure 13-8 1/3 Duty SEGMENT output waveform

3． 1/4 Duty



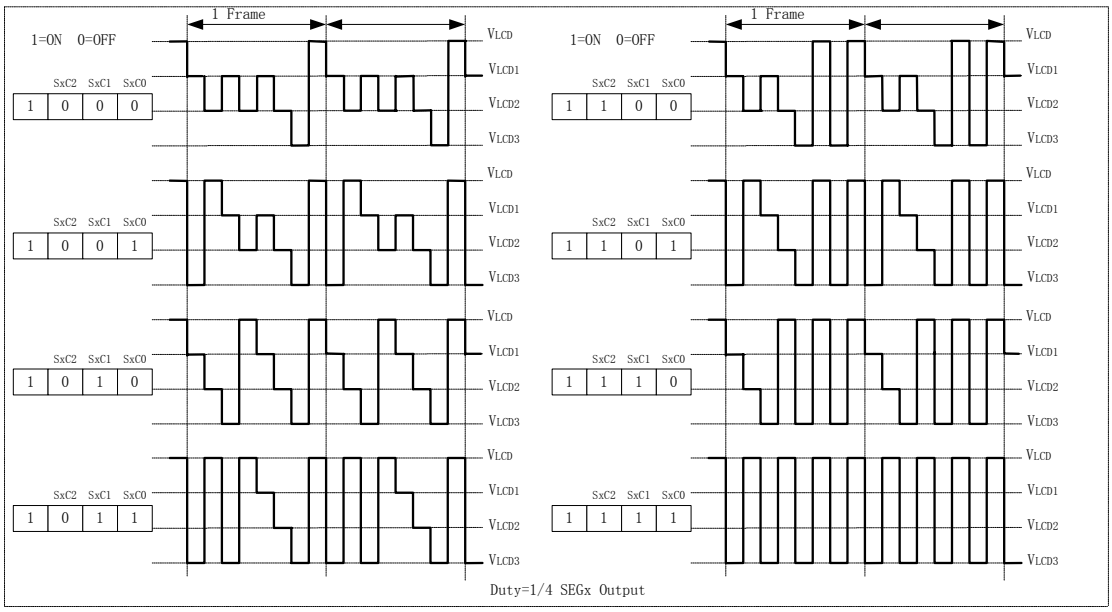


Figure 13-9 1/4 Duty SEGMENT output waveform

13.3 Registers

Table 13-6 LCD registers list

Address(EPADR)	Name	Byte length	Function
BFH	PDLCD	1	PDLCD control bit--see **table 13-7**,write-protect
C2H	LCDCLK	1	LCD clock register--see **table 13-8**
C3H	LCDCR	1	LCD control register--see **table 13-9**
C4H	LADR	1	LCD address register-- see **table 13-10**
C5H	LDAT	1	LCD data register--see **table 13-11**
00H-28H	LBUFx	1*41	LCD buffer data register--see **table 13-12**
B9H	LCDCFG	1	LCD port configure register--see **table 13-13 write-protect**
BAH	P02CFG	1	P0&P2 port configure register--see **table 13-14 write-protect.**

LCD Registers

Table 13-7 PDLCD control bit (SUPDC 0xBFH)

System Unit Power-Down Control Register (SUPDC)			**Address:** **BFH**					
	Bit7	**6**	**5**	**4**	**3**	**2**	**1**	**Bit0**
Read:	0	PDTPS	PDEMU	PDBOR	PDLVD	PDLCD	PDI2C	PDSPI
Write:	x							
Reset:	0	0	1	0	0	1	1	1

PDLCD: LCD enable control bit.

When write-protect off, 0=LCD driver module enabled; 1=LCD driver module disenabled.

Table 13-8 LCD Clock Register (LCDCLK 0xC2H)

LCD Clock Register (LCDCLK)			**Address:** **C2H**					
	Bit7	**6**	**5**	**4**	**3**	**2**	**1**	**Bit0**
Read:	0	FCSET1	FCSET0	DUTY1	DUTY0	0	LCLK1	LCLK0
Write:	x					x		

Reset:	0	0	0	1	0	0	0	0

FCSET[1:0]---Fast Charge Duty Cycle Select

DUTY[1:0]---Duty Cycle Select

LCLK[1:0]---LCD Waveform Base Clock Select

Table 13-9 LCD Control Register (LCDCR 0xC3H)

LCD Control Register (LCDCR)			Address: C3H					
	Bit7	6	5	4	3	2	1	Bit0
Read:	0	0	FC	LC	VRSEL 3	VRSEL 2	VRSEL 1	VRSEL 0
Write:	X	x						
Reset:	0	0	0	0	0	0	0	0

FC---Fast Charge Duty Cycle Select

LC---Low Current Select

VRSEL[3:0]---LCD Contrast Control

Table 13-10 LCD Address Register (LADR 0xC4H)

LCD Address Register (LADR)			Address: C4H					
	Bit7	6	5	4	3	2	1	Bit0
Read:	0	0	LADR5	LADR4	LADR3	LADR2	LADR1	LADR0
Write:	x	x						
Reset:	0	0	0	0	0	0	0	0

Writing LADR register saves the LBUFx(x=LADR[5:0]) data to the LADT register according to the index content of the LADR[5:0].

Table 13-11 LCD Data Register (LDAT 0xC5H)

LCD Data Register (LDAT)			Address: C5H					
	Bit7	6	5	4	3	2	1	Bit0
Read:	LDAT7	LDAT6	LDAT5	LDAT4	LDAT3	LDAT2	LDAT1	LDAT0
Write:								
Reset:	0	0	0	0	0	0	0	0

Writing LDAT register saves the LDAT data to the LBUFx (x==LADR[5:0]) according to the index content of the LADR[5:0].

Table 13-12 LCD Buffer Data Register (LBUFx 00H~28H)

LCD Buffer Data Register (LBUFx)			Address: 00H-28H					
	Bit7	6	5	4	3	2	1	Bit0
Read:	0	0	0	0	SxC3	SxC2	SxC1	SxC0
Write:	x	x	x	x				
Reset:	0	0	0	0	u	u	u	u

LCD buffer data register.

Table 13-13 LCD Port Configure Rigster (LCDCFG B9H)

LCDCFG			Address: B9H					
	Bit7	6	5	4	3	2	1	Bit0
Read:	PDH	PDL	PTCH	PTCL	PTBH	PTBL	PTAH	PTAL
Write:								
Reset:	0	0	0	0	0	0	0	0

Write-protect, when write-protect off it will be configured as:

PTAL=0:	SEG1/PA0－SEG4/PA3	GPIO:	PA0-PA3
PTAL=1:	SEG1/PA0－SEG4/PA3	LCD output:	SEG1-SEG4
PTAH=0:	SEG5/PA4－SEG8/PA7	GPIO:	PA4-PA7
PTAH=1:	SEG5/PA4－SEG8/PA7	LCD output:	SEG5-SEG8
PTBL=0:	SEG9/PB0－SEG12/PB3	GPIO:	PB0-PB3

PTBL=1:	SEG9/PB0－SEG12/PB3	LCD output:	SEG9-SEG12
PTBH=0:	SEG13/PB4－SEG16/PB7	GPIO:	PB4-PB7
PTBH=1:	SEG13/PB4－SEG16/PB7	LCD output:	SEG13-SEG16
PTCL=0:	SEG17/PC0－SEG20/PC3	GPIO:	PC0-PC3
PTCL=1:	SEG17/PC0－SEG20/PC3	LCD output	SEG17-SEG20
PTCH=0:	SEG21/PC4－SEG24/PC7	GPIO:	PC4-PC7
PTCH=1:	SEG21/PC4－SEG24/PC7	LCD output:	SEG21-SEG24
PTDL=0:	SEG25/PD0－SEG28/PD3	GPIO:	PD0-PD3
PTDL=1:	SEG25/PD0－SEG28/PD3	LCD output:	SEG25-SEG28
PTDH=0:	SEG29/PD4－SEG32/PD7	GPIO:	PD4-PD7
PTDH=1:	SEG29/PD4－SEG32/PD7	LCD output:	SEG29-SEG32

Table 13-14 P0&P2 Port Configure Register (P02CFG 0xBAH)

P02CFG			Address: BAH					
	Bit7	6	5	4	3	2	1	Bit0
Read: Write:	P267	P245	P223	P201	P067	P045	P023	P001
Reset:	0	0	0	0	0	0	0	0

This register is write-protected, when open it will be configured as:

P001=0:	SEG33/P0.0－SEG34/P0.1	GPIO:	P0.0-P0.1
P001=1:	SEG33/P0.0－SEG34/P0.1	LCD output:	SEG33-SEG34
P023=0:	SEG35/P0.2－SEG36/P0.3	GPIO:	P0.2-P0.3
P023=1:	SEG35/P0.2－SEG36/P0.3	LCD output:	SEG35-SEG36
P045=0:	SEG37/P0.4－SEG38/P0.5	GPIO:	P0.4-P0.5
P045=1:	SEG37/P0.4－SEG38/P0.5	LCD output:	SEG37-SEG38
P067=0:	SEG39/P0.6－SEG40/P0.7	GPIO:	P0.6-P0.7
P067=1:	SEG39/P0.6－SEG40/P0.7	LCD output:	SEG39-SEG40
P201=0:	TX1/P2.0－RX1/P2.1	UART1:	TX1-RX1
P201=1:	TX1/P2.0－RX1/P2.1	GPIO:	P2.0-P2.1
P223=0:	TX0/P2.2－RX0/P2.3	UART0:	TX0-RX0
P223=1:	TX0/P2.2－RX0/P2.3	GPIO:	P2.2-P2.3
P245=0:	LVDIN/P2.4－SF/P2.5	Pulse output:	LVDIN-SF
P245=1:	LVDIN/P2.4－SF/P2.5	GPIO:	P2.4-P2.5
P267=0:	PF/P2.6－QF/P2.7	Pulse putput:	PF-QF
P267=1:	PF/P2.6－QF/P2.7	GPIO:	P2.6-P2.7

13.4 Low-Power Modes

PSM mode:

The LCD driver module continues normal operation in PSM mode. If the LCD is not required in PSM mode, power down the LCD module by setting the LCD enable register bit PDLCD.

PDM mode:

If PDLCD=0 and LCD pins configured as LCD function before entering PDM mode, then the LCD module continues normal operation, but the data will not be refreshed; If the PDLCD=1

before entering PDM mode, then the LCD module will be powered-down.

14 Temperature Sensor

14.1 Function

The ATT7025 includes an on-chip temperature sensor(TPS) and the temperature data is saved in the register TEMPDR (0xC9H），

14.1.1 Temperature Formula

The temperature conversion formula is:

Tr=Toff-Tdata*0.625

Tr is the actual temperature (the display of temperature)

Toff is a fixed offset, so the offset of each chip need calibration separately.

Tdata is transformed from TEMPDR (0xC9H):

TEMPDR.7=0, Tdata=TEMPDR[6:0]

TEMPDR.7=1, Tdata= - (~TEMPDR[6:0]) (**Bit-wise negation operator**)

14.1.2 Temperature Offset Correction

Before the computation of temperature, Toff must be computated.

Toff=Tr +Tdata*0.625

Get the environment temperature Tr in Thermostat and Tdata in register TEMPDR, then the Toff can be computated.

14.1.3 Example of Temperature Calculattion

First step, calculate the Toff, supposed that the envirment temperature is 25℃, and TEMPDR value is 10H,then

Toff＝25 + 16*0.625＝35

Save Toff value to flash or other nonvolatile memory.

Second step, get the display temperatureTr according to the value of regiater TEMPDR.

Tr(display）	Toff	TEMPDR	Tdata
25	35	10H	16
35	35	0	0
-44	35	7FH	127
114	35	80H	-127
44	35	F0H	-15

14.2 Registers

Table 14-1 Temperature Sensor Data Register (TEMPDR 0xC9H)

Temperature Sensor Data register (TEMPDR)			**Address:**	**C9H**				
	Bit7	**6**	**5**	**4**	**3**	**2**	**1**	**Bit0**
Read:	TPDR7	TPDR6	TPDR5	TPDR4	TPDR3	TPDR2	TPDR1	TPDR0
Write:	x	x	x	x	x	x	x	x
Reset:	0	0	0	0	0	0	0	0

Table 14-2 PDTPS control bit (SUPDC 0xBFH)

System Unit Power-Down Control Register (SUPDC)			**Address:**	**BFH**				
	Bit7	**6**	**5**	**4**	**3**	**2**	**1**	**Bit0**
Read:	0	PDTPS	PDEMU	PDBOR	PDLVD	PDLCD	PDI2C	PDSPI
Write:	x							

Reset:	0	0	1	0	0	1	1	1

PDTPS: TPS enable control bit.

When write-protect off, 0= temperature sensor enabled; 1= temperature sensor disenabled

14.3 Low-Power Modes

The temperature sensor module can work in all modes. Users can turn on or off the module according to demands.

15 UART

15.1 Introduction

The ATT7025 provides two serial ports : UART0 and UART1, features as follows:

- UART0 and UART1 reserve all functions of the two interfaces of the standard 8052 except Mode0
- The UART1 exports the TX1 to support the a 38 KHz infrared modulation
- In application, UART0 generally acts as modulation interface and RS485 communication interface while UART1 is a 38 KHz infrared interface
- Two serial interfaces inputs RX0/RX1s can also be configured as the inputs of /INT0 and /INT1 in order to wake up under PDM.

Fig 15-1 is the function frame of the UART0 and UART1

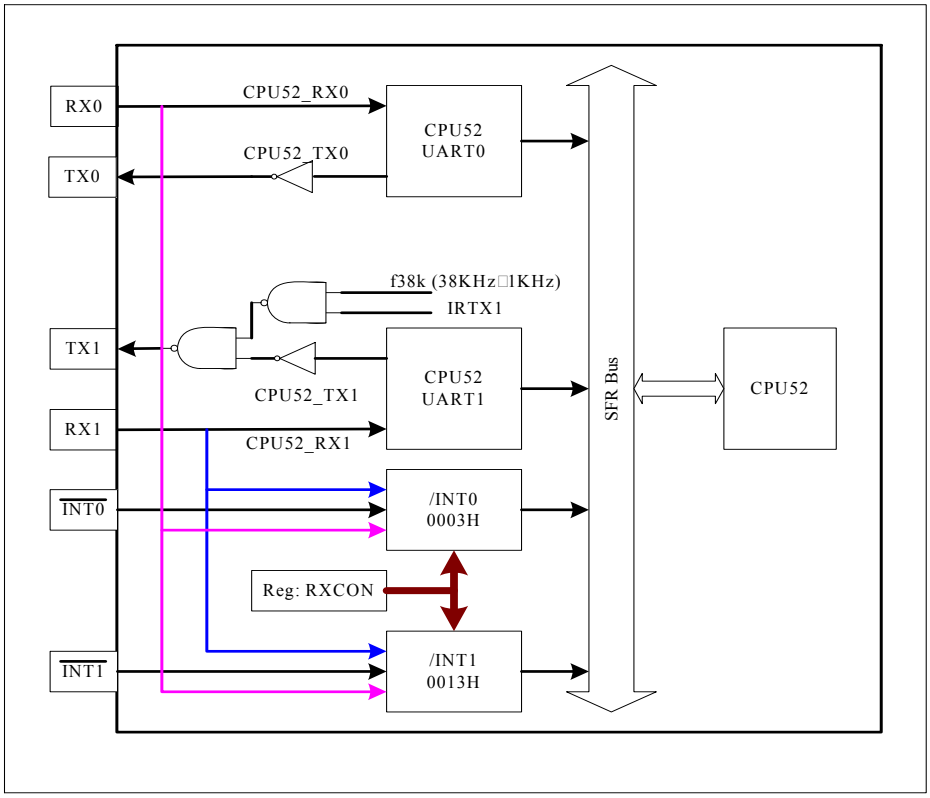


Fig 15-1 Function frame of UART0 and UART1

15.2 Function Description

15.2.1 Mode 0

UART0 and UART1 do not support mode 0.

15.2.2 Mode 1

Mode 1 provides standard asynchronous, full-duplex communication, using a total of 10 bits: 1 start bit, 8 data bits, and 1 stop bit. For receiving operations, the stop bit is stored in RB8_0 (or RB8_1). Data bits are received and transmitted LSB first.

15.2.2.1 Mode 1 Baud Rate

The mode 1 baud rate is a function of timer overflow. Serial Port 0 can use either Timer 1 or Timer 2 to generate baud rates. Serial Port 1 can only use Timer 1. The two serial ports can run at the same baud rate if they both use Timer 1, or different baud rates if Serial Port 0 uses Timer 2 and Serial Port 1 uses Timer 1.

Each time the timer increments from its maximum count (FFh for Timer 1 or FFFFh for Timer 2), a clock is sent to the baud rate circuit. The clock is then divided by 16 to generate the baud rate. When using Timer 1, the SMOD0 (or SMOD1) bit selects whether or not to divide the Timer 1 rollover rate by 2. Therefore, when using Timer 1, the baud rate is determined by the equation:

$$\text{Baud rate}=\frac{2^{SMODx}}{32}\times\text{Timer1 overflow}$$

SMOD0 is SFR bit PCON.7; SMOD1 is SFR bit EICON.7.

When using Timer 2, the baud rate is determined by the equation:

Baud rate=Timer2 overflow value/16

To use Timer 1 as the baud rate generator, it is best to use Timer 1 mode 2 (8-bit counter with auto-reload), although any counter mode can be used. The Timer 1 reload value is stored in the TH1 register, which makes the complete formula for Timer 1:

$$\text{Baud rate}=\frac{2^{SMODx}}{32}\times\frac{fsys}{12\times(256-TH1)}$$

The 12 in the denominator in the above equation can be changed to 4 by setting the T1M bit in the CKCON SFR. To derive the required TH1 value from a known baud rate (when TM1 = 0), use the equation:

$$\text{TH1}=256-\frac{2^{SMODx}\times fsys}{384\times Baud-rate\quad value}$$

You can also achieve very low serial port baud rates from Timer 1 by enabling the Timer 1 interrupt, configuring Timer 1 to mode 1.

Table 15-1 Timer 1 Reload Values for Common Serial Port Mode 1 Baud Rates

Desired Baud Rate	SMODx	C/$\overline{T}$	Timer1 Mode	**TH1 Value for 11.0592-MHz clk**
57.6Kb/s	1	0	2	0xFFH
19.2 Kb/s	1	0	2	0xFDH
9.6 Kb/s	1	0	2	0xFAH
4.8 Kb/s	1	0	2	0xF4H
2.4 Kb/s	1	0	2	0xE8H
1.2 Kb/s	1	0	2	0xD0H

To use Timer 2 as the baud rate generator, configure Timer 2 in auto-reload mode and set the TCLK and/or RCLK bits in the T2CON SFR. TCLK selects Timer 2 as the baud rate generator for the transmitter; RCLK selects Timer 2 as the baud rate generator for the receiver. The 16-bit reload value for Timer 2 is stored in the RCAP2L and RCA2H SFRs, which makes the equation for the

Timer 2 baudrate:

$$\text{Baud rate} = \frac{fsys}{32 \times (65536 - RCAP2H, RCAP2L)}$$

where RCAP2H,RCAP2L is the content of RCAP2H and RCAP2L taken as a 16-bit unsigned number. The 32 in the denominator is the result of the *clk* being divided by 2 and the Timer 2 overflow being divided by 16. Setting TCLK or RCLK to 1 automatically causes the *clk* to be divided by 2, as shown in Figure 3-6, instead of the 4 or 12 determined by the T2M bit in the CKCON SFR. To derive the required RCAP2H and RCAP2L values from a known baud rate, use the equation:

$$\text{RCAP2H,RCAP2L} = 65536 - \frac{fsys}{32 \times Baud - rate}$$

Table 15-2 lists sample values of RCAP2L and RCAP2H for a variety of desired baud rates.

Baud rate	C/$\overline{T}$	**11.0592-MHz clk RCAP2H**	**11.0592-MHz clk RCAP2L**
57.6Kb/s	0	0xFFH	0xFAH
19.2 Kb/s	0	0xFFH	0xEEH
9.6 Kb/s	0	0xFFH	0xDCH
4.8 Kb/s	0	0xFFH	0xB8H
2.4 Kb/s	0	0xFFH	0x70H
1.2 Kb/s	0	0xFEH	0xE0H

15.2.2.2 Mode 1 transmit

Figure 15-2 illustrates the mode 1 transmit timing. In mode 1, the UART begins transmitting after the first rollover of the divide-by-16 counter after the software writes to the SBUF0 (or SBUF1) register. The UART transmits data on the *txd0* (or *txd1*) pin in the following order: start bit, 8 data bits (LSB first), stop bit. The TI_0 (or TI_1) bit is set 2 *clk* cycles after the stop bit is transmitted.

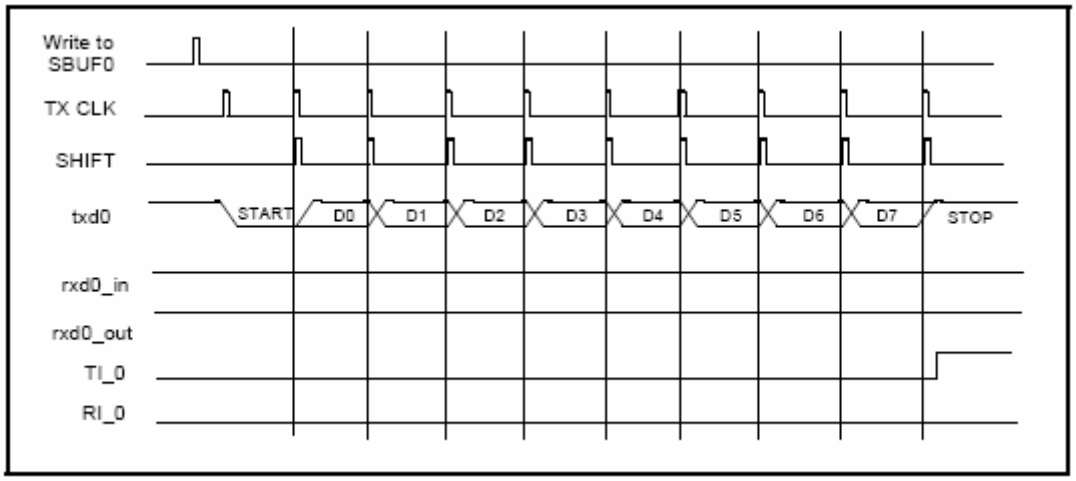


Fig 15-2 Mode 1 Transmit Timing

15.2.2.3 Mode 1 receive

Figure 15-3 illustrates the mode 1 receive timing. Reception begins at the falling edge of a start bit received on *rxd0_in* (or *rxd1_in*), when enabled by the REN_0 (or REN_1) bit. For this purpose, *rxd0_in* (or *rxd1_in*) is sampled 16 times per bit for any baud rate. When a falling edge of a start bit is detected, the divide-by-16 counter used to generate the receive clock is reset to align the counter rollover to the bit boundaries.

For noise rejection, the serial port establishes the content of each received bit by a majority decision of 3 consecutive samples in the middle of each bit time. This is especially true for the start bit. If the falling edge on *rxd0_in* (or *rxd1_in*) is not verified by a majority decision of 3 consecutive samples (low), then the serial port stops reception and waits for another falling edge on *rxd0_in* (or *rxd1_in*).

At the middle of the stop bit time, the serial port checks for the following conditions:

• RI_0 (or RI_1) = 0, and

• If SM2_0 (or SM2_1) = 1, the state of the stop bit is 1.

(If SM2_0 (or SM2_1) = 0, the state of the stop bit doesn't matter.)

If the above conditions are met, the serial port then writes the received byte to the SBUF0 (or SBUF1) register, loads the stop bit into RB8_0 (or RB8_1), and sets the RI_0 (or RI_1) bit. If the above conditions are not met, the received data is lost, the SBUF register and RB8 bit are not loaded, and the RI bit is not set.

After the middle of the stop bit time, the serial port waits for anotherhigh-to-low transition on the (*rxd0_in* or *rxd1_in*) pin.

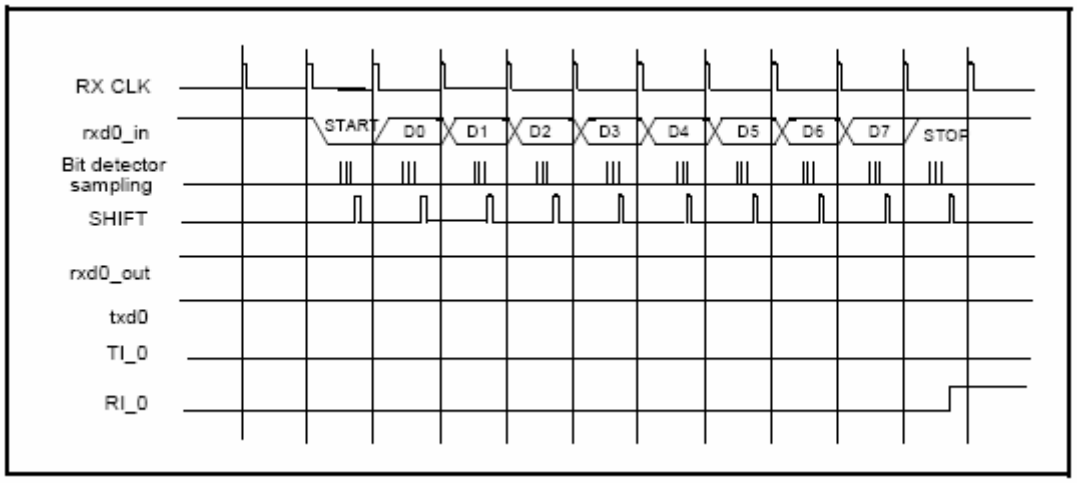


Fig 15-3 Mode 1 Receive Timing

15.2.3 Mode 2

Mode 2 provides asynchronous, full-duplex communication, using a total of 11 bits: 1 start bit, 8 data bits, a programmable 9th bit, and 1 stop bit. The data bits are transmitted and received LSB first. For transmission, the 9th bit is determined by the value in TB8_0 (or TB8_1). To use the 9th bit as a parity bit, move the value of the P bit (SFR PSW.0) to TB8_0 (or TB8_1).

The mode 2 baud rate is either *clk*/32 or *clk*/64, as determined by the

SMOD0 (or SMOD1) bit. The formula for the mode 2 baud rate is:

$$\text{Baud rate} = \frac{2^{SMODx} \times \text{fsys}}{64}$$

15.2.3.1 Mode 2 transmit

Figure 15-4 illustrates the mode 2 transmit timing. Transmission begins after the first rollover of the divide-by-16 counter following a software write to SBUF0 (or SBUF1). The UART shifts data out on the *txd0* (or *txd1*) pin in the following order: start bit, data bits (LSB first), 9th bit, stop bit. The TI_0 (or TI_1) bit is set when the stop bit is placed on the *txd0* (or *txd1*) pin.

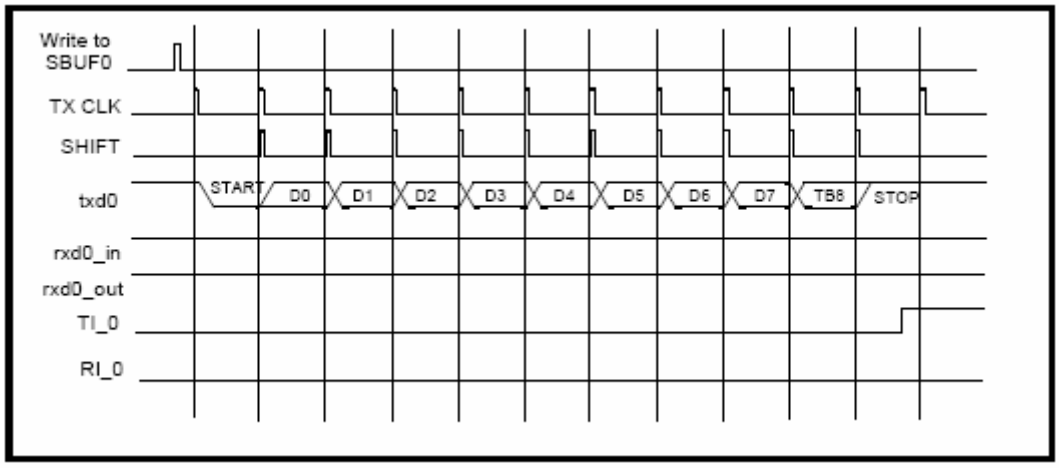


Fig 15-4 Mode 2 Transmit Timing

15.2.3.2 Mode 2 receive

Figure 15-5 illustrates the mode 2 receive timing. Reception begins at the falling edge of a start bit received on *rxd0_in* (or *rxd1_in*), when enabled by the REN_0 (or REN_1) bit. For this purpose, *rxd0_in* (or *rxd1_in*) is sampled 16 times per bit for any baud rate. When a falling edge of a start bit is detected, the divide-by-16 counter used to generate the receive clock is reset to align the counter rollover to the bit boundaries.

For noise rejection, the serial port establishes the content of each received bit by a majority decision of 3 consecutive samples in the middle of each bit time. This is especially true for the start bit. If the falling edge on *rxd0_in* (or *rxd1_in*) is not verified by a majority decision of 3 consecutive samples (low), then the serial port stops reception and waits for another falling edge on *rxd0_in* (or *rxd1_in*).

At the middle of the stop bit time, the serial port checks for the following conditions:

• RI_0 (or RI1) = 0, and

• If SM2_0 (or SM2_1) = 1, the state of the stop bit is 1.

(If SM2_0 (or SM2_1) = 0, the state of the stop bit doesn't matter.)

If the above conditions are met, the serial port then writes the received byte to the SBUF0 (or SBUF1) register, loads the 9th received bit into RB8_0 (or RB8_1), and sets the RI_0 (or RI_1) bit. If the above conditions are not met, the received data is lost, the SBUF register and RB8 bit are not loaded, and the RI bit is not set. After the middle of the stop bit time, the serial port waits for another high-to-low transition on the (*rxd0_in* or *rxd1_in*) pin.

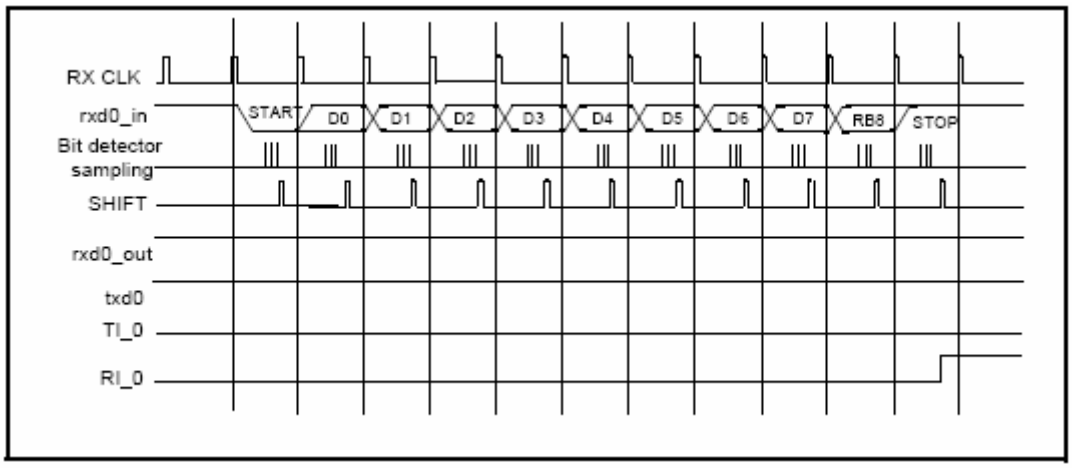


Fig 15-5 Mode 2 Receive Timing

15.2.4 Mode 3

Mode 3 provides asynchronous, full-duplex communication, using a total of 11 bits: 1 start bit, 8 data bits, a programmable 9th bit, and 1 stop bit. The data bits are transmitted and received LSB first.

The mode 3 transmit and operations are identical to mode 2. The mode 3 baud rate generation is identical to mode 1. That is, mode 3 is a combination of mode 2 protocol and mode 1 baud rate.

15.2.5 Multiprocessor Communications

The multiprocessor communication feature is enabled in modes 2 and 3 when the SM2 bit is set in the SCON SFR for a serial port (SM2_0 for Serial Port 0, SM2_1 for Serial Port 1). In multiprocessor communication mode, the 9th bit received is stored in RB8_0 (or RB8_1) and, after the stop bit is received, the serial port interrupt is activated only if RB8_0 (or RB8_1) = 1.

A typical use for the multiprocessor communication feature is when a master wants to send a block of data to one of several slaves. The master first transmits an address byte that identifies the target slave. When transmitting an address byte, the master sets the 9th bit to 1; for data bytes, the 9th bit is 0.

When SM2_0 (or SM2_1) = 1, no slave will be interrupted by a data byte. However, an address byte interrupts all slaves so that each slave can examine the received address byte to determine whether that slave is being addressed. Address decoding must be done by software during the interrupt service routine. The addressed slave clears its SM2_0 (or SM2_1) bit and prepares to receive the data bytes. The slaves that are not being addressed leave the SM2_0 (or SM2_1) bit set and ignore the incoming data bytes.

15.2.6 UART1 38 KHz Infrared Modulation

The output of the UART1 TX1 supports the 38 KHz infrared modulation. As shown **fig 15-1**, the 38 KHz infrared modulation signal actually is the output of the 38 KHz clock signal executes OR-operation with CPU52 TX1 signal. Namely when CPU52 TXs1=1, the UART1 TX1 output is 1; when CPU52 TXs 1=0, the UART1 TX1 output is 38 kHz signal.

The IRTX1(the SFR P3 CFG.1) is used to control the start and stop of the output pin TX1 of the UART1 38 KHz infrared modulation. When IRTX 1=1, 38 KHz infrared signal modulation is enabled; when IRTX 1=0, 38 KHz infrared modulation is disabled.

The 38kHz signal is generated by system clock ,especially only when the system clock comes from the external high frequency crystal oscillator clock 11.0592MHzs / 5.5296MHZs /

2.7648MHzs / 1.3824MHzs, f38k just is the 38kHz signal, but when the system clock comes from the external low frequency crystal oscillator clock or internal RC oscillator,the frequency of the signal of the f38k is lower then 38 kHz(see clockchapter).Under this condition, if the infrared 38KHz modulation function is enabled, modulation will be failure.

While using infrared 38KHz modulation function for communication, the input pin RX1 of the UART1 connects with outside infrared modulation can be used to receive signal that already been demodulated by 38KHz infrared, for outside infrared modulation is equivalent to a grounded resistance which is about 1 million ohm. In order to ensure the pin RX1 has no creepage when system is under the power down mode , there is no internal up-pull resistance. When using UART1 as infrared communication interface, up-pull resistance is needed.

15.2.7 Clock of Infrared modulation

1.When the system clock derives from the fosc, namely fsys=fosc or fsys=fosc/2,clock of infrared modulation firf=fsys/36, infrared f38k=firf/4, under this frequency, the f38k output is unequal to 38kHZ, the infrared output is abnormal.

2.when the fsys derives from the high frequency oscillator, frequency of the firf would be automatically adjusted according to PRIP[1:0] options , shown in the table below, and frequency of the f38k is 38kHz, infrared output is normal.

Table 15-6 configurations of infrared output

PRIP[1:0]		SYSCK 0	fpri	fsys	firf=fsys/18	IRN	f38k=firf/IRN
0	0	0	11.0592MHz	11.0592MHz	614.4 KHz	16	38.4 KHz
		1	11.0592MHz	5.5296MHz	307.2 KHz	8	38.4 KHz
0	1	0	5.5296MHz	5.5296MHz	307.2 KHz	8	38.4 KHz
		1	5.5296MHz	2.7648MHz	153.6 KHz	4	38.4 KHz
1	0	0	2.7648MHz	2.7648MHz	153.6 KHz	4	38.4 KHz
		1	2.7648MHz	1.3824MHz	76.8 KHz	2	38.4 KHz
1	1	0	1.3824MHz	1.3824MHz	76.8 KHz	2	38.4 KHz
		1	1.3824MHz	0.6912MHz	38.4 KHz	1	38.4 KHz

15.2.8 Configure RX0/RX1 as The input of /INT0 and /INT1

In order to wake-up from PDM through serial ports, the RX0/RX1 can be configured as the input of /INT0 and /the INT1, as shown in the**fig 15-1**. Configuring the SFR RXCON(0 xC6H, **table 15-13**) can select this function. When the RXCON is 10 XXX101, input signals of the /INT0 and /INT1 of CPU52 is just from the pins /INT0 and /INT1. When RXCON=10XXX101, input signals of the /INT0 and /INT1of CPU52 may come from RX0, RX1, INT0 and /INT1.

While using the UART1 to perform infrared communication, configuring RX1 as the input of the /INT0 or/INT1 of the CPU52 by setting up the SFR RXCON, ATT7025 can wake-up from PDM through infrared communication. CPU52 wakes by testing the input of the /INT0 and /the INT1 input of itself,therefore,only two methods that make CPU52 to wake-up from PDM can be implemented at the same time,not all of RX0, RX1, INT0 and /INT1.

15.3 Registers

Table 15-7 Register list of UART0 and UART1

adress	name	reset value	function description
0x98	SCON0	0x00	Serial Port 0 control (Table 15-8).

0x99	SBUF0	0x00	Serial Port 0 buffer.
0xC0	SCON1	0x00	Serial Port 0 control (Table 15-9). 15-9
0xC1	SBUF1	0x00	Serial Port 1 buffer
0x87	PCON	0x30	Serial Port 0 Baud rate control (Table 15-10)
0xD8	SMOD1	0x40	Serial Port 1 Baud rate control (Table 15-11)
0xBB	P3CFG	0x00	P3 output multi-configure rgister, write-protect(Table 15-12)
0xC6	RXCON	0x00	RX control (Table 15-13)
0xD8	EICON	0x40	extend inrerrupt control (table 4-6)

1.

Table15-8 UART0 Control Rigister (SCON0 0x98H)

UART0 Control Register (SCON0)			Address: 98H					
	Bit7	6	5	4	3	2	1	Bit0
Read: Write:	SM0_0	SM1_0	SM2_0	REN_0	TB8_0	RB8_0	TI_0	RI_0
Reset:	0	0	0	0	0	0	0	0

bit	description
SCON0.7	SM0_0: Serial Port 0 mode bit 0.
SCON0.6	SM1_0:Serial Port 0 mode bit 1, decoded as: SM1_0 | SM0_0 | mode | function description | Baud rate 0 | 0 | 0 | no support | — 0 | 1 | 1 | 8 bit UART | alterable 1 | 0 | 2 | 9 bit UART | fcpu/64 or fcpu/32 1 | 1 | 3 | 9 bit UART | alterable
SCON0.5	SM2_0 – Multiprocessor communication enable. In modes 2 and 3, M2_0 enables the multiprocessor communication feature. If SM2_0 = 1 in mode 2 or 3, RI_0 will not be activated if the received 9th bit is 0. If M2_0 = 1 in mode 1, RI_0 will only be activated if a valid stop is received. In mode 0, SM2_0 establishes the baud rate: when SM2_0 = 0, the baud rate is clk/12; when SM2_0 = 1, the baud rate is clk/4.
SCON0.4	REN_0 – Receive enable. When REN_0 = 1, reception is enabled.
SCON0.3	TB8_0 – Defines the state of the 9th data bit transmitted in modes 2 and 3.
SCON0.2	RB8_0 – In modes 2 and 3, RB8_0 indicates the state of the 9th bit received. In mode 1, RB8_0 indicates the state of the received stop bit. In mode 0, RB8_0 is not used.
SCON0.1	TI_0 – Transmit interrupt flag. Indicates that the transmit data word has been shifted out. In mode 0, TI_0 is set at the end of the 8th data bit. In all other modes, TI_0 is set when the stop bit is placed on the txd0 pin. TI_0 must be cleared by the software.
SCON0.0	Serial Port Receive Interrupt Flag. Set by hardware at the end of the eighth bit in Mode 0, or halfway through the stop bit in Modes 1, 2, and 3. RI must be cleared by user software.

2.

Table 15-9 UART1 Control Rigister (SCON1 0xC0H)

UART1 Control Register (SCON1)			Address: C0H					
	Bit7	6	5	4	3	2	1	Bit0
Read: Write:	SM0_1	SM1_1	SM2_1	REN_1	TB8_1	RB8_1	TI_1	RI_1
Reset:	0	0	0	0	0	0	0	0

<table>
<tr><th>bit</th><th>function</th></tr>
<tr><td>SCON1.7</td><td>SM0_1:Serial Port 1 mode bit 0.</td></tr>
<tr><td>SCON1. 6</td><td>SM1_1:Serial Port 1 mode bit 1, decoded as:
<table>
<tr><td>SM1_1</td><td>SM0_1</td><td>mode</td><td>function description</td><td>Baud rate</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>no support</td><td>—</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>8 bit UART</td><td>alterable</td></tr>
<tr><td>1</td><td>0</td><td>2</td><td>9 bit UART</td><td>fcpu/64 or fcpu/32</td></tr>
<tr><td>1</td><td>1</td><td>3</td><td>9 bit UART</td><td>alterable</td></tr>
</table></td></tr>
<tr><td>SCON1.5</td><td>SM2_1 – Multiprocessor communication enable. In modes 2 and 3, SM2_1 enables the multiprocessor communication feature. If M2_1 = 1 in mode 2 or 3, RI_1 will not be activated if the received 9th bit is 0. If SM2_1 = 1 in mode 1, RI_1 will only be activated if a valid stop is received. In mode 0, SM2_1 establishes the baud rate: when SM2_1 = 0, the baud rate is clk/12; when SM2_1 = 1, the baud rate is clk/4.</td></tr>
<tr><td>SCON1. 4</td><td>REN_1 – Receive enable. When REN_1 = 1, reception is enabled.</td></tr>
<tr><td>SCON1.3</td><td>TB8_1 – Defines the state of the 9th data bit transmitted in modes 2 and 3.</td></tr>
<tr><td>SCON1.2</td><td>RB8_1 – In modes 2 and 3, RB8_1 indicates the state of the 9th bit received. In mode 1, RB8_1 indicates the state of the received stop bit. In mode 0, RB8_1 is not used.</td></tr>
<tr><td>SCON1.1</td><td>TI_1 – Transmit interrupt flag. Indicates that the transmit data word has been shifted out. In mode 0, TI_1 is set at the end of the 8th data bit. In all other modes, TI_1 is set when the stop bit is placed on the txd1 pin. TI_1 must be cleared by the software.</td></tr>
<tr><td>SCON1.0</td><td>RI_1 – Receive interrupt flag. Indicates that a serial data word has been received. In mode 0, RI_1 is set at the end of the 8th data bit. In mode 1, RI_1 is set after the last sample of the incoming stop bit, subject to the state of SM2_1. In modes 2 and 3, RI_1 is set at the end of the last sample of RB8_1. RI_1 must be cleared by the software.</td></tr>
</table>

3. serial interface UART0 Baud rate control bit

Table 15-10 serial interface UART0 Baud rate control bit (SMOD0)

PCON			Address: 87H					
	Bit7	6	5	4	3	2	1	Bit0
Read:	SMOD0	0	1	1	GF1	GF0	STOP	IDLE
Write:		X	X	X				
Reset:	0	0	1	1	0	0	0	0

Note: when SMOD0=1, the Baud rate of serial interface UART0 is doubled..

4. serial interface UART1 Baud rate control bit

Table 15-11 serial interface UART1 Baud rate control bit (SMOD1)

EICON			Address: D8H					
	Bit7	6	5	4	3	2	1	Bit0
Read:	SMOD1	1	EPFI	PFI	WDTI	0	0	0
Write:		X				X	X	X
Reset:	0	1	0	0	0	0	0	0

Note: when SMOD1=1, the Baud rate of serial interface UART1 is doubled.

5. serial interface UART1 TX1 38KHz modulation enable bit (write protected)

Table 15-12 serial inrerface TX1 38KHz modulation enable bit (IRX1)

P3CFG			Address: BBH					
	Bit7	6	5	4	3	2	1	Bit0
Read:	0	T2	T1	T0	INT1	INT0	IRTX1	0
Write:	X							X
Reset:	0	0	0	0	0	0	0	0

Note: IRTX1 is the control bit. When IRTX1=1, the pin TX1 of serial interface UART1 is enabled to modulate 38KHz infrared signal; When IRTX1=0, the pin TX1 of serial interface UART1 is disabled to modulate 38KHz infrared signal.

6．RX control register

Table15-13 RX Control Rigister(RXCON 0xC6H)

RXCON			Address: C6H					
	Bit7	6	5	4	3	2	1	Bit0
Read: Write:	RXCON7	RXCON6	RXCON5	RXCON4	RXCON3	RXCON2	RXCON1	RXCON0
Reset:	0	0	0	0	0	0	0	0

Note: When RXCON is not equal to 10XXX101, signal of the /INT0 and /INT1 of CPU52 comes from the pins /INT0 and /INT1 directly. When RXCON＝10XXX101, signal of the /INT0 and /INT1 of CPU52 may comes from RX0, RX1, INT0 and /INT1, the configurations are shown as below:

RXCON[7:0]	CPU52 interrupt/INT0 input signal	CPU52 interrupt/INT1 input signal
= 10 000 101	/INT0	/INT1
= 10 001 101	RX0	/INT1
= 10 010 101	RX1	/INT1
= 10 011 101	RX0	RX1
= 10 100 101	/INT0	/INT1
= 10 101 101	/INT0	RX0
= 10 110 101	/INT0	RX1
= 10 111 101	RX1	RX0
not equal 10 xxx 101	/INT0	/INT1

16 SPI

16.1 Introduction

ATT7025 supports four-wire SPI. Features of the SPI module include the following:

- Full-duplex operation
- Master and slave modes
- Double-buffered operation with separate transmit and receive registers
- Eight master mode frequencies : fspi(/4/8/16/32/64/128/256/512)
- Maximum slave mode frequency = fspi/8
- Serial clock with programmable polarity and phase
- Two separately enabled interrupts:
  – SPRF (SPI receiver full)
  – SPTE (SPI transmitter empty)
- Mode fault error flag with CPU interrupt capability
- Overflow error flag with CPU interrupt capability

16.2 Function Description

SPI is a peripheral device of the CPU SFR bus and can be operated by SFR registers and interrupts.

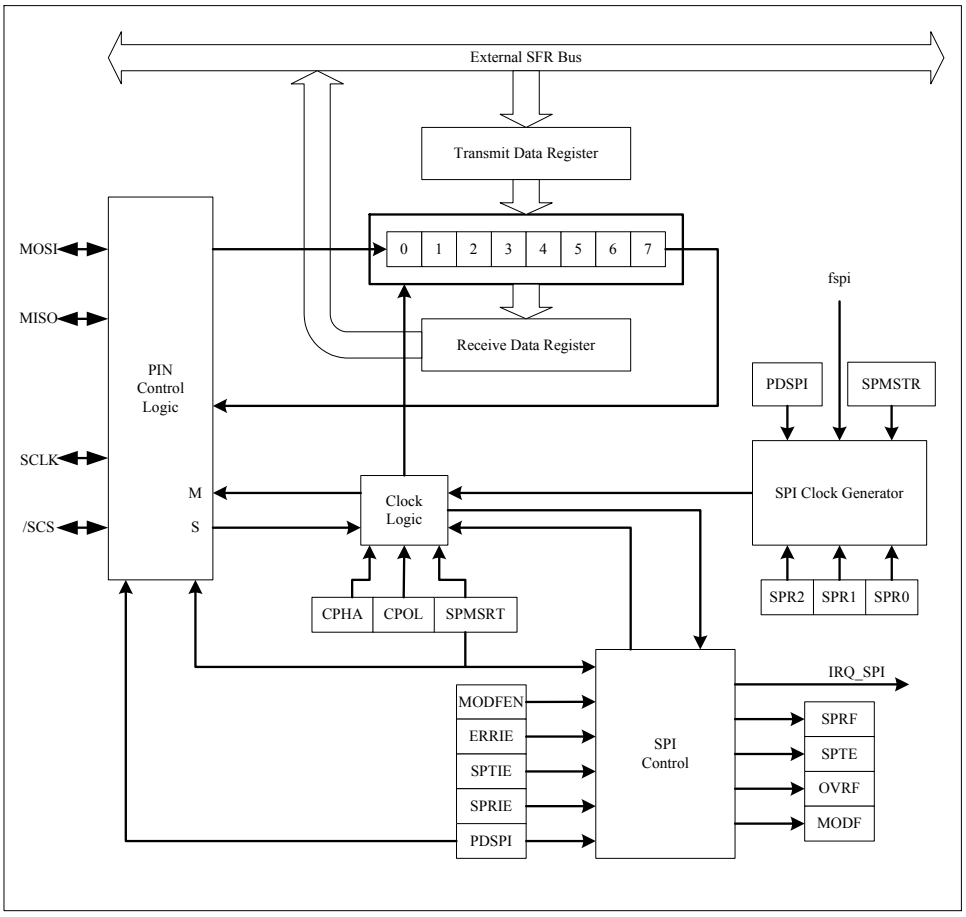


Figure 16-1 SPI Module Block Diagram

16.2.1 SPI Master Mode

The SPI operates in master mode when the SPI master bit, SPMSTR (0xD1H.5, table 16-5), is set.

Only a master SPI module can initiate transmissions. Software begins the transmission from a master SPI module by writing to the transmit data register SPIDR (0xD2H, table 16-6). If the shift register is empty, the byte immediately transfers to the shift register, setting the SPI transmitter empty bit, SPTE(0xB3H.3, table 16-4). The byte begins shifting out on the MOSI pin under the control of the serial clock. Writing to the SPI data register SPIDR(0xD2H) clears the SPTE bit.

The SPR[2:0](0xD1H.[2:0], table 16-5) bits control the baud rate generator and determine the speed of the shift register. Through the SCLK pin, the baud rate generator of the master also controls the shift register of the slave peripheral.

As the byte shifts out on the MOSI pin of the master, another byte shifts in from the slave on the master's MISO pin. The transmission ends when the receiver full bit, SPRF(0xB3H.2, table 16-4), becomes set. At the same time that SPRF becomes set, the byte from the slave transfers to the receive data register. In normal operation, SPRF signals the end of a transmission. Software clears SPRF by reading the SPI status and control register SCIIF (0xB3H, table 16-4)with SPRF set and then reading the SPI data register SPIDR(0xD2H, table 16-6).

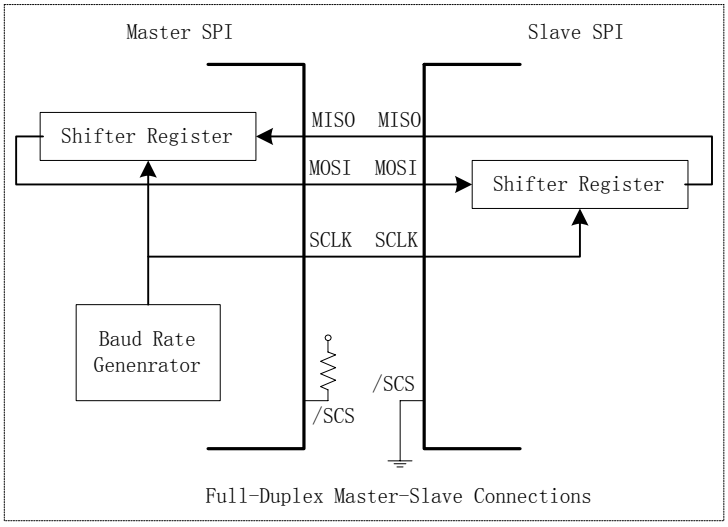


Figure 16-2 Full-Duplex Master-Slave Connections

16.2.2 SPI Slave Mode

The SPI operates in slave mode when the SPMSTR(0xD1H.5, table 16-5) bit is cleared.

In slave mode, the SCLK pin is the input for the serial clock from the master SPI. Before a data transmission occurs, the /SCS pin of the slave SPI must be at logic 0. /SCS must remain low until the transmission is complete.

In a slave SPI module, data enters the shift register under the control of the serial clock from the master SPI module. After a byte enters the shift register of a slave SPI, it transfers to the receive data register, and the SPRF bit is set. To prevent an overflow condition, slave software then must read the receive data register before another full byte enters the shift register.

The frequency of the SCLK for an SPI configured as a slave does not have to correspond to any SPI baud rate. The baud rate only controls the speed of the SCLK generated by an SPI

configured as a master.

When the master SPI starts a transmission, the data in the slave shift register begins shifting out on the MISO pin.

16.2.3 /SCS pin state

When an SPI is configured as a slave, the /SCS pin is always configured as an input. It cannot be used as a general-purpose I/O regardless of the state of the MODFEN control bit.

The CPU can always read the state of the /SCS pin by configuring the appropriate pin as an input and reading the port data register. (See table below)

PDSPI	SPMSTR	MODFEN	SPI Configuration	/SCS state
1	X	X	Not enabled	General-purpose I/O
0	0	X	slave	Input-only to SPI
0	1	0	Master without MODF	General-purpose I/O
0	1	1	Master with MODF	Input-only to SPI

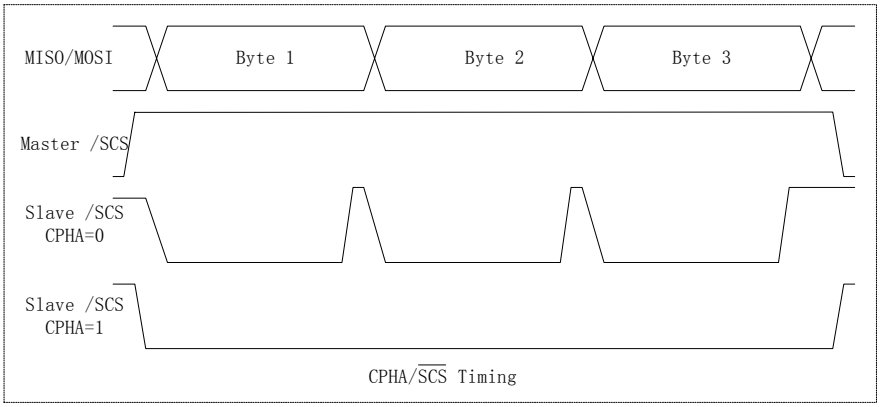
Note: X = Don't care

16.2.4 Clock Phase and Polarity Controls

Software can select any of four combinations of serial clock (SCLK) phase and polarity using two bits CPOL and CPHA. The clock polarity is specified by the CPOL control bit, which selects an active high or low clock and has no significant effect on the transmission format.

The clock phase (CPHA) control bit selects one of two fundamentally different transmission formats. The clock phase and polarity should be identical for the master SPI device and the communicating slave devices.

NOTE: Before writing to the CPOL(0xD1H.4,table 16-5) bit or the CPHA (0xD1H.3,table 16-5)bit, disable the SPI by setting the PDSPI bit.



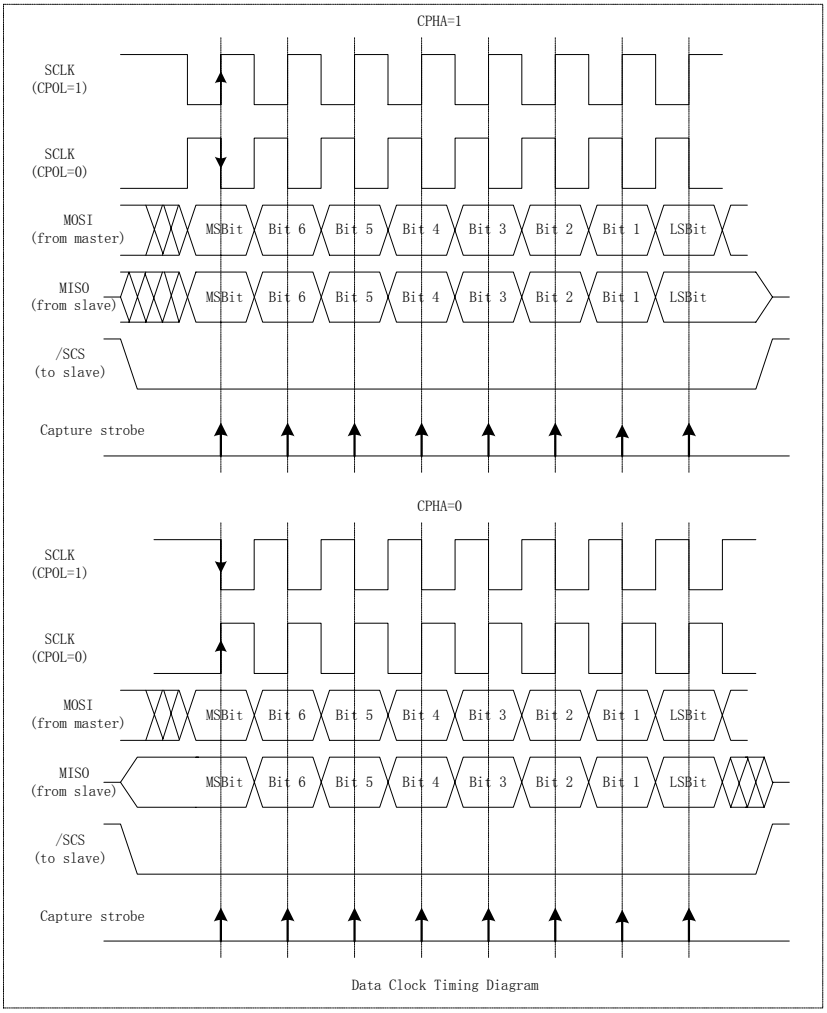


Figure 16-3 Four combinations of SCLK phase and polarity

16.2.5 SPI Error Conditions

Overflow Error (OVRF):

The overflow flag (OVRF) (0xB3H.1,table 16-4)becomes set if the receive data register still has unread data from a previous transmission. If an overflow occurs, all data received after the overflow and before the OVRF(0xB3H.1,table 16-4) bit is cleared does not transfer to the receive data register. The unread data that transferred to the receive data register before the overflow occurred can still be read. Therefore, an overflow error always indicates the loss of data. Clear the overflow flag by reading the SPI status and control register and then reading the SPI data register.

Mode Fault Error (MODF):

Setting the SPMSTR bit selects master mode and configures the SCLK and MOSI pins as outputs and the MISO pin as an input.

Clearing SPMSTR selects slave mode and configures the SCLK and MOSI pins as inputs and the MISO pin as an output.

The mode fault bit, MODF (0xB3H.0,table 16-4), becomes set any time the state of the slave select pin, /SCS, is inconsistent with the mode selected by SPMSTR.

A mode fault error occurs if:

• The /SCS pin of a slave SPI goes high during a transmission
• The /SCS pin of a master SPI goes low at any time

A mode fault in a master SPI causes the following events to occur:

• If ERRIE = 1, the SPI generates an SPI receiver/error CPU interrupt request.
• The PDSPI bit is set.
• The SPTE bit is set.
• The SPI state counter is cleared.
• The data direction register of the shared I/O port regains control of port drivers.

In a slave SPI, the MODF bit generates an interrupt request if the error interrupt enable bit (ERRIE(0xABH.1,table 16-3)) is set. The MODF bit does not set the PDSPI bit or reset the SPI in any way. Software can abort the SPI transmission by setting the PDSPI bit of the slave.

16.2.6 SPI Interrupts

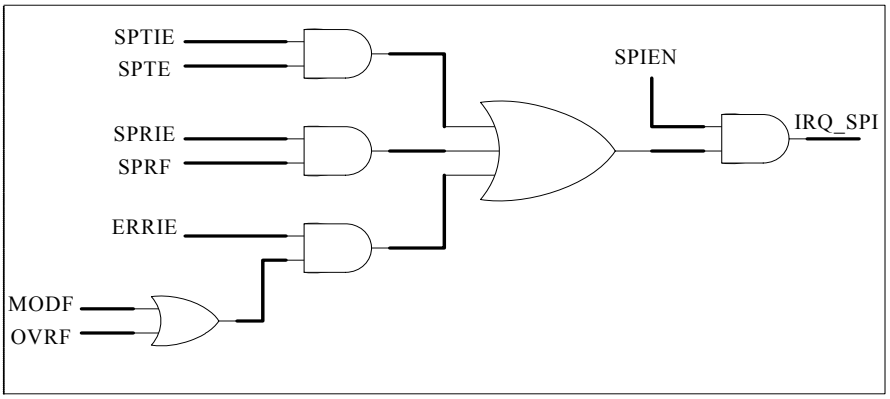


Figure 16-3 SPI interrupt

16.2.7 Resetting the SPI

Any system reset completely resets the SPI. Partial resets occur whenever the PDSPI is set. Whenever PDSPI is set, the following occurs:

• The SPTE flag is set.
• Any transmission currently in progress is aborted.
• The shift register is cleared.
• The SPI state counter is cleared, making it ready for a new complete transmission.
• All the SPI port logic is defaulted back to being general-purpose I/O.

These items are resetted only by a system reset:

• All control bits in the SPICR(0xD1H,table 16-5) register
• The status flags SPRF, OVRF, and MODF

16.3 Registers

Table 16-1 SPI registers list

Address (EPADR)	Name	Byte Length	Function
BFH	PDSPI	1	PDSPI control bit - see **table 16-2**,write protect

ABH	SCIIE	1	SPI&I2C Interrupt Enable Register - see **table 16-3**
B3H	SCIIF	1	SPI&I2C Interrupt Flag Register - see **table 16-4**
D1H	SPICR	1	SPI Control Register - see **table 16-5**
D2H	SPIDR	1	SPI Data Register - see **table 16-6**

SPI registers:

Table 16-2 PDSPI control bit (SUPDC 0xBFH)

System Unit Power-Down Control Register (SUPDC)			Address: BFH					
	Bit7	6	5	4	3	2	1	Bit0
Read:	0	PDTPS	PDEMU	PDBOR	PDLVD	PDLCD	PDI2C	PDSPI
Write:	x							
Reset:	0	0	1	0	0	1	1	1

PDSPI: SPI enable bit

Setting PDSPI causes a partial reset of the SPI.

PDSPI=0: SPI module enabled

PDSPI=1: SPI module disabled

Table 16-3 SCI Interrupt Enable Register (SCIIE 0xABH)

SCI Interrupt Enable Register (SCIIE)			Address: ABH					
	Bit7	6	5	4	3	2	1	Bit0
Read:	0	0	0	I2CIE	SPTIE	SPRIE	ERRIE	0
Write:	x	x	x					X
Reset:	0	0	0	0	0	0	0	0

SPTIE: SPI Transmitter Interrupt Enable

SPTIE=1, enables CPU interrupt requests generated by the SPTE bit.

The SPTE bit is set when a byte transfers from the transmit data register to the shift register.

SPRIE: SPI Receiver Interrupt Enable

SPRIE=1, enables CPU interrupt requests generated by the SPRF bit..

The SPRF bit is set when a byte transfers from the shift register to the receive data register.

ERRIE: Error Interrupt Enable

ERRIE=1, enables both the MODF and the OVER flag to generate CPU interrupt requests

Table 16-4 SCI Interrupt Flag Register (SCIIF 0xB3H)

SCI Interrupt Flag Register (SCIIF)			Address: B3H					
	Bit7	6	5	4	3	2	1	Bit0
Read:	I2RXIF	I2TXIF	I2NKIF	0	SPTE	SPRF	OVRF	MODF
Write:	x	x	x	x	x	x	x	x
Reset:	0	0	0	0	1	0	0	0

SPTE: SPI Transmitter Empty

This clearable, read-only flag is set each time the transmit data register transfers a byte into the shift register. SPTE generates an SPTE CPU interrupt request if the SPTIE bit in the SPI control register is set also.

Do not write to the SPI data register unless the SPTE bit is high.

During an SPTE CPU interrupt, the CPU clears the SPTE bit by writing to the transmit data register SPIDR(0xD2H, table 16-6).

Reset sets the SPTE bit.

1 = Transmit data register empty

0 = Transmit data register not empty

SPRF: SPI Receiver Full

This clearable, read-only flag is set each time a byte transfers from the shift register to the receive data register. SPRF generates a CPU interrupt request if the SPRIE bit in the SPI control register is set also.

During an SPRF CPU interrupt, the CPU clears SPRF by reading the SPI flag register SCIIF(0xB3H) with SPRF set and then reading the SPI data register SPIDR(0xD2H, table 16-6).

OVRF: Overflow Bit

This clearable, read-only flag is set if software does not read the byte in the receive data register before the next full byte enters the shift register. In an overflow condition, the byte already in the receive data register is unaffected, and the byte that shifted in last is lost.

Clear the OVRF bit by reading the flag register SCIIF(0xB3H) with OVRF set and then reading the receive data register SPIDR(0xD2H).

MODF: Mode Fault Bit

This clearable, read-only flag is set in a lave SPI if /SCS pin goes high during a transmission with the MODFEN bit set.

In a master SPI, the MODF flag is set if the /SCS pin goes low at any time with the MODFEN bit set.

Clear the MODF bit by reading the SPI flag register SCIIF(0xB3H) with MODF set and then writing to the SPI control register SPICR(0xD1H).

Table 16-5 SPI Control Register (SPICR 0xD1H)

SPI Control Register (SPICR)			Address: D1H					
	Bit7	6	5	4	3	2	1	Bit0
Read:	0	MODFEN	SPMSTR	CPOL	CPHA	SPR2	SPR1	SPR0
Write:	x							
Reset:	0	0	1	0	1	1	0	0

MODFEN: Mode Fault Enable Bit

This read/write bit, when set to 1, allows the MODF flag to be set. If the MODF flag is set, clearing the MODFEN does not clear the MODF flag.

If the SPI is enabled as a master and the MODFEN bit is low, then the /SCS pin is available as a general-purpose I/O. If the MODFEN bit is set, then this pin is not available as a general - purpose I/O.

When the SPI is enabled as a slave, the /SCS pin is not available as a general-purpose I/O regardless of the value of MODFEN.

If the MODFEN bit is low, the level of the /SCS pin does not affect the operation of an enabled SPI configured as a master. For an enabled SPI configured as a slave, having MODFEN low only prevents the MODF flag from being set. It does not affect any other part of SPI operation.

SPMSTR:SPI Master Bit

This read/write bit selects master mode operation or slave mode operation.

1 = Master mode

0 = Slave mode

CPOL:Clock Polarity Bit

This read/write bit determines the logic state of the SCLK pin between transmissions. To transmit data between SPI modules, the SPI modules must have identical CPOL values.

CPHA:Clock Phase Bit

This read/write bit controls the timing relationship between the serial clock and SPI data. To transmit data between SPI modules, the SPI modules must have identical CPHA values. When CPHA = 0, the /SCS pin of the slave SPI module must be set to logic 1 between bytes.

SPR[2:0]:SPI Baud Rate Select Bits

In master mode, these read/write bits select one of 8 baud rates. SPR[2:0] have no effect in slave mode.

SPR2	SPR1	SPR0	Baud Rate Divisor (BRD)
0	0	0	2
0	0	1	4
0	1	0	8
0	1	1	16
1	0	0	32
1	0	1	64
1	1	0	128
1	1	1	256

Use the foumula to calculate the SPI baud rate:

SPI Baud Rate=fspi/2/BRD

Fspi comes from system clock fsys.

Table 16-6 SPI Data Register (SPIDR 0xD2H)

SPI Data Register (SPIDR)			**Address:**	**D2H**				
	Bit7	**6**	**5**	**4**	**3**	**2**	**1**	**Bit0**
Read:	SPIR7	SPIR6	SPIR5	SPIR4	SPIR3	SPIR2	SPIR1	SPIR0
Write:	SPIT7	SPIT6	SPIT5	SPIT4	SPIT3	SPIT2	SPIT1	SPIT0
Reset:	u	u	u	u	u	u	u	u

The SPI data register consists of the read-only receive data register and the write-only transmit data register. Writing to the SPI data register writes data into the transmit data register. Reading the SPI data register reads data from the receive data register. The transmit data and receive data registers are separate registers that can contain different values.

17 I2C

17.1 Introduction

Features of the I2C module include the following:

- Software controllable acknowledge bit generation
- Interrupt driven byte by byte data transfer
- Calling address identification interrupt
- Auto detection of R/W bit and switching of transmit or receive mode
- Detection of START, repeated START, and STOP signals
- Auto generation of START and STOP condition in master mode
- No-ACK awareness in master mode
- 8 selectable baud rate master clocks
- Automatic recognition of the received acknowledge bit
- Support 7-bit addressing.

The bus timing and electrical characteristics of SDA and SCL have a reference to the IIC bus specification.

17.2 Function Description

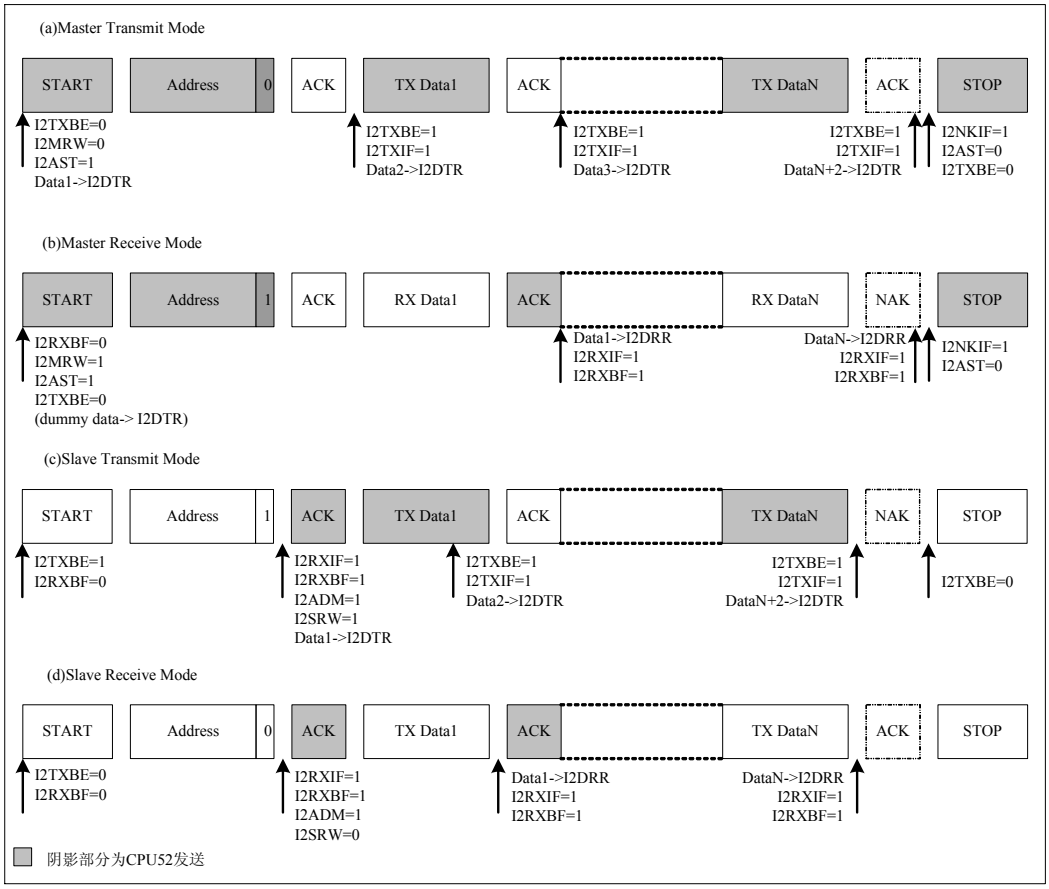


Figure 17-1 **Data Transfer Sequences for Master/Slave Transmit/Receive Modes**

I2C transmit mode are illustrated in Figure 17-1: Master Transmit mode, Master Receive mode, Slave Transmit mode, Slave Receive mode.

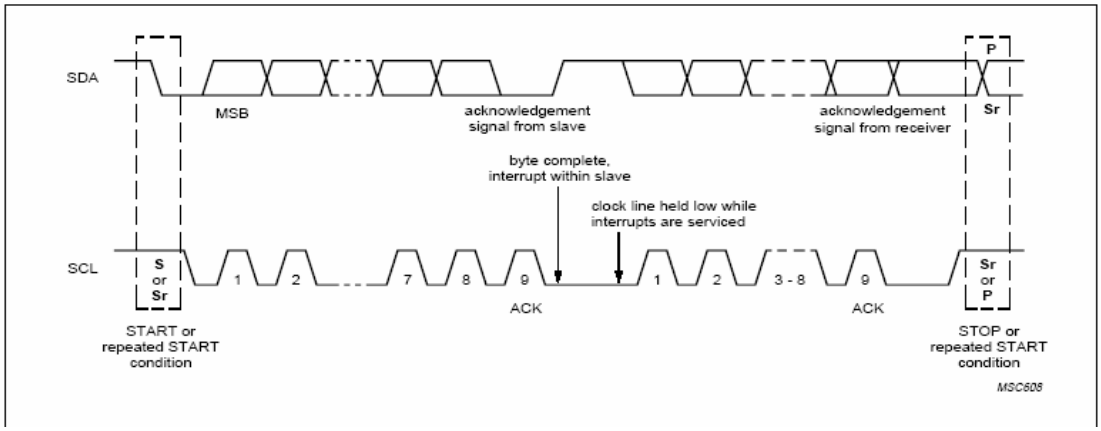


Figure 17-2 Data Transfer on the I2C Bus

Figure 17-2 shows the I2C bus data transfer sequence. It includes the START, ADDRESS, ACK, TxDATA, STOP states, etc. The more detailed has reference to the IIC bus specification.

17.3 Registers

Table 17-1 I2C registers list

Address (EPADR)	Name	Byte Length	Function
BFH	PDI2C	1	PDI2C control bit—see **table 17-3**,write-protect
D3H	I2ADR	1	I2C address register—see **tabl 17-2**
ABH	SCIIE	1	SPI&I2C interrupt enable —see **table17-4**
B3H	SCIIF	1	SPI&I2C interrupt flag register—see **table 17-5**
D4H	I2MCR	1	I2C control register—see **table 17-6**
D5H	I2SR	1	I2C state register—see **table 17-8**
D6H	I2DTR	1	I2C data transmit register—see **table 17-9**
D7H	I2DRR	1	I2C data receive register—see **table 17-10**

Registers:

Table 17-2 I2C Address Register (I2ADR 0xD3H)

I2C Address Register (I2ADR)			**Address:**	**D3H**				
	Bit7	**6**	**5**	**4**	**3**	**2**	**1**	**Bit0**
Read: **Write:**	I2AD6	I2AD5	I2AD4	I2AD3	I2AD2	I2AD1	I2AD0	EXTAD
Reset:	1	0	1	0	0	0	0	0

I2AD[6:0]: (Devices Address)

These seven bits represent the I2C interface's own specific slave address when in slave mode, and the calling address when in master mode.

EXTAD: (Expanded Address)

This bit is set to expand the address of the I2C in slave mode. When set, the I2C will acknowledge the following addresses from a calling master: $I2AD[6:0], 0000000, and 0001100.

Table 17-3 PDI2Ccontrol bit (SUPDC 0xBFH)

System Unit Power-Down Control Register (SUPDC)			**Address:**	**BFH**				
	Bit7	**6**	**5**	**4**	**3**	**2**	**1**	**Bit0**

Read:	0	PDTPS	PDEMU	PDBOR	PDLVD	PDLCD	PDI2C	PDSPI
Write:	x							
Reset:	0	0	1	0	0	1	1	1

PDI2C: I2C enable bit, write-protect

PDI2C=0: I2C module is enabled, and P3.0/SCL and P3.1/SDA pins will be configured as SCL and SDA.

PDI2C=1: I2C module is disabled, and all flags will restore its default states.

Table 17-4 SCI Interrupt Enable Register (SCIIE 0xABH)

SCI Interrupt Enable Register (SCIIE)			Address: ABH					
	Bit7	6	5	4	3	2	1	Bit0
Read:	0	0	0	I2CIE	SPTIE	SPRIE	SPERIE	0
Write:	x	x	x					X
Reset:	0	0	0	0	0	0	0	0

I2CIE: (I2C interrupt enable)

When this bit is set, the I2TXIF, I2RXIF, and I2NAKIF flags are enabled to generate an interrupt request to the CPU. When I2CIE is cleared, then these flags are prevented from generating an interrupt request.

Table 17-5 SCI Interrupt Flag Register (SCIIF 0xB3H)

SCI Interrupt Flag Register (SCIIF)			Address: B3H					
	Bit7	6	5	4	3	2	1	Bit0
Read:	I2RXIF	I2TXIF	I2NKIF	0	SPTEIF	SPRFIF	SPOVIF	SPMDIF
Write:	x	x		x	x	x	x	x
Reset:	0	0	0	0	0	0	0	0

I2RXIF: (Receive Interrupt Flag)

This flag is set after the data receive register I2DRR(0xD7H, table 17-10) is loaded with a new received data. Once the I2DRR is loaded with received data, no more received data can be loaded to the I2DRR register until the CPU reads the data from the I2DRR to clear I2RXBF(0xD5H.0, table 17-8) flag.

I2RXIF generates an interrupt request to CPU if the I2CIE bit is also set. This bit is cleared by writing "0" to it or by reset; or when the PDI2C= 1.

I2TXIF: (Transmit Interrupt Flag)

This flag is set when data in the data transmit register I2DTR(0xD6H, table 17-9) is downloaded to the output circuit, and that new data can be written to the I2DTR.

I2TXIF generates an interrupt request to CPU if the I2CIE bit is also set. This bit is cleared by writing "0" to it or by reset; or when the PDI2C= 1.

I2NKIF: (No Acknowledge Interrupt Flag)

This flag is only set in master mode (I2AST = 1) when there is no acknowledge bit detected after one data byte or calling address is transferred. This flag also clears I2AST.

I2NKIF generates an interrupt request to CPU if the I2CIE bit is also set. This bit is cleared by writing "0" to it or by reset.

Table 17-6 I2C Master Control Register (I2MCR 0xD4H)

I2C Master Control Register (I2MCR)			Address: D4H					
	Bit7	6	5	4	3	2	1	Bit0
Read:	I2TXAK	I2RPS	I2BB	I2AST	I2MRW	I2BR2	I2BR1	I2BR0
Write:			X					
Reset:	0	0	0	0	0	0	0	0

I2TXAK: (Transmit Acknowledge Enable)

This bit is set to disable the I2C from sending out an acknowledge signal to the bus at the 9th clock bit after receiving 8 data bits. When I2TXAK is cleared, an acknowledge signal will be sent at the 9^{th} clock bit.

I2RPS: (Repeated Start Enable)

This bit is set to enable repeated START signal to be generated when in master mode transfer (I2AST = 1). The I2RPS bit is cleared by hardware after the completion of repeated START signal or when the I2AST bit is cleared.

I2BB: (Bus Busy Flag)

This flag is set after a start condition is detected (bus busy), and is cleared when a stop condition (bus idle) is detected.

I2AST: (Master Control Bit)

This bit is set to initiate a master mode transfer.

In master mode, the module generates a start condition to the SDA and SCL lines, followed by sending the calling address stored in I2ADR.

When the I2AST bit is cleared by I2NKIF set (no acknowledge) or by software, the module generates the stop condition to the lines after the current byte is transmitted.

I2MRW: (Master Read/Write**)**

This bit will be transmitted out as bit 0 of the calling address when the module sets the I2AST bit to enter master mode. The I2MRW bit determines the transfer direction of the data bytes that follows. When it is "1", the module is in master receive mode. When it is "0", the module is in master transmit mode.

I2BR[2:0]: (Baud Rate Select)

Table 17-7 Baud Rate Select

I2BR2	I2BR1	I2BR0	Baud Rate (fi2c=fsys)
0	0	0	Fi2c/8
0	0	1	fi2c/16
0	1	0	fi2c/32
0	1	1	fi2c/64
1	0	0	fi2c/128
1	0	1	fi2c/256
1	1	0	fi2c/512
1	1	1	fi2c/1024

Table 17-8 I2C Status Register (I2SR 0xD5H)

I2C Status Register (I2SR)			Address: D5H					
	Bit7	6	5	4	3	2	1	Bit0
Read:	0	0	I2ADM	I2SRW	I2RXAK	0	I2TXBE	I2RXBF
Write:	X	X	x	x	X	x	x	x
Reset:	0	0	0	0	1	0	1	0

I2ADM: (Address Match**)**

This flag is set when the received data in the data receive register (I2DRR) is an calling

address which matches with the address or its extended addresses (I2EXTAD=1) specified in the I2ADR register.

1 = Received address matches I2ADR

0 = Received address does not match

I2SRW: (Slave Read/Write**)**

This bit indicates the data direction when the module is in slave mode. It is updated after the calling address is received from a master device. I2SRW = 1 when the calling master is reading data from the module (slave transmit mode). I2SRW = 0 when the master is writing data to the module (receive mode).

1 = Slave mode transmit

0 = Slave mode receive

I2RXAK: (Receive Acknowledge)

When this bit is cleared, it indicates an acknowledge signal has been received after the completion of 8 data bits transmission on the bus. When I2RXAK is set, it indicates no acknowledge signal has been detected at the 9th clock; the module will release the SDA line for the master to generate "stop" or "repeated start" condition.

I2TXBE: (Transmit Buffer Empty)

This flag indicates the status of the data transmit register (I2DTR). When the CPU writes the data to the I2DTR, the I2TXBE flag will be cleared. I2TXBE is set when I2DTR is emptied by a transfer of its data to the output circuit.

I2RXBF: (Receive Buffer Full)

This flag indicates the status of the data receive register (I2DRR). When the CPU reads the data from the I2DRR, theI2RXBF flag will be cleared. I2RXBF is set when I2DRR is full by a transfer of data from the input circuit to the I2DRR.

Table 17-9 I2C Data Transmit Register (I2DTR 0xD6H)

I2C Data Transmit Register(I2DTR)			Address: D6H					
	Bit7	6	5	4	3	2	1	Bit0
Read: Write:	I2TD7	I2TD6	I2TD5	I2TD4	I2TD3	I2TD2	I2TD1	I2TD0
Reset:	1	1	1	1	1	1	1	1

When the I2C module is enabled, PDI2C = 0, data written into this register depends on whether module is in master or slave mode.

In slave mode, the data in I2DTR will be transferred to the output circuit when:

- the module detects a matched calling address (I2ADM = 1), with the calling master requesting data (I2SRW = 1);or
- the previous data in the output circuit has be transmitted and the receiving master returns an acknowledge bit, indicated by a received acknowledge bit (I2RXAK = 0).

If the calling master does not return an acknowledge bit (I2RXAK = 1), the module will release the SDA line for master to generate a "stop" or "repeated start" condition. The data in the I2DTR will not be transferred to the output circuit until the next calling from a master. The transmit buffer empty flag remains cleared (I2TXBE = 0).

In master mode, the data in I2DTR will be transferred to the output circuit when:

- the module receives an acknowledge bit (I2RXAK = 0), after setting master transmit mode (I2RW = 0), and the calling address has been transmitted; or

• the previous data in the output circuit has be transmitted and the receiving slave returns an acknowledge bit, indicated by a received acknowledge bit (I2RXAK = 0).

If the slave does not return an acknowledge bit (I2RXAK = 1), the master will generate a "stop" or "repeated start" condition. The data in the I2DTR will not be transferred to the output circuit. The transmit buffer empty flag remains cleared (I2TXBE = 0).

Table 17-10 I2C Data Receive Register (I2DRR 0xD7H)

I2C Data Receive Register (I2DRR)			Address: D7H					
	Bit7	6	5	4	3	2	1	Bit0
Read:	I2RD7	I2RD6	I2RD5	I2RD4	I2RD3	I2RD2	I2RD1	I2RD0
Write:	x	X	x	x	x	x	x	x
Reset:	0	0	0	0	0	0	0	0

When the I2C module is enabled, PDI2C = 0, data in this read-only register depends on whether module is in master or slave mode.

In slave mode, the data in I2DRR is:

• the calling address from the master when the address match flag is set (I2ADM = 1); or

• the last data received when I2ADM = 0.

In master mode, the data in the I2DRR is:

• the last data received.

When the I2DRR is read by the CPU, the receive buffer full flag is cleared (I2RXBF = 0), and the next received data is loaded to the I2DRR. Each time when new data is loaded to the I2DRR, the I2RXIF interrupt flag is set, indicating that new data is available in I2DRR.

17.4 I/O signals

Both SDA and SCL are bidirectional lines, connected to a positive supply voltage via a pull-up resistor (see Figure 17-3). When the bus is free, both lines are HIGH. The output stages of devices connected to the bus must have an open-drain or open-collector in order to perform the wired-AND function.

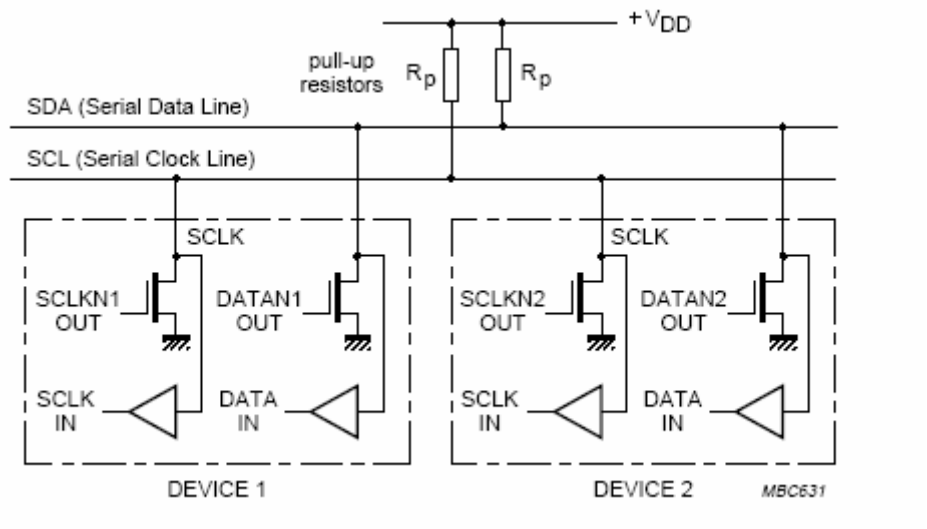


Figure 17-3 Connection of I2C-bus devices to the I2C-bus

18 GPIO

18.1 Introduction

Sixty-six bidirectional I/O pins form nine parallel ports. All I/O pins are programmable as inputs or outputs. These pins contain Schmitt trigger and glitch filter for improved EMC performance. These pins also contain an internal 30K pull-up resistor.

Avoid glitches on port pins by writing to the port data register bits before changing data direction register bits from 1 to 0.

18.2 Multiplexing Configuration

Table 18-1 LCD Output Multiplexing Configuration Register (LCDCFG 0xB9H)

LCDCFG			Address: B9H					
	Bit7	6	5	4	3	2	1	Bit0
Read: Write:	PDH	PDL	PTCH	PTCL	PTBH	PTBL	PTAH	PTAL
Reset:	0	0	0	0	0	0	0	0

Write-protect register

PTAL=0:	SEG1/PA0－SEG4/PA3 configured as GPIO:	PA0-PA3
PTAL=1:	SEG1/PA0－SEG4/PA3 configured as LCD output:	SEG1-SEG4
PTAH=0:	SEG5/PA4－SEG8/PA7 configured as GPIO:	PA4-PA7
PTAH=1:	SEG5/PA4－SEG8/PA7 configured as LCD output:	SEG5-SEG8
PTBL=0:	SEG9/PB0－SEG12/PB3 configured as GPIO:	PB0-PB3
PTBL=1:	SEG9/PB0－SEG12/PB3 configured as LCD output:	SEG9-SEG12
PTBH=0:	SEG13/PB4－SEG16/PB7 configured as GPIO:	PB4-PB7
PTBH=1:	SEG13/PB4－SEG16/PB7 configured as LCD output:	SEG13-SEG16
PTCL=0:	SEG17/PC0－SEG20/PC3 configured as GPIO:	PC0-PC3
PTCL=1:	SEG17/PC0－SEG20/PC3 configured as LCD output	SEG17-SEG20
PTCH=0:	SEG21/PC4－SEG24/PC7 configured as GPIO:	PC4-PC7
PTCH=1:	SEG21/PC4－SEG24/PC7 configured as LCD output:	SEG21-SEG24
PTDL=0:	SEG25/PD0－SEG28/PD3 configured as GPIO:	PD0-PD3
PTDL=1:	SEG25/PD0－SEG28/PD3 configured as LCD output:	SEG25-SEG28
PTDH=0:	SEG29/PD4－SEG32/PD7 configured as GPIO:	PD4-PD7
PTDH=1:	SEG29/PD4－SEG32/PD7 configured as LCD output:	SEG29-SEG32

Table 18-2 P0 and P2 Output Multiplexing Configuration Register (P02CFG 0xBAH)

P02CFG			Address: BAH					
	Bit7	6	5	4	3	2	1	Bit0
Read: Write:	P267	P245	P223	P201	P067	P045	P023	P001
Reset:	0	0	0	0	0	0	0	0

Write-protect register.

P001=0:	SEG33/P0.0－SEG34/P0.1 configured as GPIO:	P0.0-P0.1
P001=1:	SEG33/P0.0－SEG34/P0.1 configured as LCD output:	SEG33-SEG34
P023=0:	SEG35/P0.2－SEG36/P0.3 configured as GPIO:	P0.2-P0.3
P023=1:	SEG35/P0.2－SEG36/P0.3 configured as LCD output:	SEG35-SEG36
P045=0:	SEG37/P0.4－SEG38/P0.5 configured as GPIO:	P0.4-P0.5

P045=1: SEG37/P0.4－SEG38/P0.5 configured as LCD output: SEG37-SEG38
P067=0: SEG39/P0.6－SEG40/P0.7 configured as GPIO: P0.6-P0.7
P067=1: SEG39/P0.6－SEG40/P0.7 configured as LCD output: SEG39-SEG40
P201=0: TX1/P2.0－RX1/P2.1 configured as UART1: TX1-RX1
P201=1: TX1/P2.0－RX1/P2.1 configured as GPIO: P2.0-P2.1
P223=0: TX0/P2.2－RX0/P2.3 configured as UART0: TX0-RX0
P223=1: TX0/P2.2－RX0/P2.3 configured as GPIO: P2.2-P2.3
P245=0: LVDIN/P2.4 configured as LVDIN: LVDIN
P245=0: SF/P2.5 configured as pulse output: SF
P245=1: LVDIN/P2.4－SF/P2.5 configured as GPIO: P2.4-P2.5
P267=0: PF/P2.6－QF/P2.7 configured as pulse output: PF-QF
P267=1: PF/P2.6－QF/P2.7 configured as GPIO: P2.6-P2.7

Table 18-3 P1 Output Multiplexing Configuration Register (KEYIE 0xADH)

KEY Interrupt Enable Register (KEYIE)			Address: ADH					
	Bit7	6	5	4	3	2	1	Bit0
Read:	0	KEYIE6	KEYIE5	KEYIE4	KEYIE3	KEYIE2	KEYIE1	KEYIE0
Write:	X							
Reset:	0	0	0	0	0	0	0	0

KEYIEx=0: P1.x/KEYx configured as GPIO: P1.x
KEYIEx=1: P1.x/KEYx configured as keyboard input: KEYx

Table 18-4 P3 Output Multiplexing Configuration Register (P3CFG 0xBBH)

P3CFG			Address: BBH					
	Bit7	6	5	4	3	2	1	Bit0
Read:	Reserved	T2	T1	T0	INT1	INT0	IRTX1	0
Write:								X
Reset:	0	0	0	0	0	0	0	0

Write-protect register

INT0=0: P3.2/INT0 configured as GPIO: P3.2
INT0=1: P3.2/INT0 configured as: /INT0
INT1=0: P3.3/INT1 configured as GPIO: P3.3
INT1=1: P3.3/INT1 configured as: /INT1
T0=0: P3.4/T0 configured as:GPIO: P3.4
T0=1: P3.4/T0 configured as: T0
T1=0: P3.5/T1 configured as GPIO: P3.5
T1=1: P3.5/T1 configured as: T1
T2=0: P3.6/T2 configured as GPIO: P3.6
T2=1: P3.6/T2 configured as: T2

18.3 Port P0

Port P0 is a 8-bit parallel port that shares its pins with LCD SEG33-SEG40. P0.0-P0.7 can be configured for Direct LED drive.

Table 18-5 P0 Port Data Register (P0 0x80H)

P0			Address: 80H					
	Bit7	6	5	4	3	2	1	Bit0
Read:	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0
Write:								

Reset:	u	u	u	u	u	u	u	u

Table 18-6 P0 Port Direction Register (DDRP0 0xA1H))

DDRP0			Address: A1H					
	Bit7	6	5	4	3	2	1	Bit0
Read: Write:	DDRP07	DDRP06	DDRP05	DDRP04	DDRP03	DDRP02	DDRP01	DDRP00
Reset:	0	0	0	0	0	0	0	0

0 = Corresponding port pin configured as input

1 = Corresponding port pin configured as output

Table 18-7 P0 Port LED Control Register (LEDP0 0xA5H)

LEDP0			Address: A5H					
	Bit7	6	5	4	3	2	1	Bit0
Read: Write:	LEDP07	LEDP06	LEDP05	LEDP04	LEDP03	LEDP02	LEDP01	LEDP00
Reset:	0	0	0	0	0	0	0	0

0 = Corresponding port pin configured for standard drive

1 = Corresponding port pin configured for LED drive, 10mA sinking current

Note: Corresponding Direction register bit DDRP0x should be configured as output for LED drive.

18.4 Port P1

Port P1 is a 7-bit parallel port that shares its pins with KEY0-KEY6. P1.0-P1.6 can be configured for Direct LED drive.

Table 18-8 P1 Data Register (P1 0x90H)

P1			Address: 90H					
	Bit7	6	5	4	3	2	1	Bit0
Read: Write:	Reserved	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0
Reset:	u	u	u	U	u	u	u	u

Table 18-9 P1 Direction Register (DDRP1 0xA2H)

DDRP1			Address: A2H					
	Bit7	6	5	4	3	2	1	Bit0
Read:	0	DDRP16	DDRP15	DDRP14	DDRP13	DDRP12	DDRP11	DDRP10
Write:	X							
Reset:	0	0	0	0	0	0	0	0

0 = Corresponding port pin configured as input

1 = Corresponding port pin configured as output

Table 18-10 P1 Port LED Control Register (LEDP1 0xA6H)

LEDP1			Address: A6H					
	Bit7	6	5	4	3	2	1	Bit0
Read: Write:	Reserved	LEDP16	LEDP15	LEDP14	LEDP13	LEDP12	LEDP11	LEDP10
Reset:	0	0	0	0	0	0	0	0

0 = Corresponding port pin configured for standard drive

1 = Corresponding port pin configured for LED drive, 10mA sinking current

Note: Corresponding Direction register bit DDRP1x should be configured as output for LED drive. Bit7 is reserved and modification is not recommended.

18.5 Port P2

Port P2 is a 8-bit parallel port that shares its pins with RX0/TX0/RX1/TX1/LVDIN/PF/QF/SF.

Table 18-11 P2 Data Register (P2 0xA0H)

P2			Address: A0H					
	Bit7	6	5	4	3	2	1	Bit0
Read: Write:	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0
Reset:	u	u	u	U	u	u	u	u

Table 18-12 P2 Direction Register (DDRP2 0xA3H)

DDRP2			Address: A3H					
	Bit7	6	5	4	3	2	1	Bit0
Read: Write:	DDRP27	DDRP26	DDRP25	DDRP24	DDRP23	DDRP22	DDRP21	DDRP20
Reset:	0	0	0	0	0	0	0	0

0 = Corresponding port pin configured as input

1 = Corresponding port pin configured as output

18.6 Port P3

Port P3 is a 7-bit parallel port that shares its pins with SCL/SDA/INT0/INT1/T0/T1/T2. The P3.0-P3.6 can be configured for Direct LED drive.

Table 18-13 P3 Data Register (P3 0xB0H)

P3			Address: B0H					
	Bit7	6	5	4	3	2	1	Bit0
Read: Write:	Reserved	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0
Reset:	u	u	u	U	u	u	u	u

Table 18-14 P3 Direction Reister (DDRP3 0xA4H)

DDRP3			Address: A4H					
	Bit7	6	5	4	3	2	1	Bit0
Read: Write:	Reserved	DDRP36	DDRP35	DDRP34	DDRP33	DDRP32	DDRP31	DDRP30
Reset:	0	0	0	0	0	0	0	0

0 = Corresponding port pin configured as input

1 = Corresponding port pin configured as output

Table 18-15 P3 Port LED Control Register (LEDP3 0xA7H)

LEDP3			Address: A7H					
	Bit7	6	5	4	3	2	1	Bit0
Read: Write:	Reserved	LEDP36	LEDP35	LEDP34	LEDP33	LEDP32	LEDP31	LEDP30
Reset:	0	0	0	0	0	0	0	0

0 = Corresponding port pin configured for standard drive

1 = Corresponding port pin configured for LED drive, 10mA sinking current

Note: Corresponding Direction register bit DDRP3x should be configured as output for LED drive. Bit7 is reserved and modification is not recommended.

18.7 Port A

Port A is a 8-bit parallel port that shares its pins with LCD SEG1-SEG8.

Table 18-16 PTA Data Register (PTA 0x93H)

PTA			Address: 93H					
	Bit7	6	5	4	3	2	1	Bit0
Read: Write:	PTA7	PTA6	PTA5	PTA4	PTA3	PTA2	PTA1	PTA0
Reset:	u	u	u	U	u	u	u	u

Table 18-17 PTA Direction Register (DDRA 0x9BH)

DDRA			Address: 9BH					
	Bit7	6	5	4	3	2	1	Bit0
Read: Write:	DDRA7	DDRA6	DDRA5	DDRA4	DDRA3	DDRA2	DDRA1	DDRA0
Reset:	0	0	0	0	0	0	0	0

0 = Corresponding port pin configured as input

1 = Corresponding port pin configured as output

18.8 Port B

Port B is a 8-bit parallel port that shares its pins with LCD SEG9-SEG16.

Table 18-18 PTB Data Register (PTB 0x94H)

PTB			Address: 94H					
	Bit7	6	5	4	3	2	1	Bit0
Read: Write:	PTB7	PTB6	PTB5	PTB4	PTB3	PTB2	PTB1	PTB0
Reset:	u	u	u	U	u	u	u	u

Table 18-19 PTB Direction Register (DDRB 0x9CH)

DDRB			Address: 9CH					
	Bit7	6	5	4	3	2	1	Bit0
Read: Write:	DDRB7	DDRB6	DDRB5	DDRB4	DDRB3	DDRB2	DDRB1	DDRB0
Reset:	0	0	0	0	0	0	0	0

0 = Corresponding port pin configured as input

1 = Corresponding port pin configured as output

18.9 Port C

Port C is a 8-bit parallel port that shares its pins with LCD SEG17-SEG24. The PTC0-PTC7 can be configured for Direct LED drive.

Table 18-20 PTC Data Register (PTC 0x95H)

PTC			Address: 95H					
	Bit7	6	5	4	3	2	1	Bit0
Read: Write:	PTC7	PTC6	PTC5	PTC4	PTC3	PTC2	PTC1	PTC0
Reset:	u	u	u	U	u	u	u	u

Table 18-21 PTC Direction Register (DDRC 0x9DH)

DDRC			Address: 9DH					
	Bit7	6	5	4	3	2	1	Bit0
Read: Write:	DDRC7	DDRC6	DDRC5	DDRC4	DDRC3	DDRC2	DDRC1	DDRC0
Reset:	0	0	0	0	0	0	0	0

0 = Corresponding port pin configured as input

1 = Corresponding port pin configured as output

Table 18-22 PTC LED Control Register (LEDC 0xAEH)

LEDC			Address: AEH					
	Bit7	6	5	4	3	2	1	Bit0
Read: Write:	LEDC7	LEDC6	LEDC5	LEDC4	LEDC3	LEDC2	LEDC1	LEDC0
Reset:	0	0	0	0	0	0	0	0

0 = Corresponding port pin configured for standard drive

1 = Corresponding port pin configured for LED drive, 10mA sinking current

Note: Corresponding Direction register bit DDRCx should be configured as output for LED drive.

18.10 Port D

Port D is a 8-bit parallel port that shares its pins with LCD SEG25-SEG32.

Table 18-23 PTD Data Register PTD 0x96H)

PTD			Address: 96H					
	Bit7	6	5	4	3	2	1	Bit0
Read: Write:	PTD7	PTD6	PTD5	PTD4	PTD3	PTD2	PTD1	PTD0
Reset:	u	u	u	U	u	u	u	u

Table 18-24 PTD Direction Register (DDRD 0x9EH)

DDRD			Address: 9EH					
	Bit7	6	5	4	3	2	1	Bit0
Read: Write:	DDRD7	DDRD6	DDRD5	DDRD4	DDRD3	DDRD2	DDRD1	DDRD0
Reset:	0	0	0	0	0	0	0	0

0 = Corresponding port pin configured as input

1 = Corresponding port pin configured as output

18.11 Port E

Port E is a 4-bit parallel port that shares its pins with the SPI module. The PTE0-PTE3 can be be configured for Direct LED drive..

Table 18-25 PTE Data Register (PTE 0x97H)

PTE			Address: 97H					
	Bit7	6	5	4	3	2	1	Bit0
Read: Write:	x	x	x	X	PTE3	PTE2	PTE1	PTE0
Reset:	u	u	u	U	u	u	u	u

Table 18-26 PTE Data Register (DDRE 0x9FH)

DDRE			Address: 9FH					
	Bit7	6	5	4	3	2	1	Bit0
Read: Write:	x	x	x	X	DDRE3	DDRE2	DDRE1	DDRE0
Reset:	0	0	0	0	0	0	0	0

0 = Corresponding port pin configured as input

1 = Corresponding port pin configured as output

Tale 18-27 PTE Port LED Control Register (LEDE 0xAFH)

LEDE			Address: AFH					
	Bit7	6	5	4	3	2	1	Bit0
Read: Write:	x	x	x	x	LEDE3	LEDE2	LEDE1	LEDE0
Reset:	0	0	0	0	0	0	0	0

0 = Corresponding port pin configured for standard drive

1 = Corresponding port pin configured for LED drive, 10mA sinking current

Note: Corresponding Direction register bit DDREx should be configured as output for LED drive.

18.12 Low-Power Modes

In PDM mode, all the GPIO pins, except LCD pins, PF, QF and SF pin, are the inputs. These pins contain an internal 30K pull-up resistor, and the I/O state is not controlled by Direction Registers in PDM mode. RX1 is also input, but it doesn't contain internal pull-up resistor.

LCD pins is the inputs and contain internal pull-up resistor if they are configured as GPIO before entering PDM mode. PF, QF, and SF are output and low in PDM mode.

19 KBI

19.1 Introduction

The ATT7025 keyboard module (KBI) provides 7 independently maskable external interrupts. When a port pin is enabled for keyboard interrupt mode, an internal 30kΩ pull-up resistor is also enabled on the pin.

Features of the KBI module include the following:

- Seven KBI pins KEYx with internal 30kΩ pull-up resistor.
- Programmable falling edge-only or falling edge- and low level- sensitive
- Not support KBI mode to exit from PDM

19.2 Function Description

Writing to the KEYIE0-KEYIE6（table 19-2）bits in the keyboard input register independently enables or disables P1 pin as a keyboard input pin. Enabling a keyboard input pin in P1 also enables its internal pull-up device.

Reset clears the keyboard interrupt request and the MODEK bit(table 19-1). Keyboard interrupt flag and KEYIE see the CPU52 interrupt int4. To determine the logic level on a keyboard interrupt pin, use the data direction register to configure the pin as an input and read the data register.

Generating **keyboard interrupt:**

A keyboard interrupt is launched when one or more keyboard pins goes low after all were high. The MODEK bit in the keyboard status and control register controls the triggering type of the keyboard interrupt.

• If the keyboard interrupt is edge-sensitive only, a falling edge on a keyboard pin does not latch an interrupt request if another keyboard pin is already low. To prevent losing an interrupt request on one pin because another pin is still low, software must deal with the latter pin while it is low.

• If the keyboard interrupt is falling edge- and low level-sensitive, an interrupt request is present as long as any keyboard pin is low.

Clearing **keyboard interrupt:**

If the MODEK bit is set, the keyboard interrupt pins are both negative edge and low-active, and all of the following actions must occur to clear a keyboard interrupt request:

• Software generate the interrupt acknowledge signal by writing a logic 1 to the ACKK bit in the keyboard status register and clear the flip-latch output.

• All of enabled keyboard interrupt pins to logic 1

• For other information, see the CPU52 int4.

If the MODEK bit is clear, the keyboard interrupt pin is falling-edge sensitive only. With ACKK is set, the keyboard interrupt request is cleared immediately.

NOTE:

Setting a keyboard interrupt enable bit (KBIEx) forces the corresponding keyboard interrupt pin P1.x to be an input, overriding the P1 direction register. However, the P1 direction register bit must be input mode for software to read the pin

19.3 Registers

Table 19-1 KEY Control Register (KEYCR 0xF7H)

KEY Control Register (KEYCR)			Address: F7H					
	Bit7	6	5	4	3	2	1	Bit0
Read:	0	0	0	0	0	0	MODEK	0
Write:	x	x	x	X	x	x		ACKK
Reset:	0	0	0	0	0	0	0	0

MODEK: Keyboard Triggering Sensitivity Bit. This read/write bit controls the triggering sensitivity of the keyboard interrupt pins.

1 = Keyboard interrupt requests on falling edges and low levels.

0 = Keyboard interrupt requests on falling edges only.

ACKK: Keyboard Acknowledge Bit. Writing a logic 1 to this write-only bit clears the keyboard interrupt request.

Table 19-2 P1 Output Multiplexing Configuration Register (KEYIE 0xADH)

KEY Interrupt Enable Register (KEYIE)			Address: ADH					
	Bit7	6	5	4	3	2	1	Bit0
Read:	0	KEYIE6	KEYIE5	KEYIE4	KEYIE3	KEYIE2	KEYIE1	KEYIE0
Write:	x							
Reset:	0	0	0	0	0	0	0	0

KEYIEx=0: P1.x/KEYx configured as GPIO: P1.x

KEYIEx=1: P1.x/KEYx configured as keyboard input: KEYx

20 PWM

20.1 Introduction

The ATT7025 PWM supports two kinds of operating modes: Tone generator and Pulse Width Modulation (PWM). Users can generate Tone waveform and PWM waveform by configuring registers.

20.2 Function Description

PWM support two kinds of operating modes: Tone generator and Pulse Width Modulation.

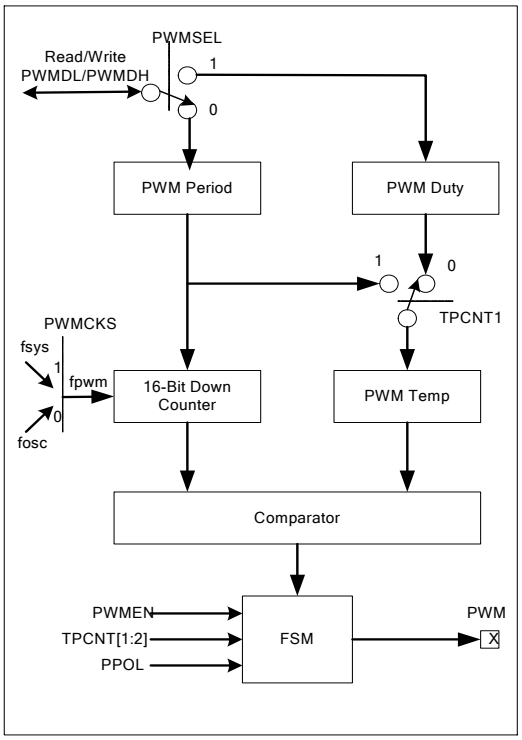


Figure 20-1 PWM module Block Diagram

Operating modes select:

TPCNT2	TPCNT1	PWMEN	Mode
X	X	0	Disable(Default)
0	0	1	PWM
0	1	1	Tone-Square
1	1	1	Tone-Staircase

The PWMEN (0xE5H.7, table 20-1) is used to enable or disable the PWM/Tone module. When PWMEN=1,the module is enabled. It can be configured as either the Tone generator or the PWM, which is selcected by TPCNT1(0xE5H.0, table 20-1), and then the PWM/TOUT pins are configured as PWM output pins.When PWMEN=0,the PWM module circuit is disabled completely.

When TPCNT1=0, it is configured as PWM mode. The PWM cycle is decided by the PWM Period register, and the PWM Duty is decided by the PWM Duty register.

When TPCNT1=1, it is configured as tone mode to generate Tone-Square or Tone-Staircase Waveform. When TPCNT2(0xE5H.1, table 20-1)=0,Tone-Square is generated,and the Duty is

50%; when TPCNT2=1,Tone-Staircase is generated.

20.2.1 Tone Generator

Support two kinds of Tone modes: Tone-Square or Tone-Staircase. Tone-Square supports two voltage output: 0V and VCC. Tone-Staircase supports three voltage outputs:0V、high resistance and VCC. In Tone-Staircase mode, the last 1/4 output of every half a cycle is high resistance.

Tone frequency expression:

$$\text{ToneFrequency} = \frac{1}{2\times(PWMPeriod[15:0]+1)\times T_{PWM}} = \frac{f_{PWM}}{2\times(PWMPeriod[15:0]+1)}$$

Tone-Square waveform figure:（PWMPeriod[15:0]=1）

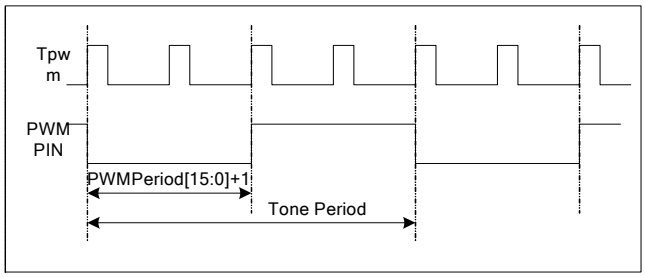
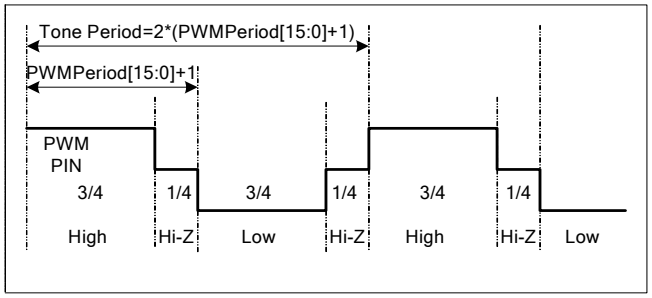


Figure 20-2 Tone-Square waveform

Tone-Staircase waveform figure:（when Period<3, output equal duty Tone-Square）



Tigure 20-3 Tone-Staircase waveform

20.2.2 Pulse Width Modulation

The PWM Period(0xE5H.5, table 20-1) register controls the PWM cycle, and the PWM Duty register controls the Duty pulse width. Users can select On Duty or Off Duty by control bit PPOL.

When PPOL=1, select Off Duty. When PPOL=0, select On Duty.

PPOL	Condition	Duty Cycle
0	0≤Duty<Period	Intermediate Value
0	Duty≥Period	100%(Always outputs high)
1	0≤Duty<Period	Intermediate Value
1	Duty≥Period	0%(Logic ‘0’)

When PPOL=0, select ON Duty

$$\text{PWMFrequency} = \frac{1}{(PWMPeriod[15:0]+1)\times T_{PWM}} = \frac{f_{PWM}}{PWMPeriod[15:0]+1}$$

$$\text{PWM ON Period} = (PWMDuty[15:0]+1)\times T_{PWM}$$

$$\text{Duty Cycle} = \frac{PWMDuty[15:0]+1}{PWMPeriod[15:0]+1}$$

While PPOL=1, select Off Duty

$$\text{Duty Cycle} = \frac{PWMPeriod[15:0]-PWMDuty[15:0]}{PWMPeriod[15:0]+1}$$

PWM waveform figure (PPOL=1, PWM Period=5, PWM Duty=1)

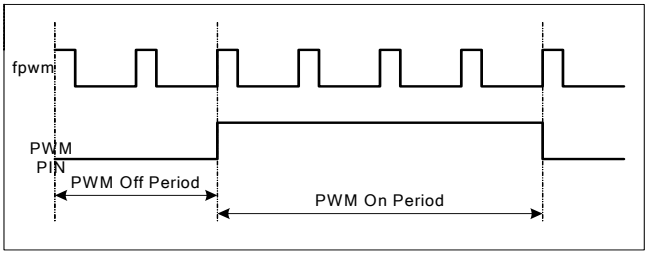


Figure 20-4 PWM waveform figure

20.3 Registers

Table 20-1 PWM Control Register (PWMCON 0xE5H)

PWM Control Register (PWMCON)			Address: E5H					
	Bit7	6	5	4	3	2	1	Bit0
Read:	PWMEN	0	PPOL	0	PWMSEL	PWMCKS	TPCNT2	TPCNT1
Write:		X		X				
Reset:	0	0	0	0	0	0	0	0

PWMEN: PWM/Tone Enable

PWMEN=1: PWM/Tone module enabled

PWMEN=0: PWM/Tone module disabled

PPOL: Duty polarity select

PPOL=0: On Duty

PPOL=1: Off Duty

PWMSEL: PWM register select

Select which register to be written/read by PWMDL/PWMDH.

PWMSEL=0: select PWM Period register

PWMSEL=1: select PWM Duty register

PWMCKS: PWM/Tone clock select

PWMCKS=0: fpwm=fosc

PWMCKS=1: fpwm=fsys

TPCNT[2:1]: PWM operating mode select

TPCNT2	TPCNT1	PWMEN	Mode
X	X	0	Disable(Default)
0	0	1	PWM
0	1	1	Tone-Square
1	1	1	Tone-Staircase

Table 20-2 PWM Low Data Register (PWMDL 0xE6H)

PWM Low Data Register (PWMDL)			Address: E6H					
	Bit7	6	5	4	3	2	1	Bit0
Read: Write:	PWMD7	PWMD6	PWMD5	PWMD4	PWMD3	PWMD2	PWMD1	PWMD0
Reset:	0	0	0	0	0	0	0	0

Table 20-3 PWM High Data Register (PWMDH 0xE7H)

PWM High Data Register (PWMDH)			Address: E7H					
	Bit7	6	5	4	3	2	1	Bit0
Read: Write:	PWMD15	PWMD14	PWMD13	PWMD12	PWMD11	PWMD10	PWMD9	PWMD8
Reset:	0	0	0	0	0	0	0	0

PWMD[15:0] is the register used to write/read the PWM Period and the PWM Duty. When PWMSEL=0, writing/reading PWMD[15:0] is to write/read the PWM Period register. When PWMSEL=1, writing/reading PWMD[15:0] is to write/read the PWM Duty register.

21 Programming Mode

21.1 Introduction

The ATT7025 includes three debug modes:

- UAM（User Application Mode）
- SFPM（Serial Flash Programming Mode）
- PFPM（Parallel Flash Programming Mode）

The ATT7025 is configured to different mode through the pin TEST/TMS1/TMS0. Table 21-1 shows the corresponding relations.

Table 21-1 programme mode selection

TEST	TMS1	TMS0	Work Mode
1	1	1	UAM mode
1	0	1	SFPM mode
1	1	0	PFPM mode
1	0	0	Reserved
0	X	X	

21.2 Function

21.2.1 UAM

It is the normal mode for user : the CPU begin execution from Flash Program Memory location 0000H after reset. If Monitor Rom is enabled(BROMEN=1) in User Mode , the Monitor Rom routines can be accessed for IAP(In-Application Programming) and OCD(On-Chip Debug) strategies.

21.2.2 FPM

There are two programming modes: parallel and serial. 2KB on-chip Monitor Rom is used during serial and parallel programming modes when it is temporarily mapped to 0000H to 07FFH. That is, after reset in FPM,The CPU52 begin execution from Monitor Rom location 0000H.

The serial programming method involve In-System Programming and UART0 is required.This method costs least resources(as shown in Figure 21-1).

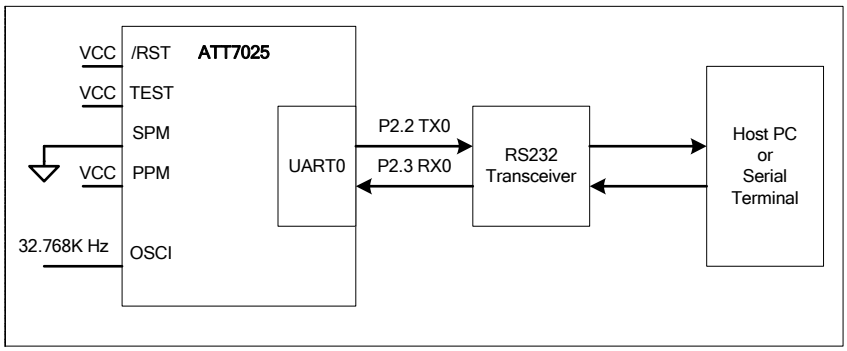


Figure 21-1 SPFM connect map

Parallel programming methods typically involve a third-party programmer. The ports PA/PB/PC as well as P2.4/P2.5/P2.7 and many other ports are required in this mode. Compared to the serial programming methods, this method is faster and always used in the factory(as shown in Figure 21-2).

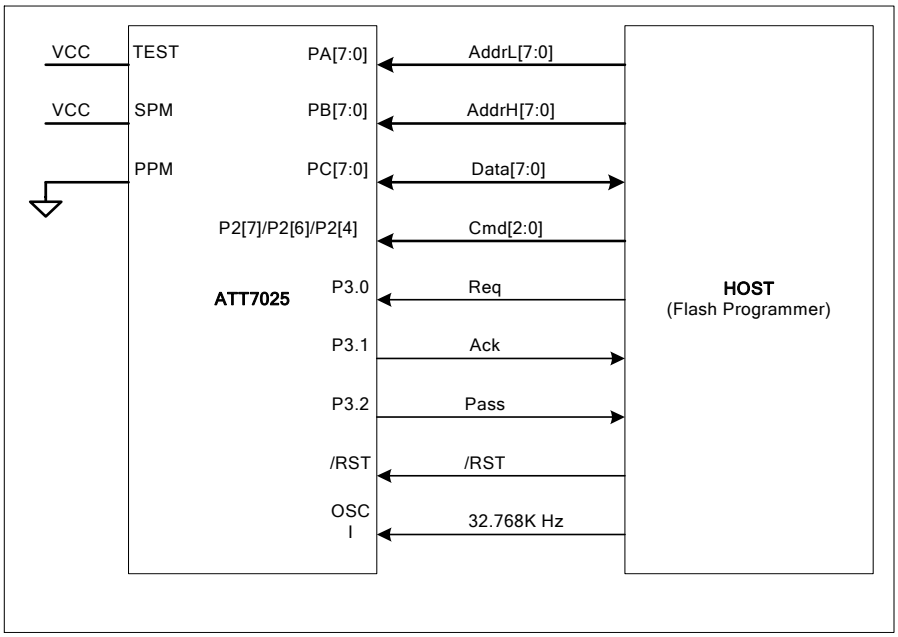


Figure 21-2 PPFM connect map

21.2.3 The mode after reset

After reset, ATT7025 run in different mode according to the different mode configurations.

The UAM mode is the main working mode provided to the user. The CPU begin execution from Flash Program Memory location 0000H.

The FPM mode is used for the system development, which involve on-line programming (ISP) and on-line debuging (OCD). The CPU52 begin execution from Memory location 0000H which is remaped for Monitor Rom. The mode is selected by the configuration of pins TEST/TMS1/TMS0 (**table 21-1)**.

NOTE: Hiterndtech provides the SDK Solutions supporting OCD and IAP functions and the solutions for the Flash Programmer. More detail is shown in <ATT7025 Develops Platform Operating instructions> and <ATT7025 Flash Programmer Operating instructions>

22 On-chip ICE (In-Circuit Emulator) support

22.1 Introduction

Three functions are supported by ICE of ATT7025:

- OCD (On-Chip Debug)
- ISP (In-System Programming)
- IAP (In-Application Programming)

.

The ICE for ATT7025 is hardware-based and mainly realized by the program in Monitor Rom. The hardware required for On-Chip ICE includes: mode-switch, hardware breadpoint and Monitor Rom.

22.2 Function Description

The ICE for ATT7025 is hardware-based and mainly realized by the program in Monitor Rom. The hardware required for On-Chip ICE of ATT7025 is described as follows:

1. Mode-switch

Two modes is provided by ATT7025:

1） UAM(User Application Mode)

It is the normal mode for user : the CPU begin execution from Flash Program Memory location 0000H after reset. If Monitor Rom is enabled (BROMEN=1) in User Mode , the Monitor Rom routines can be accessed for IAP and OCD strategies.

2） FPM(Flash Programming Mode)

There are two programming modes: parallel and serial. 2KB of on-chip Monitor Rom is used during serial and parallel programming modes when it is temporarily mapped to 0000H to 07FFH.

Serial programming methods typically involve in-system programming and UART0 is required. Parallel programming methods typically involve a third-party programmer. When ATT7025 is in parallel programming mode, its ports will be configured for parallel interface with Host Flash Programmer. The ports PA/PB/PC as well as P2.4/P2.5/P2.7 and many other ports are required in this mode. Compared to the serial programming methods, this method is faster and always used in the factory.

The SFPM(Serial Flash Programming Mode) and PFPM(Parallel Flash Programming Mode) can be configured respectively through register SPMOD（**table 22-7**）.

2. Hardware breakpoint

There are two hardware breakpoints in ATT7025. Both of them can be set in the Program Memory or the Data Memory. The interrupt vector of IRQ_OCD is 0033H.

The related registers include: HWBPL（**table 22-2**）、HWBPH（**table 22-3**）、HWBPCR（**table 22-4**） and BPSEL （**table 22-5**）。

6. Monitor Rom

In the FPM mode,the CPU52 begin execution from Flash Program Memory location 0000H

which is remaped by Monitor Rom. It detects the programming mode which is serial or parallel.. Then different subroutines will be executed to complete the analysis and operation of the programming command.

In the UAM mode, the CPU52 begin execution from Flash Program Memory location 0000H. If Monitor Rom is enabled, the Monitor Rom routines can be accessed for IAP and OCD strategies.

The Monitor Rom routines for IAP support flash memory commands such as Flash Write /Erase. The Monitor Rom routines for OCD support the basic debugging commands such as S-SingleStep, B-Breakpoint etc. They communicate with PC using UART0.

Notes :The register BROMEN （table 22-6）must be correctly configured when accessing the Monitor Rom routines.

22.3 Registers

Table 22-1 ICE register list

Address	Name	Reset Value	Function
0xE1	HWBPL	0x00	Hardware BreakPoint Low Address Register －table 22-2
0xE2	HWBPH	0x00	Hardware BreakPoint High Address Register－table 22-3
0xE3	HWBPCR	0x00	Hardware Breakpoint Control Register－table 22-4
0xF6 MCON.7	BPSEL	0	Memory Control Register－table 22-5
0xBE FMCFG.2	BROMEN	0	BOOT ROM Enable Control bit－table 22-6,write-protect
0xE9 FMCON.1	SPMOD	0	Flash Memory Control Register－table 22-7

1. Hardware BreakPoint Low Address Register

Table 22-2 Hardware BreakPoint Low Address Register (0xE1H,HWBPL)

Hardware BreakPoint Low Address Register (HWBPL)			**Address:** **E1H**					
	Bit7	**6**	**5**	**4**	**3**	**2**	**1**	**Bit0**
Read: **Write:**	BPL7	BPL6	BPL5	BPL4	BPL3	BPL2	BPL1	BPL0
Reset:	0	0	0	0	0	0	0	0

Desciption:BreakPoint Low Address. The low 8 bits of the 16bit breakpoint address.

2. Hardware BreakPoint High Address Register

Table 22-3 Hardware BreakPoint High Address Register (0xE2H,HWBPH)

Hardware BreakPoint High Address Register (HWBPH)			**Address:** **E2H**					
	Bit7	**6**	**5**	**4**	**3**	**2**	**1**	**Bit0**
Read: **Write:**	BPH7	BPH6	BPH5	BPH4	BPH3	BPH2	BPH1	BPH0
Reset:	0	0	0	0	0	0	0	0

Desciption:BreakPoint High Address;The high 8 bit of the 16 bit breakpoint address.

3．Hardware Breakpoint Control Register

Table 22-4 Hardware Breakpoint Control Register (0xE3H,HWBPCR)

Hardware Breakpoint Control Register (HWBPCR)			Address: E3H					
	Bit7	6	5	4	3	2	1	Bit0
Read:	0	0	0	0	0	0	PMSEL	BPEN
Write:	BPACK	X	X	x	X	X		
Reset:	0	0	0	0	0	0	0	0

bit	function
HWBPCR.7	BPACK:Breakpoint Acknowledge. This bit indicates that a break condition has been recognized by a hardware breakpoint register(s). Write 0: No effect. Write 1: Clear Breadpoint that selected by BPSEL
HWBPCR[6:2]	Reserved. Read: 0
HWBPCR.1	PMSEL:Program Memory Select. Write this bit to select memory for address breakpoints of register selected by BPSEL. Write 0: Break on address in data memory. Write 1: Break on address in program memory
HWBPCR.0	BPEN:breakpoint enable. Write 0: Breakpoint disabled. Write 1: Breakpoint enabled.

4．**BPSEL**

Table 22-5 Memory Control Register (0xF6H MCON.7)

Memory Control Register (MCON)			Address: F6H					
	Bit7	6	5	4	3	2	1	Bit0
Read:	BPSEL	0	0	0	0	0	0	RAMMAP
Write:		X	X	x	X	X	X	
Reset:	0	0	0	0	0	0	0	0

BPSEL:Breakpoint Address Selection.

Write: Select one of two Breakpoint registers: 0 or 1.

Read: Provides the Breakpoint register that created the last interrupt: 0 or 1.

5．**BROMEN（writen-protect）**

Table 22-6 BOOT ROM enable control bit(0xBEH FMCFG.2)

FMCFG			Address: BEH					
	Bit7	6	5	4	3	2	1	Bit0
Read:	DFS2	DFS1	DFS0	0	0	BROMEN	PMLOCK	RSLOCK
Write:				X	X			
Reset:	0	0	0	0	0	0	0	0

BROMEN:Boot Rom enable;

Write 0: Boot Rom routines can not be accessed .

Write 1: Boot Rom routines can be accessed .

6．**SPMOD**

Table 22-7 FPM mode state bit (0xF6H MCON.7)

Flash Memory Control Register (FMCON)			Address: E9H					
	Bit7	6	5	4	3	2	1	Bit0
Read:	PS1MAP	FOP1	FOP0	MMAP	FMAP	BUSY	SPMOD	0
Write:				X		X	X	X
Reset:	0	0	0	0	0	0	0	0

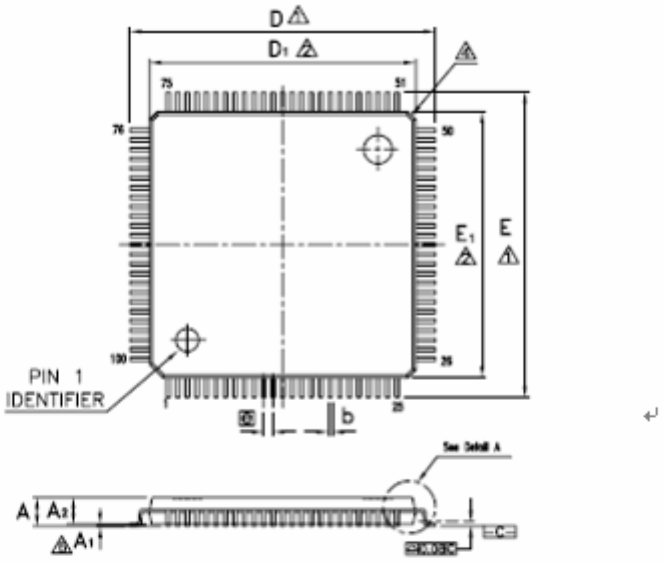
SPMOD:Serial/Parallel Mode

Write 0: The Parallel FPM mode ;

Write 1: The Serial FPM mode .

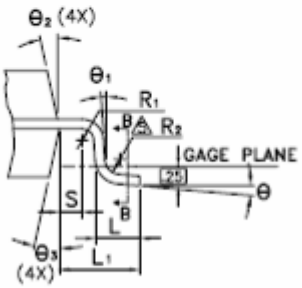
23 Package Diagrams

ATT7025: **Lead Free** QFP100

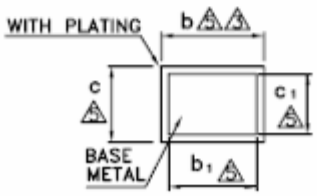


NOTE :

1. TO BE DETERMINED AT SEATING PLANE C .
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.
4. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
5. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm AND 0.25 mm FROM THE LEAD TIP.
6. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
7. CONTROLLING DIMENSION : MILLIMETER.
8. REFERENCE DOCUMENT : JEDEC MS-026 , BED.



DETAIL A



SECTION B-B

Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.22	0.27	0.007	0.009	0.011
b1	0.17	0.20	0.23	0.007	0.008	0.009
c	0.09	—	0.20	0.004	—	0.008
c1	0.09	—	0.16	0.004	—	0.006
D	15.85	16.00	16.15	0.624	0.630	0.636
D1	13.90	14.00	14.10	0.547	0.551	0.555
E	15.85	16.00	16.15	0.624	0.630	0.636
E1	13.90	14.00	14.10	0.547	0.551	0.555
e	0.50 BSC			0.020 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
R1	0.08	—	—	0.003	—	—
R2	0.08	—	0.20	0.003	—	0.008
S	0.20	—	—	0.008	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	—	—	0°	—	—
θ2	12°TYP			12°TYP		
θ3	12°TYP			12°TYP		