

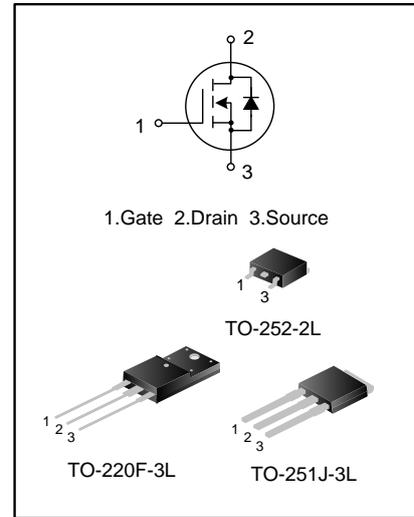
4A, 650V DP MOS POWER TRANSISTOR

GENERAL DESCRIPTION

SVS4N65F/MJ/D is an N-channel enhancement mode high voltage power MOSFETs produced using the new platform of Silan's DP MOS technology. It achieves low conduction loss and switching losses. It leads the design engineers to their power converters with high efficiency, high power density, and superior thermal behavior. Furthermore, it's universal applicable, i.e., suitable for hard and soft switching topologies.

FEATURES

- ◆ 4A, 650V, $R_{DS(on)(typ)}=0.95\Omega@V_{GS}=10V$
- ◆ New revolutionary high voltage technology
- ◆ Ultra low gate charge
- ◆ Extreme dv/dt rated
- ◆ High peak current capability



ORDERING INFORMATION

| Part No. | Package | Marking | Material | Packing |
|------------|------------|-----------|--------------|-------------|
| SVS4N65F | TO-220F-3L | SVS4N65F | Halogen free | Tube |
| SVS4N65MJ | TO-251J-3L | SVS4N65MJ | Halogen free | Tube |
| SVS4N65D | TO-252-2L | SVS4N65D | Halogen free | Tube |
| SVS4N65DTR | TO-252-2L | SVS4N65D | Halogen free | Tape & Reel |

ABSOLUTE MAXIMUM RATINGS ($T_C=25^\circ\text{C}$ unless otherwise noted)

| Characteristics | Symbol | Ratings | | | Unit |
|---|-----------|-------------------------|-----------|----------|---------------------|
| | | SVS4N65F | SVS4N65MJ | SVS4N65D | |
| Drain-Source Voltage | V_{DS} | 650 | | | V |
| Gate-Source Voltage | V_{GS} | ± 30 | | | V |
| Drain Current | I_D | $T_C=25^\circ\text{C}$ | | | A |
| | | $T_C=100^\circ\text{C}$ | | | |
| Drain Current Pulsed | I_{DM} | 12 | | | A |
| Power Dissipation($T_C=25^\circ\text{C}$) -Derate above 25°C | P_D | 30 | 42 | 39 | W |
| | | 0.24 | 0.34 | 0.31 | W/ $^\circ\text{C}$ |
| Single Pulsed Avalanche Energy (Note 1) | E_{AS} | 118 | | | mJ |
| Operation Junction Temperature Range | T_J | -55~+150 | | | $^\circ\text{C}$ |
| Storage Temperature Range | T_{stg} | -55~+150 | | | $^\circ\text{C}$ |

THERMAL CHARACTERISTICS

| Characteristics | Symbol | Ratings | | | Unit |
|---|-----------------|----------|-----------|----------|----------------------|
| | | SVS4N65F | SVS4N65MJ | SVS4N65D | |
| Thermal Resistance, Junction-to-Case | $R_{\theta JC}$ | 4.17 | 2.98 | 3.21 | $^{\circ}\text{C/W}$ |
| Thermal Resistance, Junction-to-Ambient | $R_{\theta JA}$ | 120 | 110 | 110 | $^{\circ}\text{C/W}$ |

ELECTRICAL CHARACTERISTICS ($T_C=25^{\circ}\text{C}$ unless otherwise noted)

| Characteristics | Symbol | Test conditions | Min. | Typ. | Max. | Unit |
|---|--------------|--|------|------|-----------|----------|
| Drain -Source Breakdown Voltage | B_{VDSS} | $V_{GS}=0V, I_D=250\mu A$ | 650 | -- | -- | V |
| Drain-Source Leakage Current | I_{DSS} | $V_{DS}=650V, V_{GS}=0V$ | -- | -- | 1.0 | μA |
| Gate-Source Leakage Current | I_{GSS} | $V_{GS}=\pm 30V, V_{DS}=0V$ | -- | -- | ± 100 | nA |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{GS}=V_{DS}, I_D=250\mu A$ | 2.0 | -- | 4.0 | V |
| Static Drain-Source On State Resistance | $R_{DS(on)}$ | $V_{GS}=10V, I_D=2A$ | -- | 0.95 | 1.2 | Ω |
| Input Capacitance | C_{iss} | $V_{DS}=100V, V_{GS}=0V,$ $f=1.0\text{MHz}$ | -- | 318 | -- | pF |
| Output Capacitance | C_{oss} | | -- | 30.4 | -- | |
| Reverse Transfer Capacitance | C_{rss} | | -- | 0.65 | -- | |
| Turn-on Delay Time | $t_{d(on)}$ | $V_{DD}=325V, I_D=4.0A,$ $V_{GS}=10V, R_G=10\Omega$ (Note 2,3) | -- | 8.0 | -- | ns |
| Turn-on Rise Time | t_r | | -- | 24.2 | -- | |
| Turn-off Delay Time | $t_{d(off)}$ | | -- | 30.1 | -- | |
| Turn-off Fall Time | t_f | | -- | 25.3 | -- | |
| Total Gate Charge | Q_g | $V_{DS}=520V, I_D=4.0A,$ $V_{GS}=10V$ (Note 2,3) | -- | 11.9 | -- | nC |
| Gate-Source Charge | Q_{gs} | | -- | 2.25 | -- | |
| Gate-Drain Charge | Q_{gd} | | -- | 6.43 | -- | |

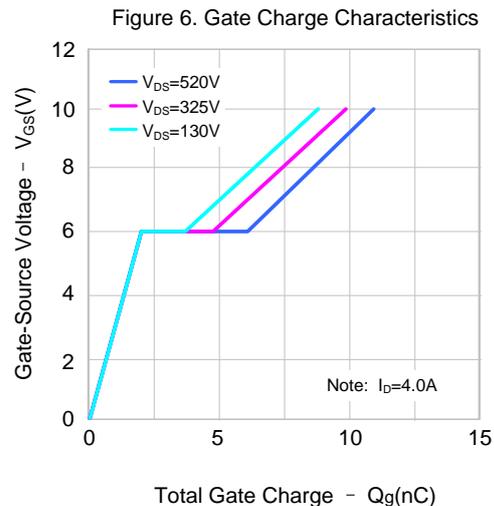
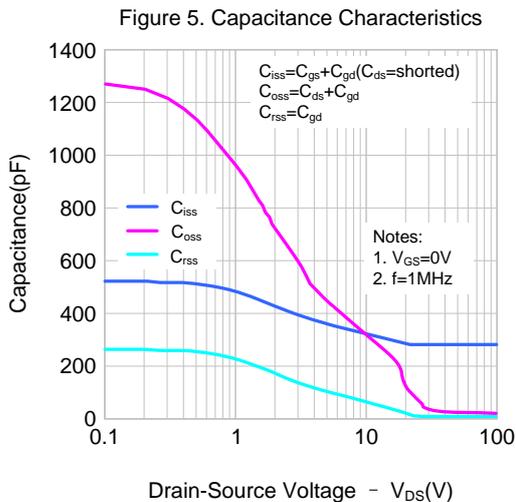
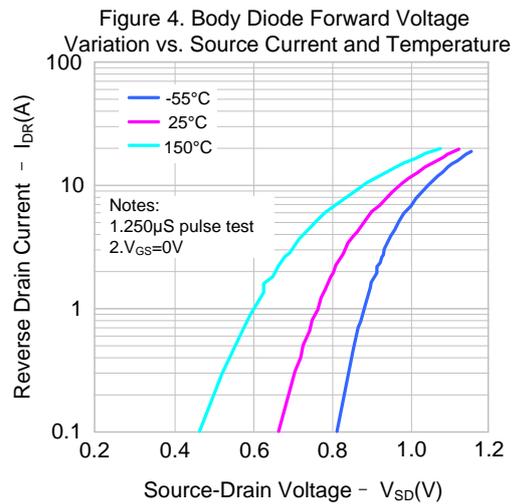
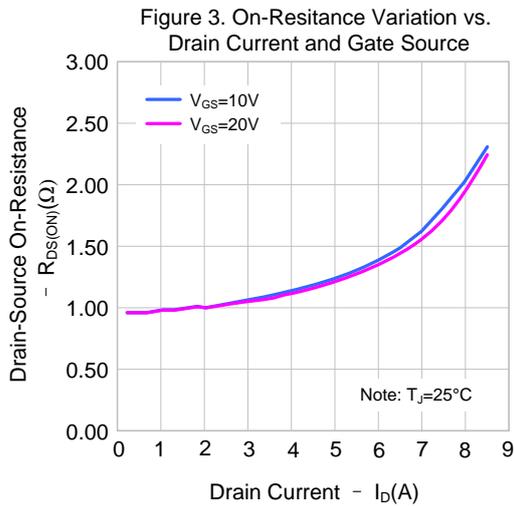
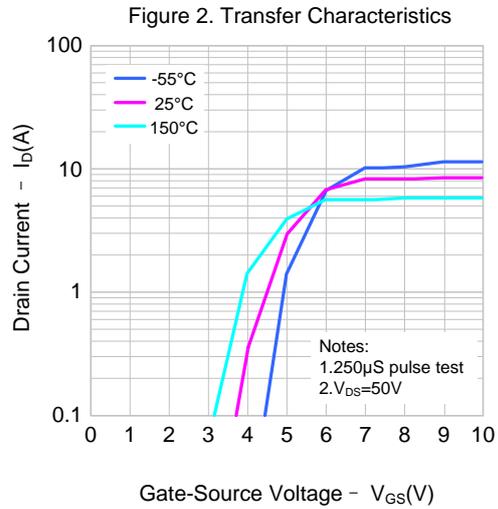
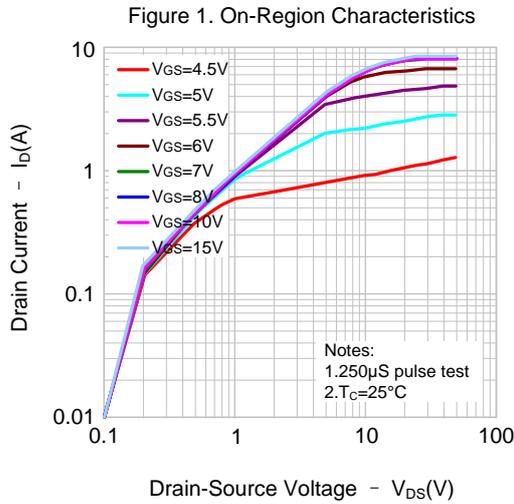
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

| Characteristics | Symbol | Test conditions | Min. | Typ. | Max. | Unit |
|---------------------------|----------|---|------|------|------|---------|
| Continuous Source Current | I_S | Integral Reverse P-N Junction Diode in the MOSFET | -- | -- | 4.0 | A |
| Pulsed Source Current | I_{SM} | | -- | -- | 12 | |
| Diode Forward Voltage | V_{SD} | $I_S=4.0A, V_{GS}=0V$ | -- | -- | 1.4 | V |
| Reverse Recovery Time | T_{rr} | $I_S=4.0A, V_{GS}=0V,$ $di_f/dt=100A/\mu s$ | -- | 280 | -- | ns |
| Reverse Recovery Charge | Q_{rr} | | -- | 2.03 | -- | μC |

Notes:

1. $L=30\text{mH}, I_{AS}=2.8A, V_{DD}=100V, R_G=25\Omega,$ starting $T_J=25^{\circ}\text{C};$
2. Pulse Test: Pulse width $\leq 300\mu s,$ Duty cycle $\leq 2\%;$
3. Essentially independent of operating temperature.

TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS(continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

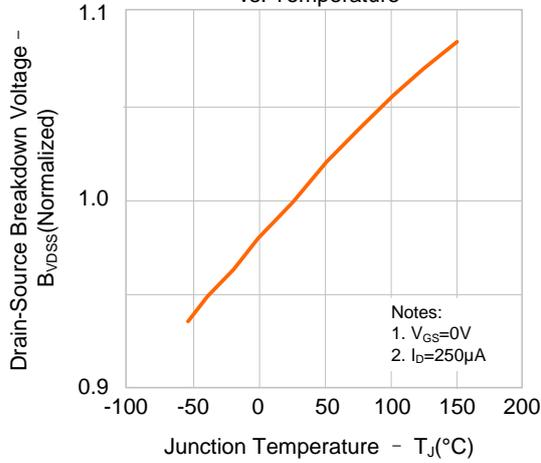


Figure 8. On-resistance Variation vs. Temperature

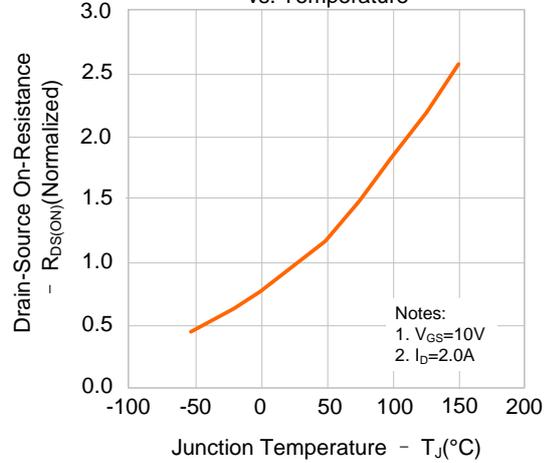


Figure 9-1. Max. Safe Operating Area(SVS4N65F)

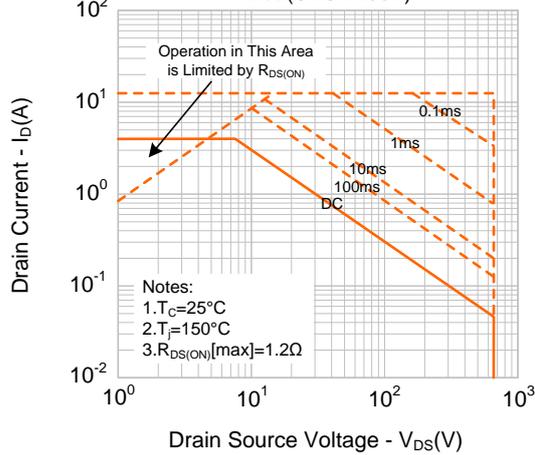


Figure 9-2. Max. Safe Operating Area(SVS4N65MJ)

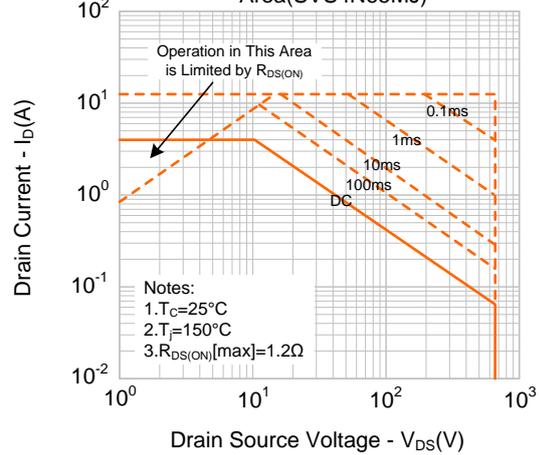
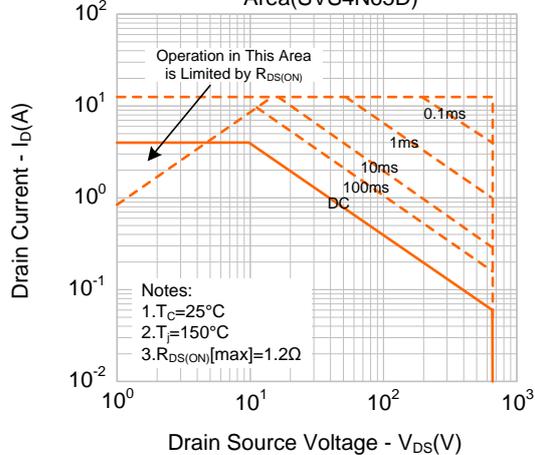
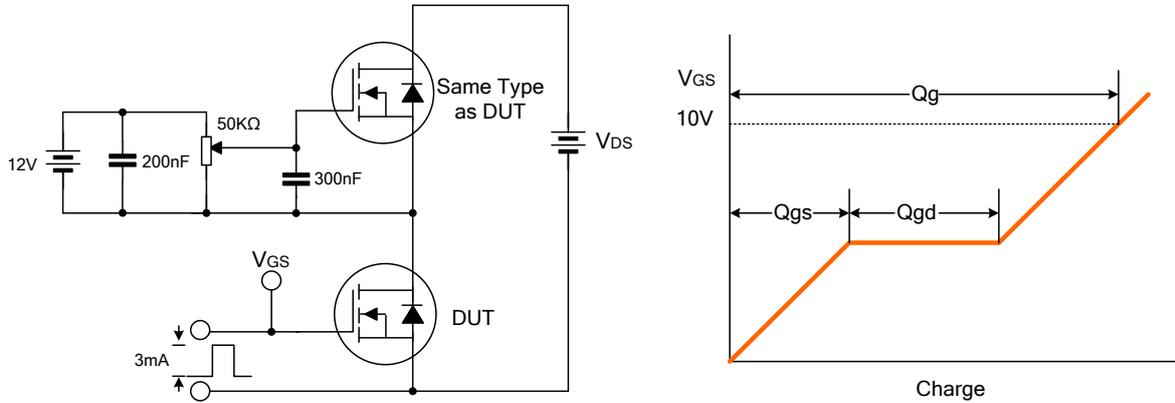


Figure 9-3. Max. Safe Operating Area(SVS4N65D)

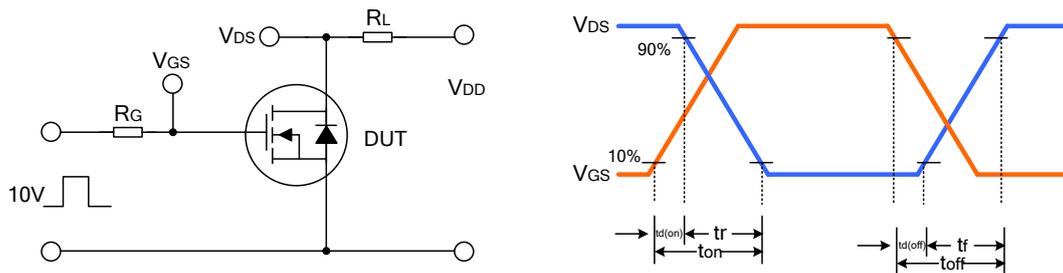


TYPICAL TEST CIRCUIT

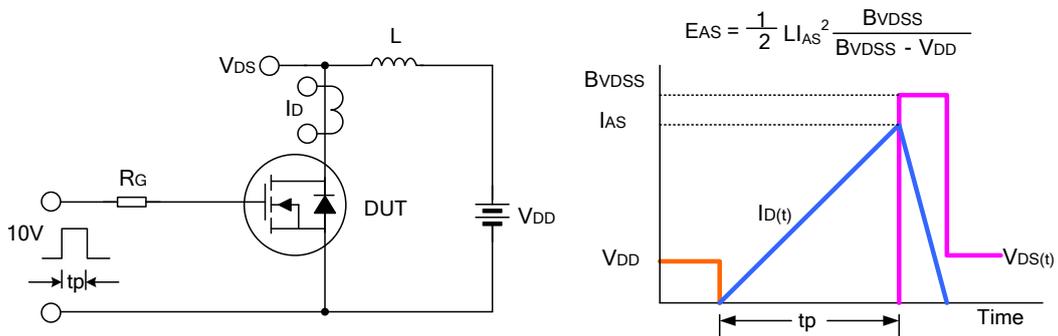
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveform



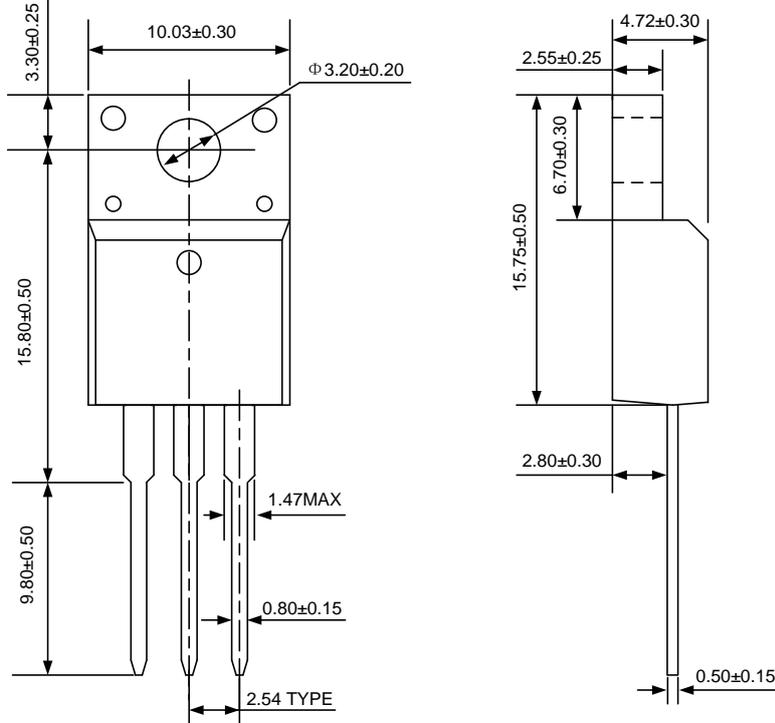
Unclamped Inductive Switching Test Circuit & Waveform



PACKAGE OUTLINE

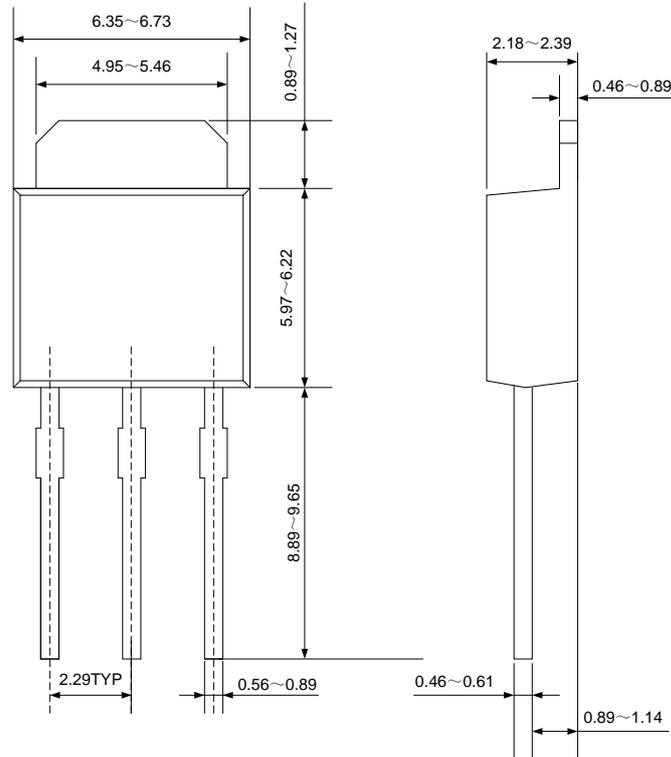
TO-220F-3L

UNIT: mm



TO-251J-3L

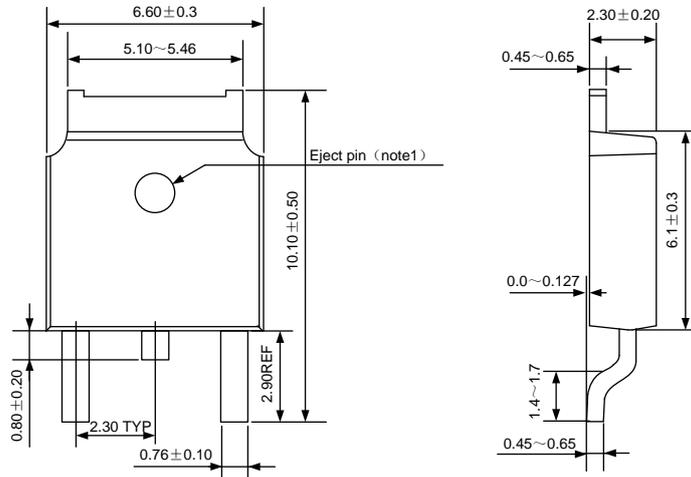
UNIT: mm



PACKAGE OUTLINE (continued)

TO-252-2L

UNIT: mm



NOTE1 : There are two conditions for this position:has an eject pin or has no eject pin.

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|------------|---|----------------|---|
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|-------|-----|---------|--------|
| Rev.: | 1.0 | Author: | Yin Zi |
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Revision History:

1. First release
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