

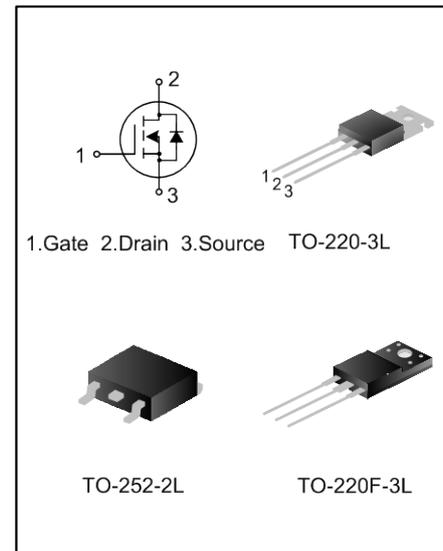
## 6A, 800V DP MOS POWER TRANSISTOR

### DESCRIPTION

SVS6N80T/D/F is an N-channel enhancement mode high voltage power MOSFETs produced using the new platform of Silan's DP MOS technology. It achieves low conduction loss and switching losses. It leads the design engineers to their power converters with high efficiency, high power density, and superior thermal behavior. Furthermore, it's universal applicable, i.e., suitable for hard and soft switching topologies.

### FEATURES

- ◆ 6A,800V,  $R_{DS(on)(typ.)}=0.8\Omega@V_{GS}=10V$
- ◆ New revolutionary high voltage technology
- ◆ Ultra low gate charge
- ◆ Periodic avalanche rated
- ◆ Extreme dv/dt rated
- ◆ High peak current capability



### ORDERING INFORMATION

Part No.	Package	Marking	Material	Packing
SVS6N80T	TO-220-3L	SVS6N80T	Pb free	Tube
SVS6N80D	TO-252-2L	SVS6N80D	Halogen free	Tube
SVS6N80DTR	TO-252-2L	SVS6N80D	Halogen free	Tape & Reel
SVS6N80F	TO-220F-3L	SVS6N80F	Pb free	Tube

### ABSOLUTE MAXIMUM RATINGS (Unless otherwise noted, $T_C=25^\circ\text{C}$ )

Characteristics	Symbol	Ratings			Unit
		SVS6N80T	SVS6N80D	SVS6N80F	
Drain-Source Voltage	$V_{DS}$	800			V
Gate-Source Voltage	$V_{GS}$	$\pm 30$			V
Drain Current	$T_C=25^\circ\text{C}$	6.0			A
	$T_C=100^\circ\text{C}$	4			
Drain Current Pulsed	$I_{DM}$	24			A
Power Dissipation ( $T_C=25^\circ\text{C}$ ) - Derate above $25^\circ\text{C}$	$P_D$	110	82	33	W
		0.88	0.66	0.26	
Single Pulsed Avalanche Energy (Note 1)	$E_{AS}$	250			mJ
Operation Junction Temperature Range	$T_J$	-55~+150			$^\circ\text{C}$
Storage Temperature Range	$T_{stg}$	-55~+150			$^\circ\text{C}$

## THERMAL CHARACTERISTICS

Characteristics	Symbol	Ratings			Unit
		SVS6N80T	SVS6N80D	SVS6N80F	
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	1.14	1.52	3.79	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	62.5	62.0	62.5	°C/W

## ELECTRICAL CHARACTERISTICS (Unless otherwise noted, $T_c=25^\circ\text{C}$ )

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Drain -Source Breakdown Voltage	$B_{VDSS}$	$V_{GS}=0V, I_D=250\mu A$	800	--	--	V
Drain-Source Leakage Current	$I_{DSS}$	$V_{DS}=800V, V_{GS}=0V$	--	--	1.0	$\mu A$
Gate-Source Leakage Current	$I_{GSS}$	$V_{GS}=\pm 30V, V_{DS}=0V$	--	--	$\pm 100$	nA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS}=V_{DS}, I_D=250\mu A$	2.0	--	4.0	V
Static Drain- Source On State Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=3A$	--	0.8	0.95	$\Omega$
Input Capacitance	$C_{iss}$	$f=1\text{MHz}, V_{GS}=0V, V_{DS}=100V$	--	474.7	--	pF
Output Capacitance	$C_{oss}$		--	23.2	--	
Reverse Transfer Capacitance	$C_{rss}$		--	3.3	--	
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=400V, V_{GS}=10V, R_G=4.7\Omega, I_D=6A$ (Note 2,3)	--	9.3	--	ns
Turn-on Rise Time	$t_r$		--	22.7	--	
Turn-off Delay Time	$t_{d(off)}$		--	42.3	--	
Turn-off Fall Time	$t_f$		--	25.6	--	
Total Gate Charge	$Q_g$	$V_{DD}=640V, V_{GS}=10V, I_D=6A$ (Note 2,3)	--	24.3	--	nC
Gate-Source Charge	$Q_{gs}$		--	2.8	--	
Gate-Drain Charge	$Q_{gd}$		--	14.9	--	

## SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Continuous Source Current	$I_S$	Integral Reverse P-N Junction Diode in the MOSFET	--	--	6.0	A
Pulsed Source Current	$I_{SM}$		--	--	24	
Diode Forward Voltage	$V_{SD}$	$I_S=6.0A, V_{GS}=0V$	--	--	1.4	V
Reverse Recovery Time	$T_{rr}$	$I_S=6.0A, V_{GS}=0V, dI_F/dt=100A/\mu s$	--	398.6	--	ns
Reverse Recovery Charge	$Q_{rr}$		--	3.5	--	$\mu C$

### Notes:

- $L=79\text{mH}, I_{AS}=2.4A, V_{DD}=100V, R_G=25\Omega$ , starting  $T_J=25^\circ\text{C}$ ;
- Pulse Test: Pulse width  $\leq 300\mu s$ , Duty cycles  $\leq 2\%$ ;
- Essentially independent of operating temperature.

**TYPICAL CHARACTERISTICS**

Figure 1. On-Region Characteristics

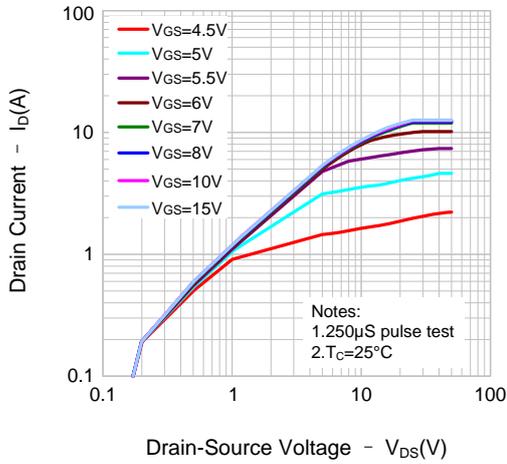


Figure 2. Transfer Characteristics

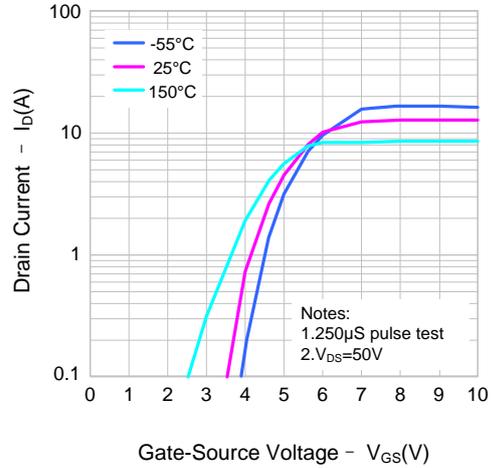


Figure 3. On-Resistance Variation vs. Drain Current

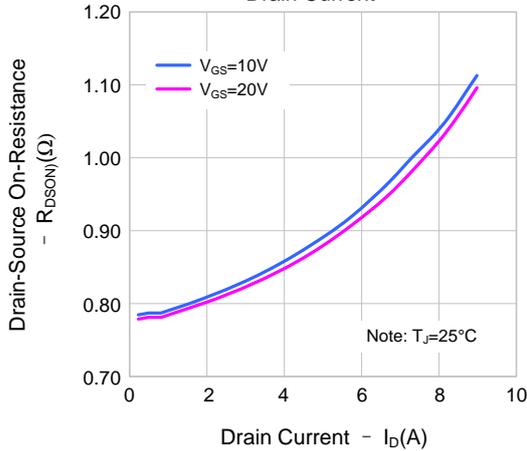


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

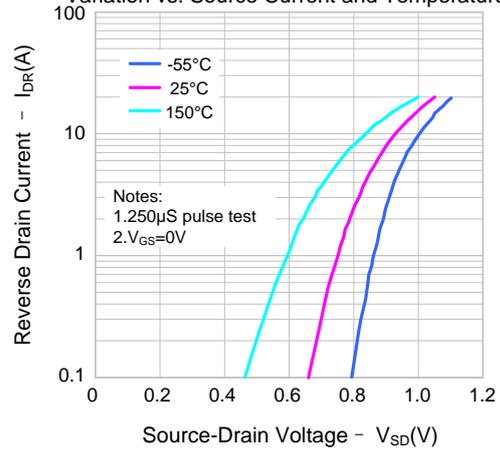


Figure 5. Capacitance Characteristics

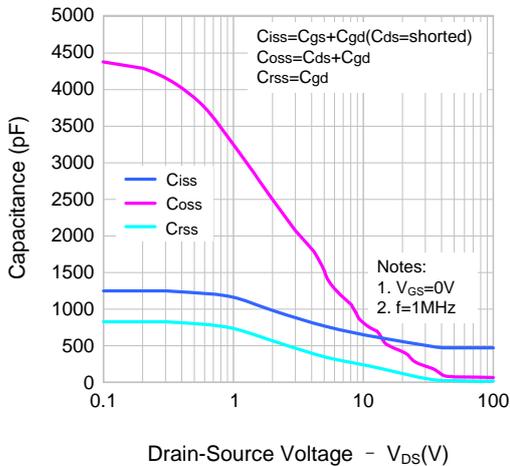
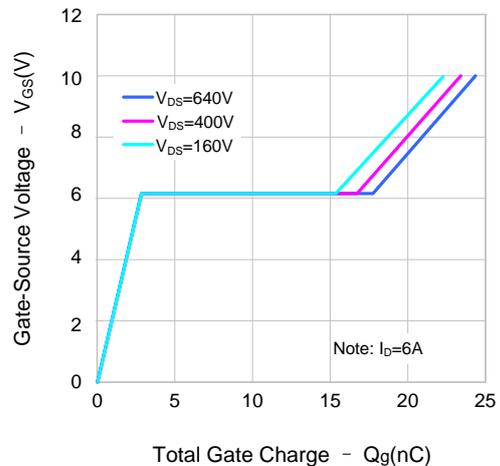


Figure 6. Gate Charge Characteristics



**TYPICAL CHARACTERISTICS (continued)**

Figure 7. Breakdown Voltage Variation vs. Temperature

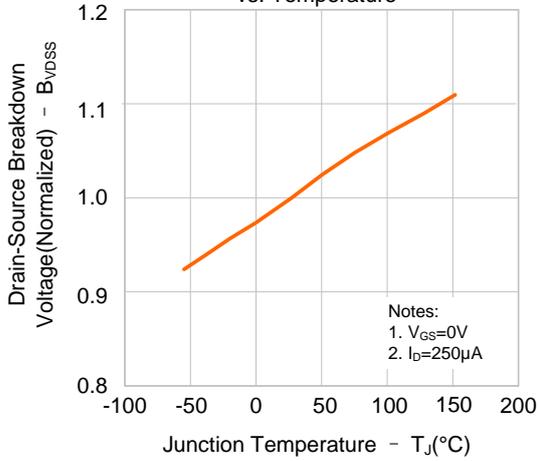


Figure 8. On-resistance Variation vs. Temperature

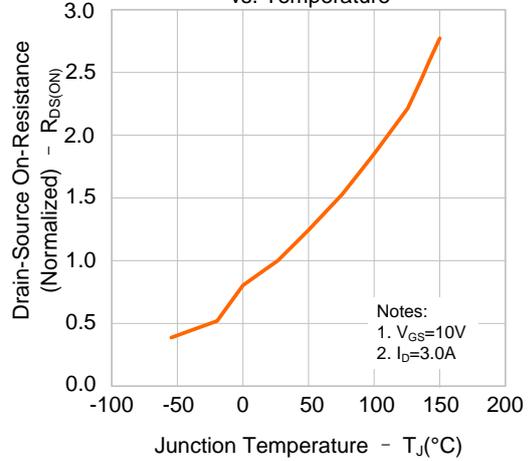


Figure 9-1. Max. Safe Operating Area (SVS6N80T)

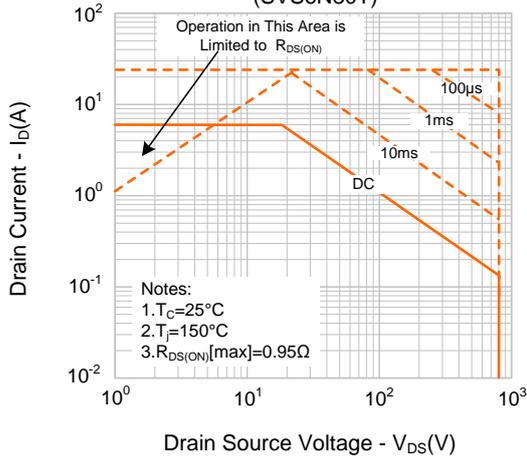


Figure 9-2. Max. Safe Operating Area (SVS6N80D)

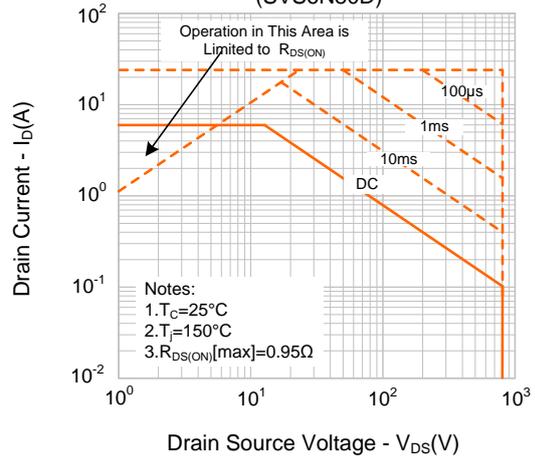
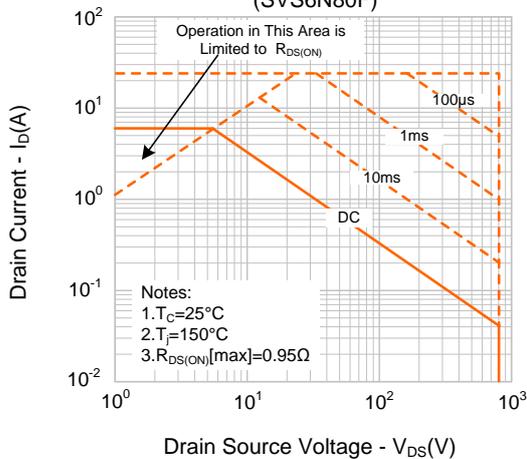
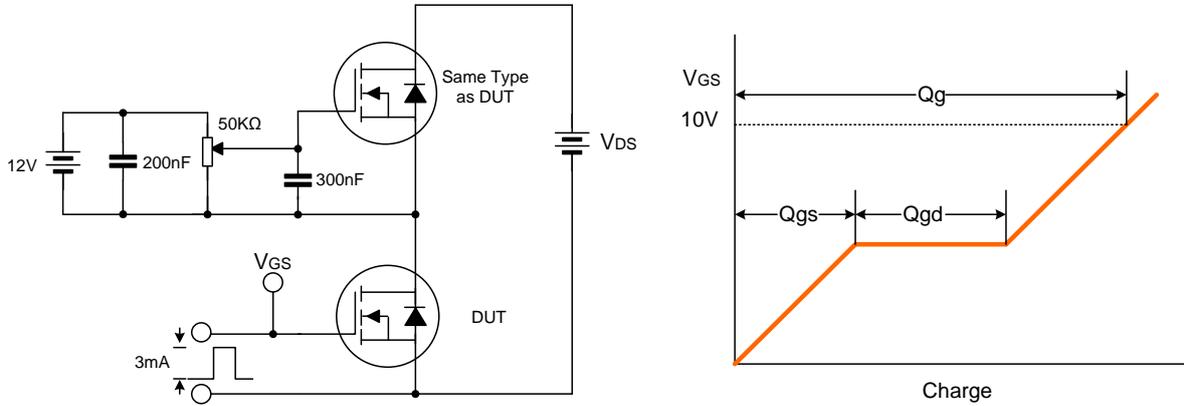


Figure 9-3. Max. Safe Operating Area (SVS6N80F)

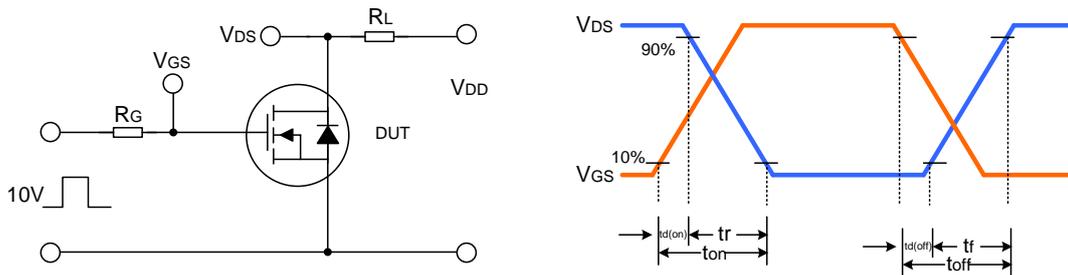


**TYPICAL TEST CIRCUIT**

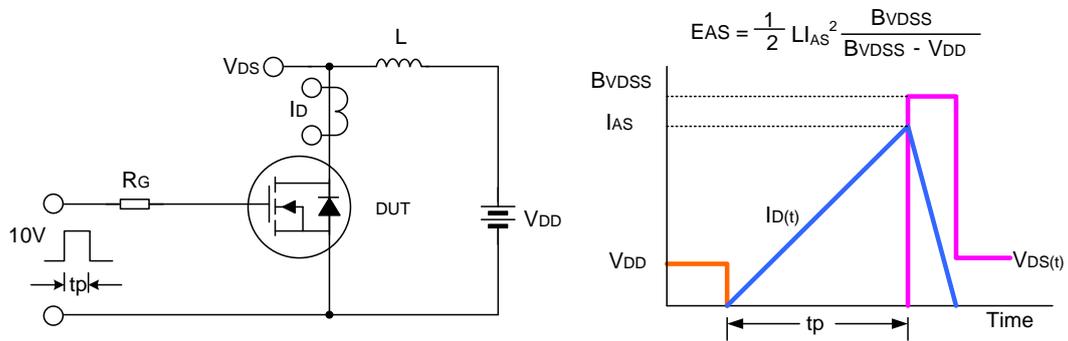
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveform



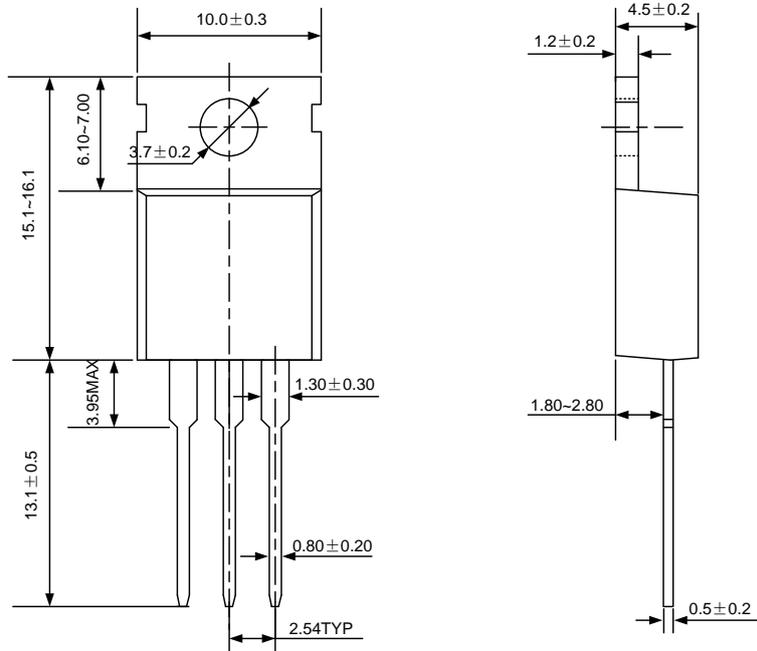
Unclamped Inductive Switching Test Circuit & Waveform



**PACKAGE OUTLINE**

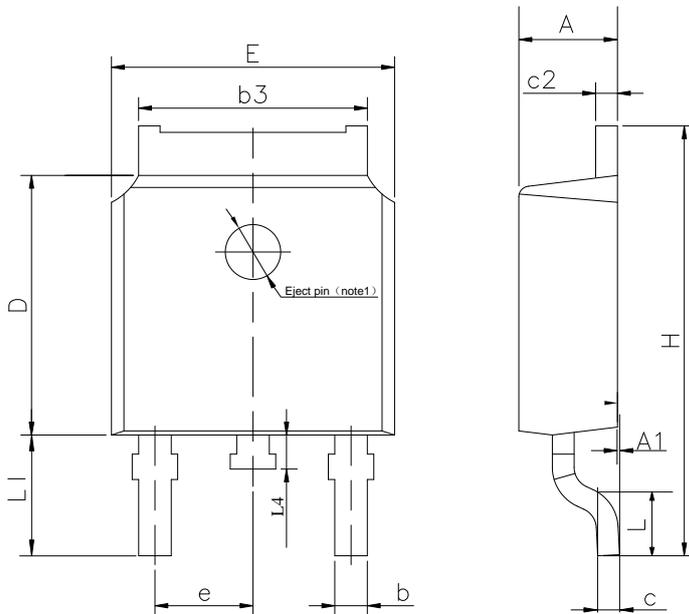
**TO-220-3L**

**UNIT: mm**



**TO-252-2L**

**UNIT: mm**



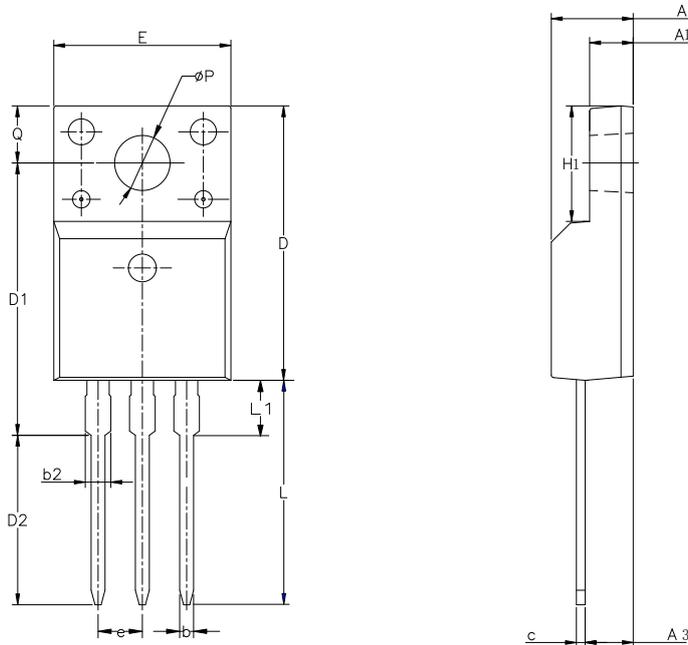
SYMBOL	MIN	NOM	MAX
A	2.10	2.30	2.50
A1	0	---	0.127
b	0.66	0.76	0.89
b3	5.10	5.33	5.46
c	0.45	---	0.65
c2	0.45	---	0.65
D	5.80	6.10	6.40
E	6.30	6.60	6.90
e	2.30TYP		
H	9.60	10.10	10.60
L	1.40	1.50	1.70
L1	2.90REF		
L4	0.60	0.80	1.00

NOTE1 : There are two conditions for this position:has an eject pin or has no eject pin.

PACKAGE OUTLINE(continued)

TO-220F-3L

UNIT: mm



SYMBOL	MIN	NOM	MAX
A	4.42	4.70	5.02
A1	2.30	2.54	2.80
A3	2.50	2.76	3.10
b	0.70	0.80	0.90
b2	—	—	1.47
c	0.35	0.50	0.65
D	15.25	15.87	16.25
D1	15.30	15.75	16.30
D2	9.30	9.80	10.30
E	9.73	10.16	10.36
e	2.54BCS		
H1	6.40	6.68	7.00
L	12.48	12.98	13.48
L1	/	/	3.50
$\phi P$	3.00	3.18	3.40
Q	3.05	3.30	3.55

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Rev.:	1.1	Author:	Yin Zi
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Revision History:

1. Add the package of TO-252-2L
2. Add the package of TO-220F-3L
3. Modify the typical characteristics
4. Modify the ordering information

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Rev.:	1.0	Author:	Yin Zi
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Revision History:

1. First release
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