

M5M2167P-55, -70

16384-BIT (16384-WORD BY 1-BIT) STATIC RAM

DESCRIPTION

This is a family of 16384-word by 1-bit static RAMs, fabricated with the high-performance N-channel silicon-gate MOS process and designed for high-speed application. These devices operate on a single 5V supply, and are directly TTL compatible. They include a power-down feature as well.

FEATURES

- Fast access time
M5M2167P-55.....55 ns (max)
M5M2167P-70.....70 ns (max)
- Low power dissipation
Active.....400 mW (typ)
Standby by.....40 mW (typ)
- Power down by \bar{S}
- Single 5V power supply
- Fully static operation
Requires neither external clock nor refreshing
- All inputs and output are directly TTL compatible
- Easy memory expansion by chip-select (\bar{S}) input
- Interchangeable with Intel's 2167

APPLICATION

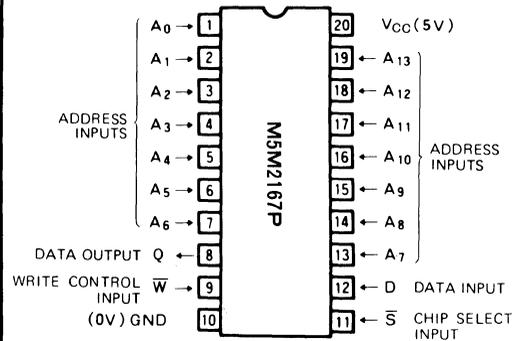
- High-speed memory systems

FUNCTION

A write operation is executed during the \bar{S} low and \bar{W} low overlap time. In this period, address signals must be stable. When \bar{W} is low, the Q terminal is maintained in the high impedance state, so it is possible to connect D and Q terminals directly.

In a read operation, after setting \bar{W} to high, and \bar{S} to low if the address signals are stable, the data is available at the Q terminal.

PIN CONFIGURATION (TOP VIEW)

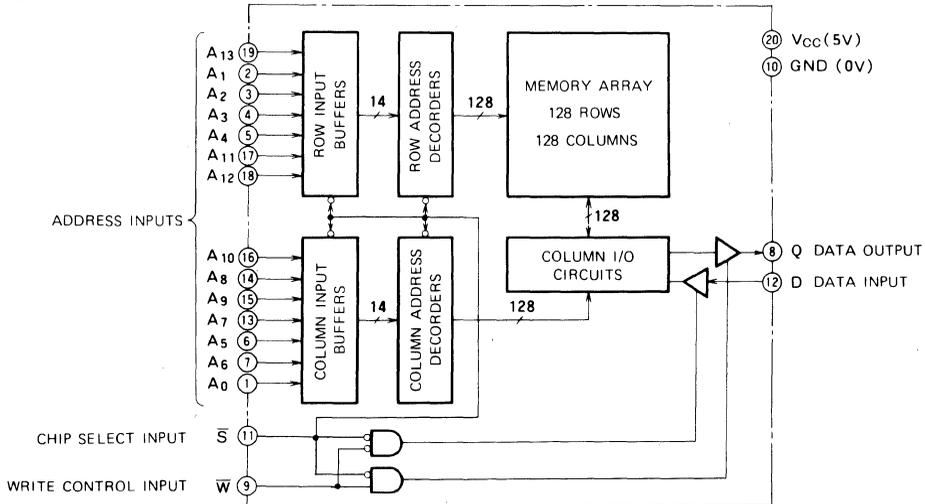


Outline 20 P4

When \bar{S} is high, the chip is in the non-selectable state, disabling both reading and writing. In this case the output is in the floating (high-impedance) state, useful for OR-ties with other devices.

Signal \bar{S} controls the power-down feature. When \bar{S} goes high, power dissipation is reduced to 1/10 of active power. The access time from \bar{S} is equivalent to the address access time.

BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Limits	Unit
V _{CC}	Supply voltage	With respect to GND	-3.5 ~ 7	V
V _I	Input voltage		-3.5 ~ 7	V
V _O	Output voltage		-3.5 ~ 7	V
P _d	Maximum power dissipation		1	W
T _{opr}	Temperature under bias		-10 ~ 85	°C
T _{stg}	Storage temperature		-65 ~ 150	°C

RECOMMENDED OPERATING CONDITIONS (T_a = 0 ~ 70°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V _{CC}	Supply voltage	4.5	5	5.5	V
V _{IL}	Low-level input voltage	-3		0.8	V
V _{IH}	High-level input voltage	2		6	V

Necessary airflow cooling >2m/s

ELECTRICAL CHARACTERISTICS (T_a = 0 ~ 70°C, V_{CC} = 5V ± 10%, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V _{IH}	High-level input voltage		2		6	V
V _{IL}	Low-level input voltage		-3		0.8	V
V _{OH}	High-level output voltage	I _{OH} = -4 mA	2.4			V
V _{OL}	Low-level output voltage	I _{OL} = 8 mA			0.4	V
I _I	Input current	V _I = 0 ~ 5.5 V			10	μA
I _{OZ}	Off-state output current	V _I (\bar{S}) = 2V, V _O = 0 ~ V _{CC}			50	μA
I _{CC1}	Supply current from V _{CC}	V _I (\bar{S}) = 0.8V Output open		T _a = 25°C T _a = 0°C	80 125	mA
I _{CC2}	Stand by current	V _I (\bar{S}) = 2V output open			8 30	mA
I _{PO}	Peak power-on current	V _{CC} = 0 ~ 4.5V V _I (\bar{S}) = Lower of V _{CC} or V _{IH min}			30	mA
C _I	Input capacitance	V _I = GND, V _I = 25mVrms, f = 1MHz			5	pF
C _O	Output capacitance	V _O = GND, V _O = 25mVrms, f = 1MHz			6	pF

Note 1. Current flow into an IC is positive, out is negative.

SWITCHING CHARACTERISTICS (FOR READ CYCLE) (T_a = 0 ~ 70°C, V_{CC} = 5V ± 10%, unless otherwise noted)

Symbol	Parameter	M5M2167P-55			M5M2167P-70			Unit
		Min	Typ	Max	Min	Typ	Max	
t _{CR}	Read cycle time	55			70			ns
t _{a(A)}	Address access time			55			70	ns
t _{a(S)}	Chip select access time			55			70	ns
t _{V(A)}	Data valid time after address	5			5			ns
t _{en(S)}	Output enable time after chip selection	10			10			ns
t _{dis(S)}	Output disable time after chip deselection	0		25	0		30	ns
t _{PU}	Power-up time after chip selection	0			0			ns
t _{PD}	Power down time after chip deselection			30			40	ns

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TIMING REQUIREMENTS (FOR WRITE CYCLE) ($T_a = 0 \sim 70^\circ\text{C}$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted)

Symbol	Parameter	M5M2167P-55			M5M2167P-70			Unit
		Min	Typ	Max	Min	Typ	Max	
t_{CW}	Write cycle time	55			70			ns
$t_{SU(S)}$	Chip select setup time	50			60			ns
$t_{SU(A)_1}$	Address setup time 1 (\overline{W} CONTROL)	5			5			ns
$t_{SU(A)_2}$	Address setup time 2 (\overline{S} CONTROL)	0			0			ns
$t_{W(W)}$	Write pulse width	35			40			ns
$t_{rec(W)}$	Write recovery time	5			5			ns
$t_{SU(D)}$	Data setup time	25			30			ns
$t_H(D)$	Data hold time	0			0			ns
$t_{dis(W)}$	Output disable time after \overline{W} low	0		25	0		30	ns
$t_{en(W)}$	Output enable time after \overline{W} high	0			0			ns
$t_{su(A-\overline{WH})}$	Address to \overline{W} high	40			45			ns

CONDITIONS

Input pulse levels 0 to 3V
 input rise and falltime 5 ns
 Input timing reference level 1.5V
 Output timing reference level 0.8~2V
 Output load Fig. 1, Fig. 2

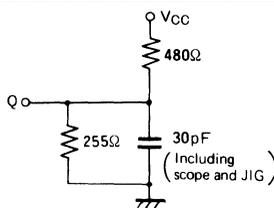


Fig. 1 Output load

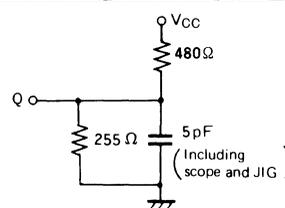
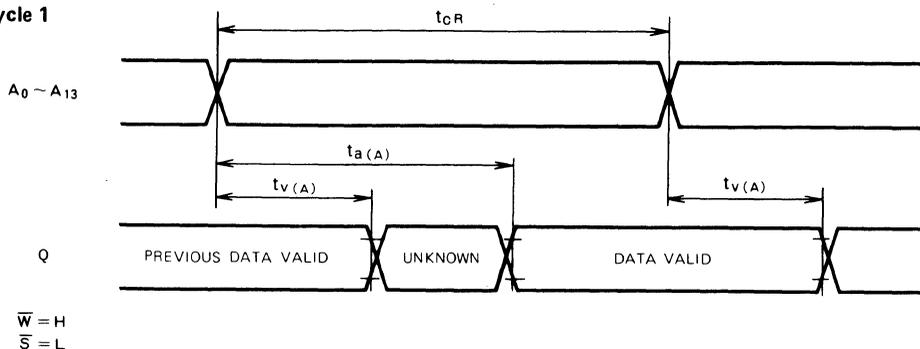


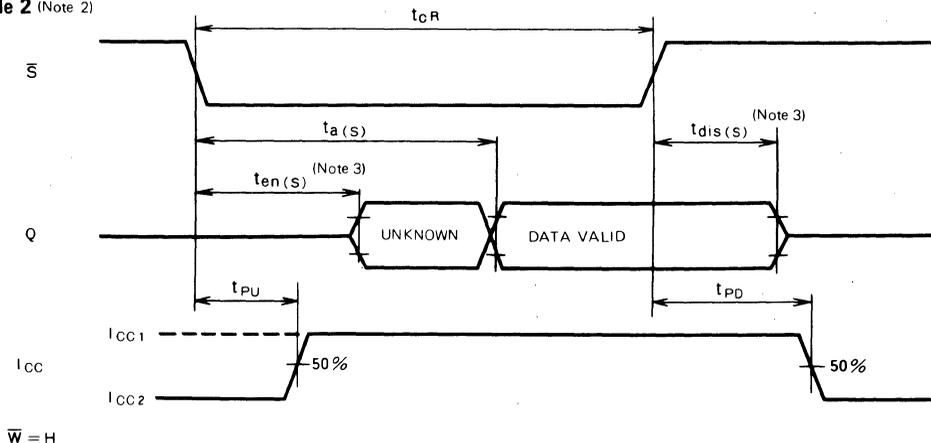
Fig. 2 Output load for t_{en} , t_{dis}

TIMING DIAGRAMS

Read cycle 1



Read cycle 2 (Note 2)



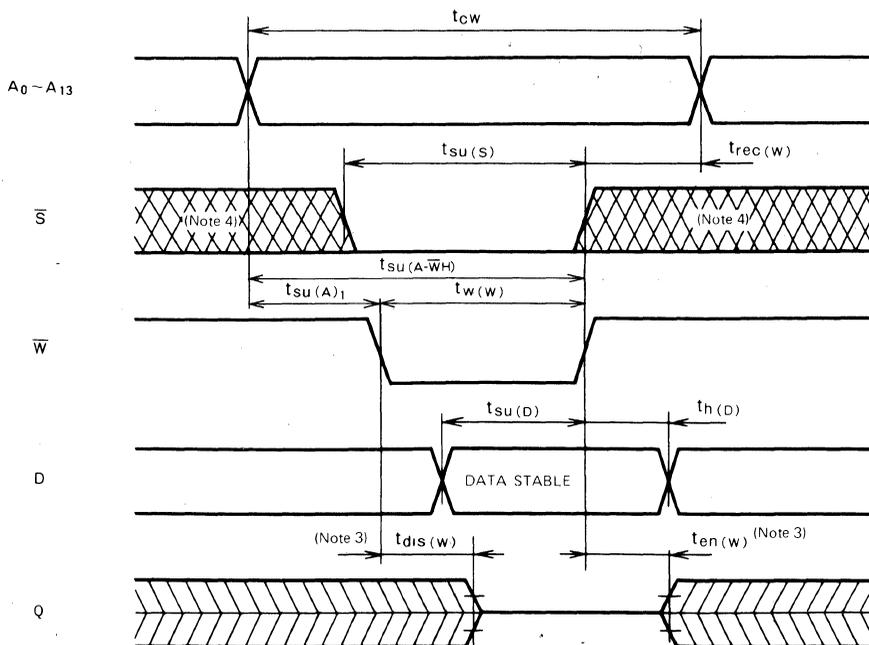
Note 2. Addresses valid prior to or coincident with \overline{S} transition low.

3. Transition is measured $\pm 500\text{mV}$ from steady state voltage with specified loading in Figure 2.

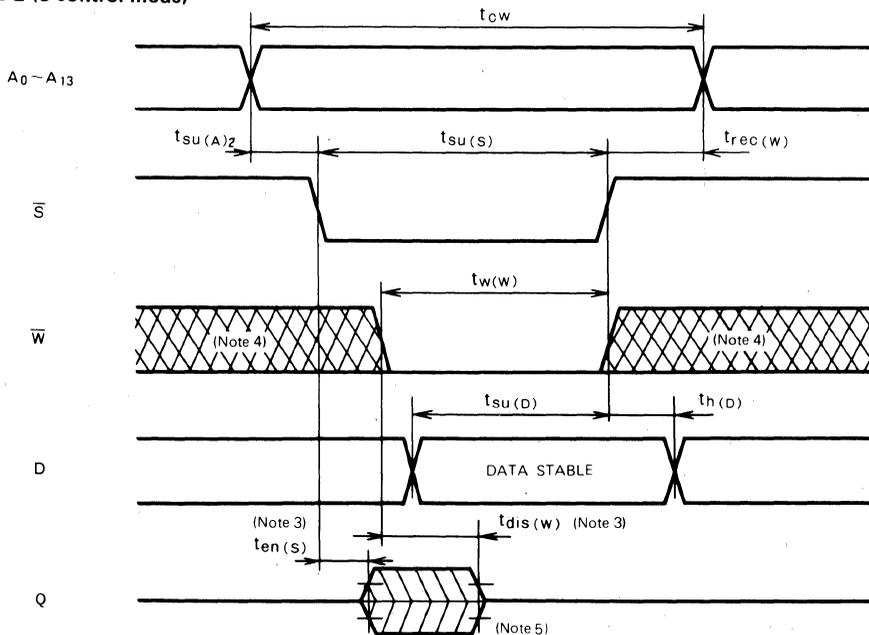
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TIMING DIAGRAMS

Write cycle 1 (\bar{W} control mode)



Write cycle 2 (\bar{S} control mode)



- Note 4. Hatching indicates the state is don't care.
- Note 5. When the falling edge of \bar{W} is simultaneous or prior to the falling edge of \bar{S} , the output is maintained in the high impedance.