M5M23C65-XXXP

PRELIMINARY

Notice: This is not a final specification.
Some parameters are subject to change.

65536-BIT(8192-WORD BY 8-BIT)MASK-PROGRAMMABLE ROM

DESCRIPTION

The Mitsubishi M5M23C65-XXXP is a 65536-bit mask-programmable high speed read-only memory.

The M5M23C65-XXXP is fabricated by silicon gate CMOS technology and available in a 24-pin DIL package.

The XXX in type code is a three-digit decimal number assigned by Mitsubishi to identify the customer's specification to which the ROM has been programmed.

FEATURES

$A_0 \sim A_{12}$	Addresses
CS/$\overline{\text{CS}}$	Chip select
$D_0 \sim D_7$	Outputs

- 8192 word x 8-bit organization
- Access time . . . . 350 ns (max)
- Chip select CS/$\overline{\text{CS}}$ mask programmable
- Low power supply current (Icc)

    Active . . . . 40 mA (max)

    Standby . . . . 10 mA (max)   (TTL-compatible)

    50 μA (max)   (CS/$\overline{\text{CS}}$ =

    0.2V/Vcc−0.2V)

- Single 5V power supply
- 3-state output buffer
- Input and output TTL-compatible
- Standard 24-pin DIL package

FUNCTION

Set the CS/$\overline{\text{CS}}$ terminals to the read mode. (high level/low level)

High level/low level inputs to CS/$\overline{\text{CS}}$ and address signals

PIN CONFIGURATION (TOP VIEW)

Outline 24P4

to the address inputs ($A_0 \sim A_{12}$) make the data contents of the designated address location available at the data input/output ($D_0 \sim D_7$).

When the CS/$\overline{\text{CS}}$ signal is low/high, data input/output are in a floating state, and the device is in the standby mode or power-down mode.

The active logic level of CS/$\overline{\text{CS}}$ can be programmed at the time of fabricating the ROM mask.

BLOCK DIAGRAM

65536-BIT(8192-WORD BY 8-BIT)MASK-PROGRAMMABLE ROM

ABSOLUTE MAXIMUM RATINGS (Note 1)

Temperature under bias .... $-10°C \sim +80°C$

Storage temperature .... $-65°C \sim +150°C$

All input or output voltage (Note 2) .... $-0.3V \sim +7V$

Note 1 Stresses above those listed may cause permanent damage to the device.
This is a stress rating only and functional operation of the device at
these or at any other conditions above those indicated in the operational
sections of this specification is not implied.
Exposure to absolute maximum rating conditions for extended periods
affects device reliability.

   2 With respect to Ground

RECOMMENDED OPERATING CONDITIONS (Ta = 0 ~ 70°C)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage (Note 1)	4.5	5	5.5	V
GND	Supply voltage		0		V
V_{IH}	High level input voltage	2.4		$V_{CC}+0.1$	V
V_{IL}	Low level input voltage	-0.1		0.45	V

Note1 Need $1\mu F$ ceramic capacitor between V_{CC} and GND.

D.C. CHARACTERISTICS (Ta = 0 ~ 70°C, V_{CC}=5V ± 10%, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I_{LI}	Input load current		-10		10	μA
I_{LO}	Output leakage current		-10		10	μA
I_{CC1}	V_{CC} current standby	$CS/\overline{CS} = V_{IL}/V_{IH}$			10	mA
		$CS/\overline{CS} = 0.2V/V_{CC}-0.2V$			50	μA
I_{CC2}	V_{CC} current active	$CS/\overline{CS} = V_{IH}/V_{IL}$, Output open			40	mA
V_{IL}	Input low voltage		-0.1		0.6	V
V_{IH}	Input high voltage		2.2		$V_{CC}+0.1$	V
V_{OL}	Output low voltage	$I_{OL}=2.1mA$			0.45	V
V_{OH}	Output high voltage	$I_{OH}=-400\mu A$	2.4			V

A.C. CHARACTERISTICS (Ta = 0 ~ 70°C, V_{CC}=5V ± 10%, V_{IH}=2.4V, V_{IL}=0.45V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{a(AD)}$	Address to output delay	$CS/\overline{CS} = V_{IH}/V_{IL}$			350	ns
$t_{a(CD)}$	Chip select to output delay				350	ns
$t_{a(DF)}$	Chip select to output float				200	ns
t_{OH}	Output hold from address	$CS/\overline{CS} = V_{IH}/V_{IL}$	0			ns

MITSUBISHI ELECTRIC

A.C. WAVEFORMS
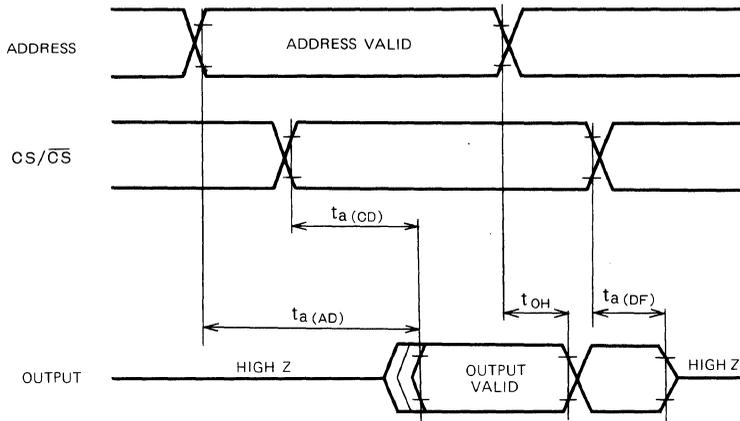
Test Conditions for A.C. Characteristics
Input voltage: $V_{IL}=0.45V$, $V_{IH}=2.4V$
Input rise and fall times : $\leq 20ns$
Reference voltage at timing measurement: Inputs 0.8V and 2V
Output load: 1 TTL gate, $C_L=100pF$ Outputs 0.8V and 2V

CAPACITANCE $(Ta=25°C, f=1MHz)$

Symbol	Parameter	Text conditions	Limits			Unit
			Min	Typ	Max	
C_{IN}	Input Capacitance	$V_{IN}=0V$			10	pF
C_{OUT}	Output Capacitance	$V_{OUT}=0V$			15	pF