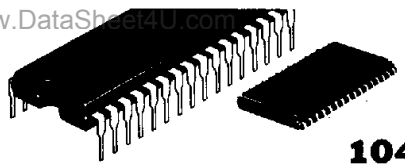


M5M51008P,FP-70,-85,-10,-12,-70L,-85L, -10L,-12L,-70LL,-85LL,-10LL,-12LL

1048576-BIT(131072-WORD BY 8-BIT)CMOS STATIC RAM

MITSUBISHI (MEMORY/ASIC)

DESCRIPTION

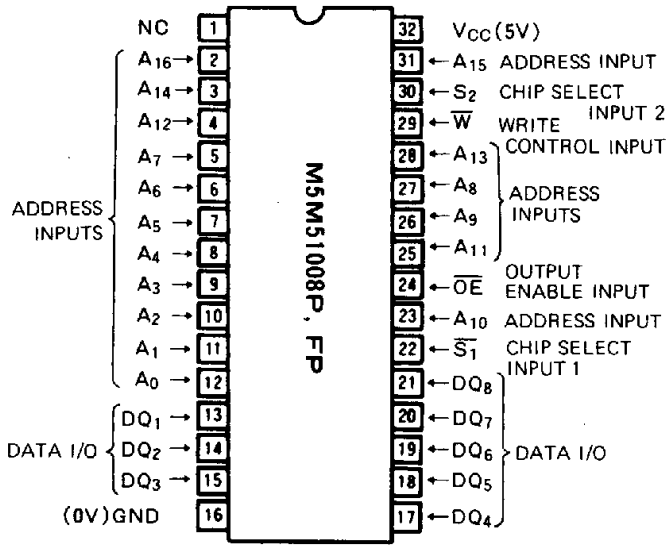
The M5M51008P, FP are 1,048,576-bit CMOS static RAM organized as 131,072 word by 8-bit which are fabricated using high-performance triple polysilicon CMOS technology. The use of resistive load NMOS cells and CMOS periphery result in a high density and low power static RAM. They are ideal for the memory systems which require simple interface. The stand-by current is low enough for a battery back-up application. They are mounted in a standard 32 pin package and configured in an industrial standard 128K x 8-bit pinout.

FEATURE

TYPE	Access time (max)	Power supply current	
		Active (max)	Stand-by (max)
M5M51008P, FP-70 M5M51008P, FP-85 M5M51008P, FP-10 M5M51008P, FP-12	70ns 85ns 100ns 120ns	30mA (1MHz)	2mA
M5M51008P, FP-70L M5M51008P, FP-85L M5M51008P, FP-10L M5M51008P, FP-12L	70ns 85ns 100ns 120ns		100μA (V_{CC} =5.5V) 50μA (V_{CC} =3.0V)
M5M51008P, FP-70LL M5M51008P, FP-85LL M5M51008P, FP-10LL M5M51008P, FP-12LL	70ns 85ns 100ns 120ns		20μA (V_{CC}=5.5V) 10μA (V_{CC}=3.0V)

- Single +5V power supply
- Easy memory expansion and power down by $\overline{S_1}$, S_2
- Data hold on +2V power supply
- $\overline{OE}$ prevents data contention in the I/O bus
- Low stand-by current 1.0μA (TYP)

PIN CONFIGURATION (TOP VIEW)



NC: NO CONNECTION

Outline 32P4 (P)
32P2M (FP)

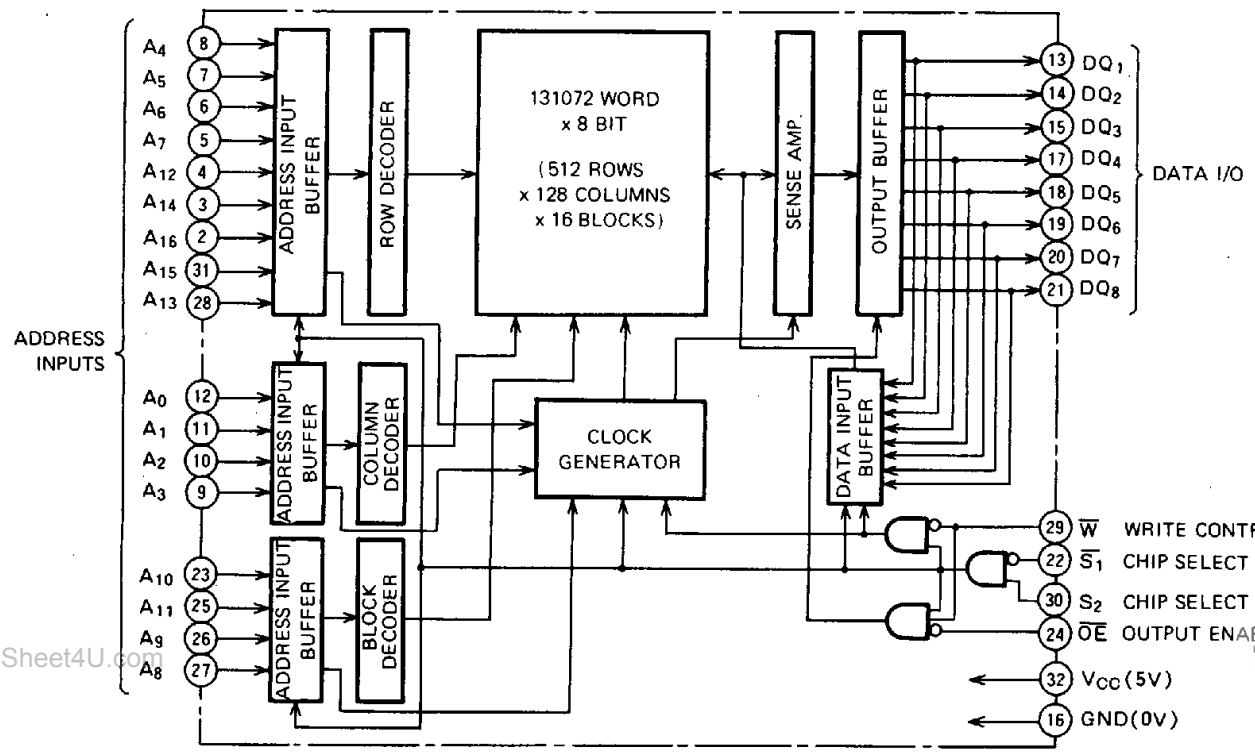
PACKAGE

M5M51008P . . . . . 32 pin 600 mil DIP
M5M51008FP . . . . . 32 pin 525 mil SOP
(small outline package)

APPLICATION

Small capacity memory units.

BLOCK DIAGRAM



FUNCTION

The operation mode of the M5M51008P, FP are determined by a combination of the device control inputs $\overline{S_1}$, S_2, $\overline{W}$ and $\overline{OE}$. Each mode is summarized in the function table.

A write cycle is executed whenever the low level $\overline{W}$ overlaps with the low level $\overline{S_1}$ and the high level S_2. The address must be set up before the write cycle and must be stable during the entire cycle. The data is latched into a cell on the trailing edge of $\overline{W}$, $\overline{S_1}$ or S_2, whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained. The output enable input $\overline{OE}$ directly controls the output stage. Setting the $\overline{OE}$ at a high level, the output stage is in a high-impedance state, and the data bus contention problem in the write cycle is eliminated.

A read cycle is executed by setting $\overline{W}$ at a high level and $\overline{OE}$ at a low level while $\overline{S_1}$ and S_2 are in an active state ($\overline{S_1}$ = L, S_2 = H).

When setting $\overline{S_1}$ at a high level or S_2 at a low level, the chips are in a non-selectable mode in which both reading and writing are disabled. In this mode, the output state is in a high-impedance state, allowing OR-tie with other chips and memory expantion by $\overline{S_1}$ and S_2. The power supply current is reduced as low as the stand-by current which is specified as I_{CC3} or I_{CC4}, and the meory data can be held at +2V power supply, enabling battery back-up operation during power failure or power-down operation in the non-selected mode.

FUNCTION TABLE

$\overline{S_1}$	S_2	$\overline{W}$	$\overline{OE}$	Mode	DQ	I_{CC}
X	L	X	X	Non selection	High-impedance	Stand-by
H	X	X	X	Non selection	High-impedance	Stand-by
L	H	L	X	Write	D_{in}	Active
L	H	H	L	Read	D_{out}	Active
L	H	H	H		High-impedance	Active

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Units
V_{CC}	Supply voltage	With respect to GND	−0.3～7	V
V_I	Input voltage	With respect to GND	−0.3*～V_{CC}+0.3	V
V_O	Output voltage	With respect to GND	0～V_{CC}	V
Pd	Power dissipation	Ta＝25°C	700	mW
Topr	Operating temperature		0～70	°C
Tstg	Storage temperature		−65～150	°C

*−3.0V incase of AC (Pulse width ≦50ns)

DC ELECTRICAL CHARACTERISTICS (Ta＝0～70°C, V_{CC}＝5V±10%, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits Min	Limits Typ	Limits Max	Units
V_{IH}	High-level input voltage			2.2		V_{CC}+0.3	V
V_{IL}	Low-level input voltage			−0.3*		0.8	V
V_{OH}	High-level output voltage	I_{OH}＝−1mA		2.4			V
		I_{OH}＝−0.1mA		V_{CC}-0.5			
V_{OL}	Low-level output voltage	I_{OL}＝2mA				0.4	V
I_I	Input leakage current	V_I＝0～V_{CC}				±1	μA
I_O	Output leakage current	$\overline{S_1}$＝V_{IH} or S_2＝V_{IL} or $\overline{OE}$＝V_{IH}				1	μA
		$V_{I/O}$＝0～V_{CC}				−1	μA
I_{CC1}	Active supply current (AC, MOS level)	$\overline{S_1}$≦0.2V, S_2≧V_{CC}−0.2V other inputs ≦0.2V or≧V_{CC} − 0.2V Output-open (duty 100%)	Min cycle		50	90	mA
			1MHz		25	30	
I_{CC2}	Active supply current (AC, TTL level)	$\overline{S_1}$＝V_{IL}, S_2＝V_{IH} other inputs ＝V_{IH} or V_{IL} Output-open (duty 100%)	Min cycle		60	100	mA
			1MHz		30	40	
I_{CC3}	Stand by current	S_2≦0.2V or $\overline{S_1}$≧V_{CC}− 0.2V, S_2≧ V_{CC}−0.2V other inputs ＝0～V_{CC}	P,FP			2	mA
			P,FP-L			100	μA
			P,FP-LL		1.0		μA
I_{CC4}	Stand by current	$\overline{S_1}$＝V_{IH} or S_2＝V_{IL} other inputs ＝0～V_{CC}				3	mA

*−3.0V incase of AC (Pulse width ≦50ns)

CAPACITANCE (Ta＝0～70°C, V_{CC}＝5V±10%, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Units
C_I	Input capacitance	V_I＝GND, V_I＝25mVrms, f＝1MHz			6	pF
C_O	Output capacitance	V_O＝GND, V_O＝25mVrms, f＝1MHz			8	pF

Note 1: Direction for current flowing into an IC is positive (no mark). 2: Typical value is V_{CC} = 5V, T_a = 25°C.

AC ELECTRICAL CHARACTERISTICS (T_a=0~70°C, V_{CC}=5V±10%, unless otherwise noted)

(1) MEASUREMENT CONDITIONS

Input pulse . . . . . V_{IH} = 2.4V, V_{IL} = 0.6V
Input rise and fall time . . . 5ns
Reference leve . . . . . V_{OH} = V_{OL} = 1.5V
Transition is measured ±500mV from steady state voltage. (for t_{en}, t_{dis})
Output loads . . . . . Fig. 1, C_L = 100pF (P, FP-85, -10, -12, -85L, -10L, -12L, -85LL, -10LL, -12LL)
C_L = 30pF (P, FP-70, -70L, -70LL)
C_L = 5pF (for t_{en}, t_{dis})

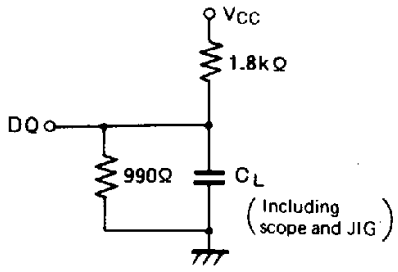


Fig. 1 Output load

(2) READ CYCLE

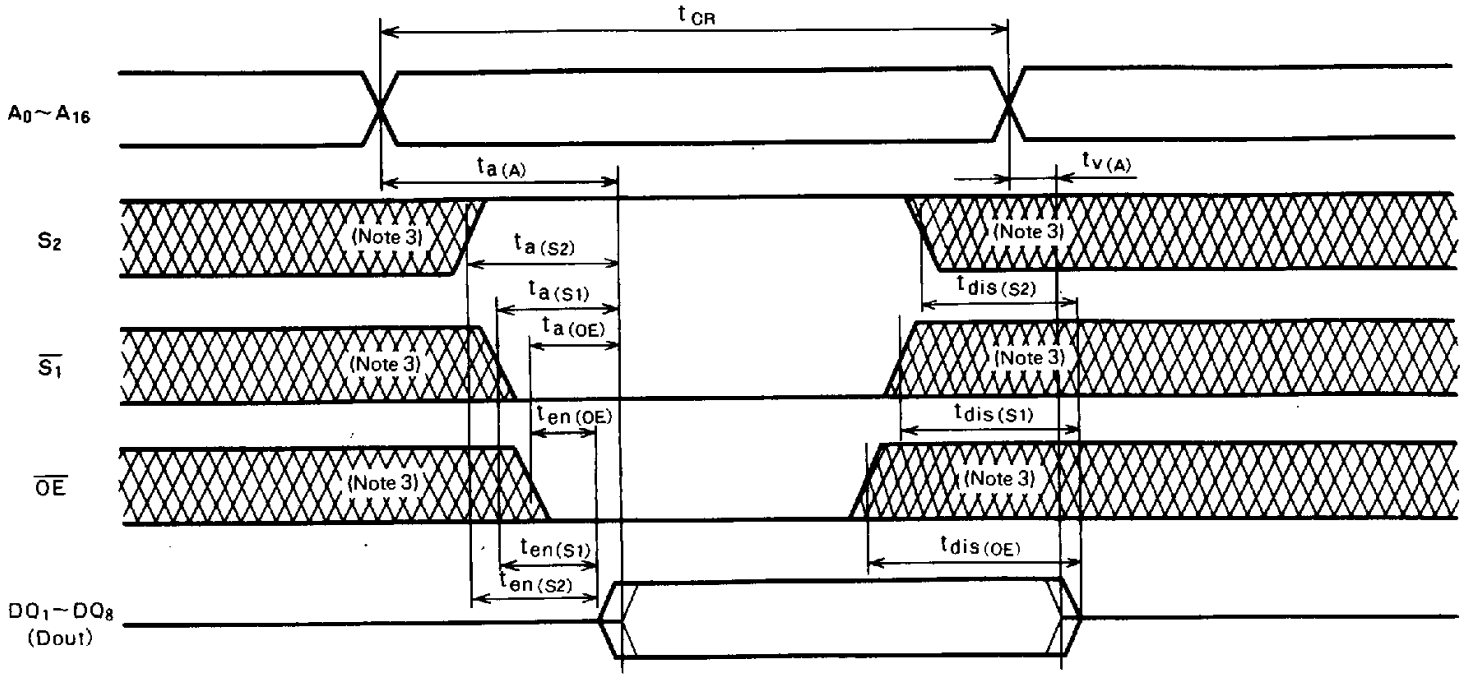
Symbol	Parameter	M5M51008P, FP								Units
		-70, -70L, -70LL		-85, -85L, -85LL		-10, -10L, -10LL		-12, -12L, -12LL		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{CR}	Read cycle time	70		85		100		120		ns
$t_{a(A)}$	Address access time		70		85		100		120	ns
$t_{a(S1)}$	Chip select 1 access time		70		85		100		120	ns
$t_{a(S2)}$	Chip select 2 access time		70		85		100		120	ns
$t_{a(OE)}$	Output enable access time		35		45		50		60	ns
$t_{dis(S1)}$	Output disable time after $\overline{S_1}$ high		25		30		35		40	ns
$t_{dis(S2)}$	Output disable time after S_2 low		25		30		35		40	ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high		25		30		35		40	ns
$t_{en(S1)}$	Output enable time after $\overline{S_1}$ low	5		5		5		5		ns
$t_{en(S2)}$	Output enable time after S_2 high	5		5		5		5		ns
$t_{en(OE)}$	Output enable time after $\overline{OE}$ low	5		5		5		5		ns
$t_{v(A)}$	Data valid time after address	10		10		10		10		ns

(3) WRITE CYCLE

Symbol	Parameter	M5M51008P, FP								Units
		-70, -70L, -70LL		-85, -85L, -85LL		-10, -10L, -10LL		-12, -12L, -12LL		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{CW}	Write cycle time	70		85		100		120		ns
$t_{w(W)}$	Write pulse width	55		65		75		85		ns
$t_{su(A)}$	Address set up time	0		0		0		0		ns
$t_{su(A-WH)}$	Address set up time with respect to $\overline{W}$ high	65		75		85		100		ns
$t_{su(S1)}$	Chip select 1 set up time	65		75		85		100		ns
$t_{su(S2)}$	Chip select 2 set up time	65		75		85		100		ns
$t_{su(D)}$	Data set up time	30		35		40		45		ns
$t_{h(D)}$	Data hold time	0		0		0		0		ns
$t_{rec(W)}$	Write recovery time	0		0		0		0		ns
$t_{dis(W)}$	Output disable time from $\overline{W}$ low		25		30		35		40	ns
$t_{dis(OE)}$	Output disable time from $\overline{OE}$ high		25		30		35		40	ns
$t_{en(W)}$	Output enable time from $\overline{W}$ high	5		5		5		5		ns
$t_{en(OE)}$	Output enable time from $\overline{OE}$ low	5		5		5		5		ns

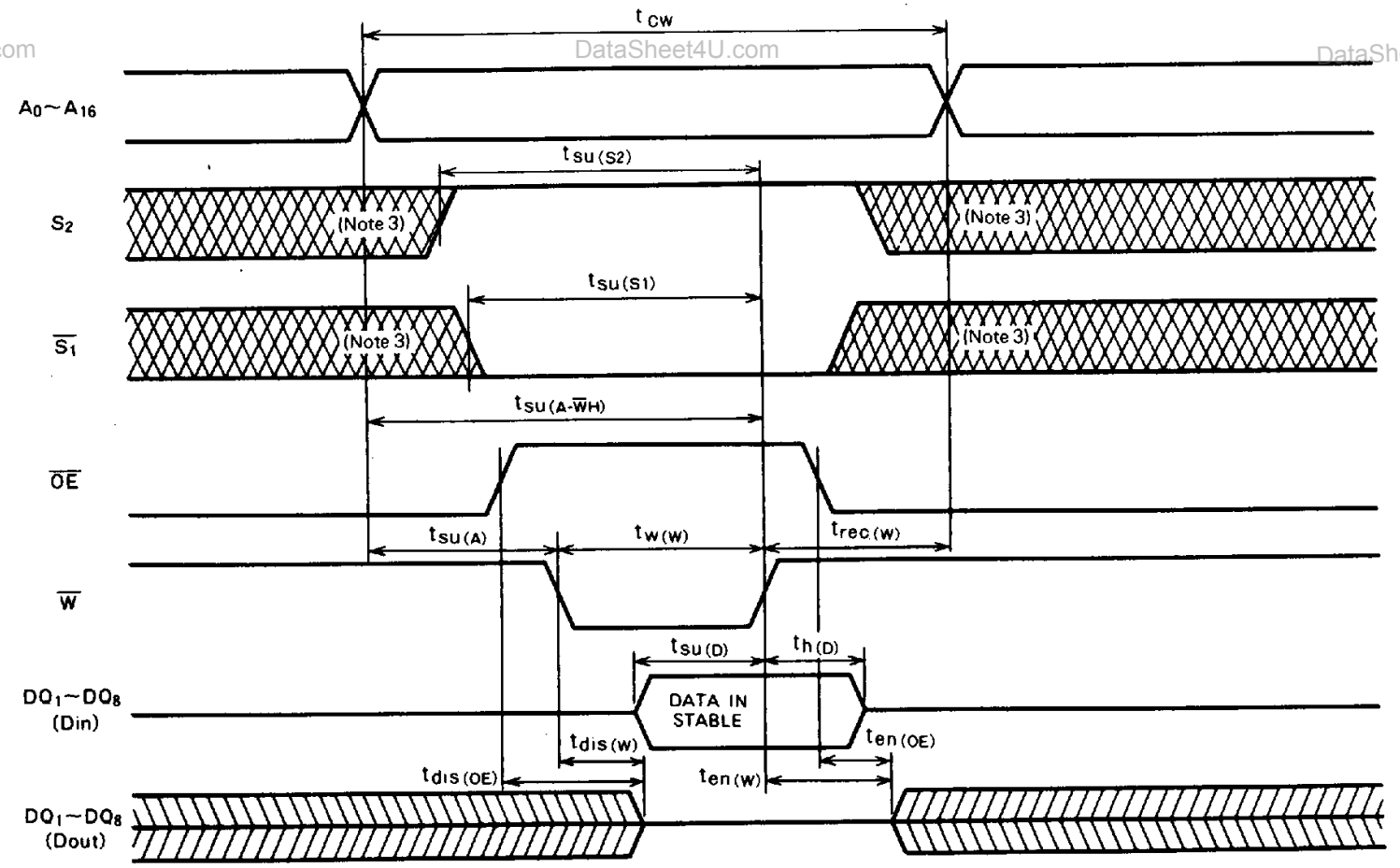
(4) TIMING DIAGRAMS

Read cycle

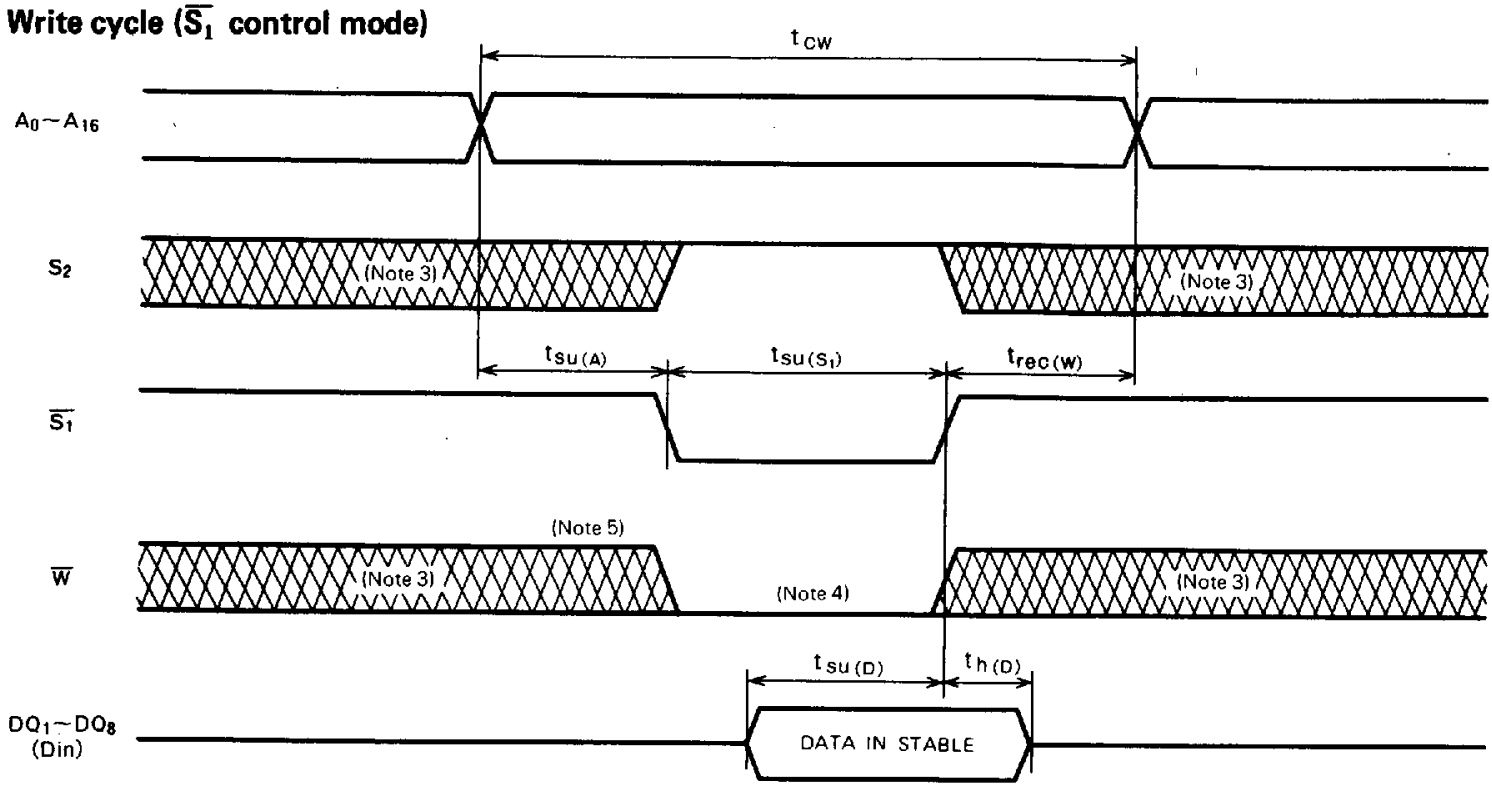


W = "H" level

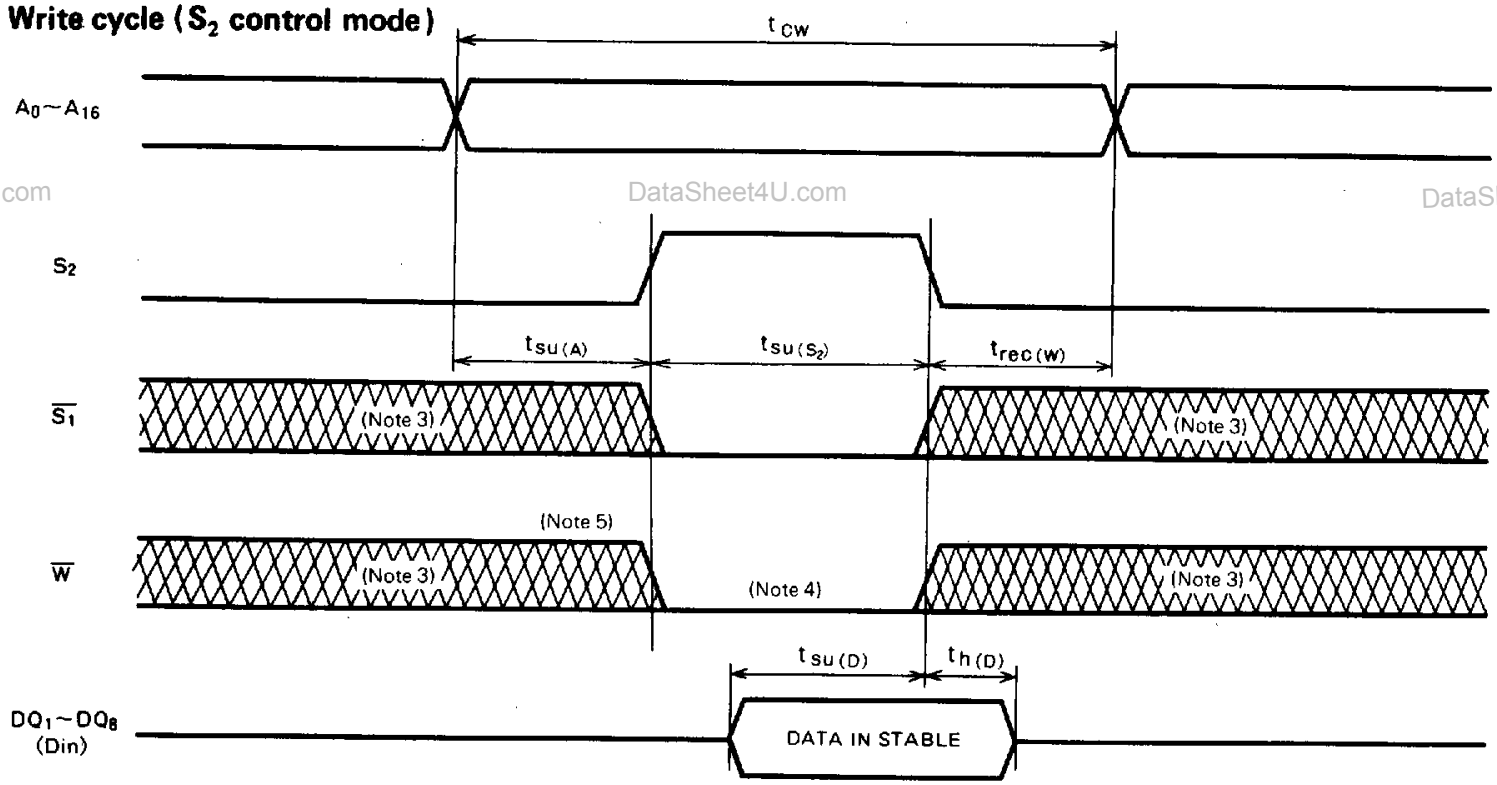
Write cycle (W control mode)



Write cycle ($\overline{S_1}$ control mode)



Write cycle (S_2 control mode)



Note 3: Hatching indicates the state is 'don't care'.
4: Writing is executed while S_2 high overlaps $\overline{S_1}$ and $\overline{W}$ low.
5: When the falling edge of $\overline{W}$ is simultaneously or prior to the falling edge of $\overline{S_1}$ or rising edge of S_2, the outputs are maintained in the high impedance state.
6: Don't apply inverted phase signal externally when DQ pin is output mode.

POWER DOWN CHARACTERISTICS

ELECTRICAL CHARACTERISTICS (T_a = 0 ~ 70°C, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ	Max	
$V_{CC(PD)}$	Power down supply voltage			2			V
$V_{I(\overline{S_1})}$	Chip select input $\overline{S_1}$	$2.2V \leqq V_{CC(PD)}$		2.2			V
		$2V \leqq V_{CC(PD)} \leqq 2.2V$			$V_{CC(PD)}$		
$V_{I(S_2)}$	Chip select input S_2	$4.5V \leqq V_{CC(PD)}$				0.8	V
		$V_{CC(PD)} < 4.5V$				0.2	
$I_{CC(PD)}$	Power down supply current	V_{CC}=3V $S_2 \leqq 0.2V$ or $\overline{S_1} \geqq V_{CC}-0.2V$, $S_2 \geqq V_{CC}-0.2V$	P, FP			2	mA
			P, FP-L			50	μA
			P, FP-LL			10 note 7	μA

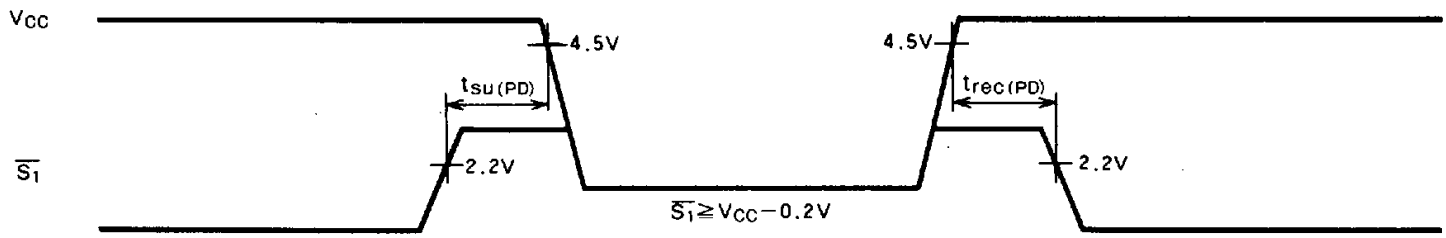
Note 7: I_{CC} (PD) = 1μA in case of T_a = 25°C

TIMING REQUIREMENTS (T_a = 0 ~ 70°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{su\ (PD)}$	Power down set up time		0			ns
$t_{rec\ (PD)}$	Power down recovery time		5			ms

POWER DOWN CHARACTERISTICS

$\overline{S_1}$ control mode



S_2 control mode