PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change

M5M417800CJ,TP-5,-6,-7, -5S,-6S,-7S

FAST PAGE MODE 16777216-BIT (2097152-WORD BY 8-BIT) DYNAMIC RAM

DESCRIPTION

This is a family of 2097152-word by 8-bit dynamic RAMs, fabricated with the high performance CMOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential.

The use of double-layer metal process combined with twin-well CMOS technology and a single-transistor dynamic storage stacked capacitor cell provide high circuit density at reduced costs. Multiplexed address inputs permit both a reduction in pins and an increase in system densities.

FEATURES

Type name	$\overline{RAS}$ access time (max.ns)	$\overline{CAS}$ access time (max.ns)	Address access time (max.ns)	$\overline{OE}$ access time (max.ns)	Cycle time (min.ns)	Power dissipation (typ.mW)
M5M417800CXX-5,-5S	50	13	25	13	90	655
M5M417800CXX-6,-6S	60	15	30	15	110	540
M5M417800CXX-7,-7S	70	20	35	20	130	475

XX=J,TP

- Standard 28pin SOJ, 28pin TSOP
- Single 5V±10% supply
- Low stand-by power dissipation
  - 5.5mW (Max) ---------- CMOS Input level
  - 2.2mW (Max) * ---------- CMOS Input level
- Low operating power dissipation
  - M5M417800Cxx-5,-5S ---------- 800.0mW (Max)
  - M5M417800Cxx-6,-6S ---------- 660.0mW (Max)
  - M5M417800Cxx-7,-7S ---------- 580.0mW (Max)
- Self refresh capability *
  - Self refresh current ---------- 200.0 μA(Max)
- Fast-page mode, Read-modify-write, $\overline{RAS}$-only refresh
- $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh capabilities
  Early-write mode and $\overline{OE}$ to control output buffer impedance
- All inputs, output TTL compatible and low capacitance
- 2048 refresh cycles every 32ms (A_0~A_{10})

* Applicable to self refresh version (M5M417800CJ,TP-5S,-6S,-7S :option) only

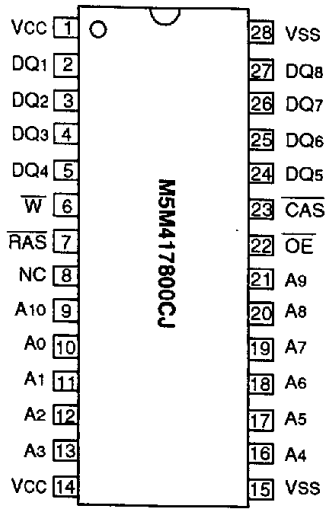
APPLICATION

Main memory unit for computers, Microcomputer memory, Refresh memory for CRT

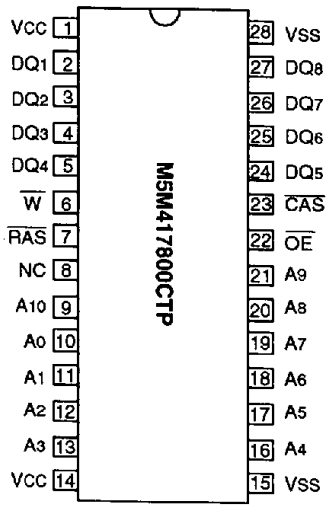
PIN DESCRIPTION

Pin name	Function
A_0~A_{10}	Address inputs
DQ_1~DQ_8	Data inputs/outputs
$\overline{RAS}$	Row address strobe input
$\overline{CAS}$	Column address strobe input
$\overline{W}$	Write control input
$\overline{OE}$	Output enable input
V_{CC}	Power supply (+5V)
V_{SS}	Ground (0V)

PIN CONFIGURATION (TOP VIEW)



Outline 28P0N-A (400mil SOJ)



Outline 28P3N-C (400mil TSOP)

NC:NO CONNECTION

PRELIMINARY
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M5M417800CJ,TP-5,-6,-7,-5S,-6S,-7S

FAST PAGE MODE 16777216-BIT (2097152-WORD BY 8-BIT) DYNAMIC RAM

FUNCTION

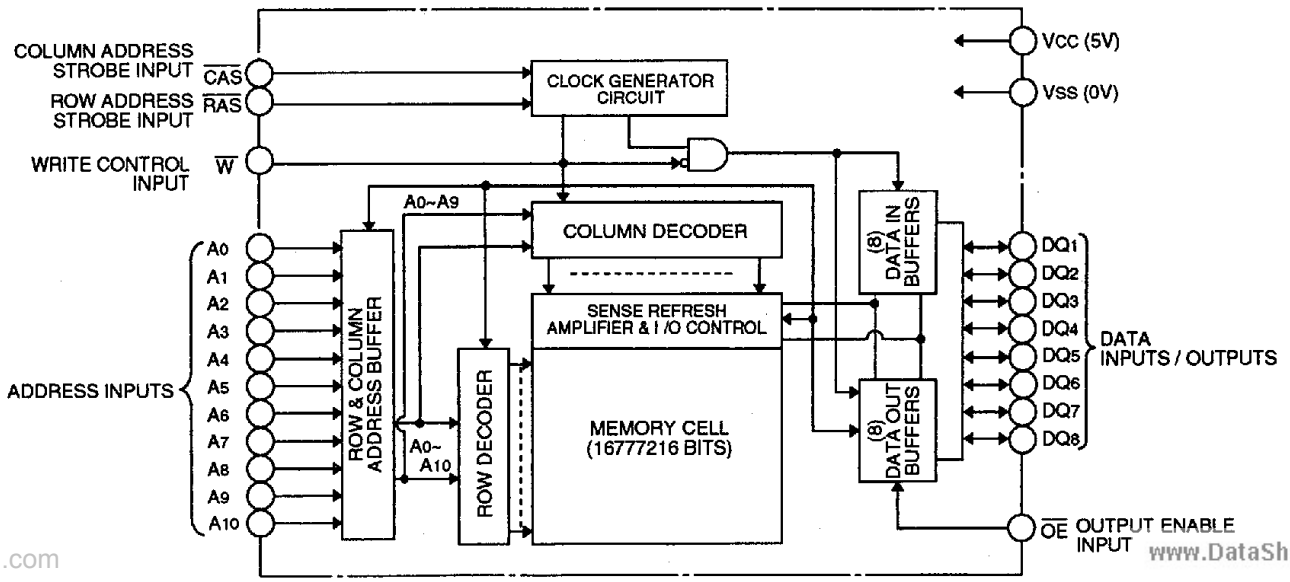
The M5M417800CJ, TP provide, in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g., fast page mode, $\overline{RAS}$-only refresh, and delayed-write. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs						Input/Output		Refresh	Remark
	$\overline{RAS}$	$\overline{CAS}$	$\overline{W}$	$\overline{OE}$	Row address	Column address	Input	Output		
Read	ACT	ACT	NAC	ACT	APD	APD	OPN	VLD	YES	Fast page mode identical
Write (Early write)	ACT	ACT	ACT	DNC	APD	APD	VLD	OPN	YES	
Write (Delayed write)	ACT	ACT	ACT	DNC	APD	APD	VLD	IVD	YES	
Read-modify-write	ACT	ACT	ACT	ACT	APD	APD	VLD	VLD	YES	
$\overline{RAS}$-only refresh	ACT	NAC	DNC	DNC	APD	DNC	DNC	OPN	YES	
Hidden refresh	ACT	ACT	NAC	ACT	APD	DNC	OPN	VLD	YES	
Self refresh	ACT	ACT	NAC	DNC	DNC	DNC	DNC	OPN	YES	
$\overline{CAS}$ before $\overline{RAS}$ refresh	ACT	ACT	NAC	DNC	DNC	DNC	DNC	OPN	YES	
Stand-by	NAC	DNC	DNC	DNC	DNC	DNC	DNC	OPN	NO	

Note : ACT : active, NAC : nonactive, DNC : don' t care, VLD : valid, IVD : invalid, APD : applied, OPN : open

BLOCK DIAGRAM



PRELIMINARY

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M5M417800CJ,TP-5,-6,-7,-5S,-6S,-7S

FAST PAGE MODE 16777216-BIT (2097152-WORD BY 8-BIT) DYNAMIC RAM

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to Vss	-1 ~ 7	V
V_I	Input voltage		-1 ~ 7	V
V_O	Output voltage		-1 ~ 7	V
I_O	Output current		50	mA
P_d	Power dissipation	Ta=25°C	1000	mW
T_{opr}	Operating temperature		0 ~ 70	°C
T_{stg}	Storage temperature		-65 ~ 150	°C

RECOMMENDED OPERATING CONDITIONS (Ta=0~70°C, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage	0	0	0	V
V_{IH}	High-level input voltage, all inputs	2.4		5.5	V
V_{IL}	Low-level input voltage, all inputs	-1.0**		0.8	V

Note 1 : All voltage values are with respect to Vss.
**: V_{IL}(min.) is -2.0V when undershoot width is less than 25ns. (Undershoot width is with respect to V_{SS}.)

ELECTRICAL CHARACTERISTICS (Ta=0~70°C, Vcc=5V±10%, Vss=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{OH}	High-level output voltage		I_{OH}=-5mA	2.4		Vcc	V
V_{OL}	Low-level output voltage		I_{OL}=4.2mA	0		0.4	V
I_{OZ}	Off-state output current		Q floating 0V≦V_{OUT}≦5.5V	-10		10	μA
I_I	Input current		0V≦V_{IN}≦5.5V, Other inputs pins=0V	-10		10	μA
I_{CC1} (AV)	Average supply current from Vcc, operating (Note 3,4)	M5M417800C-5,-5S	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC}=t_{WC}=min. output open			145	mA
		M5M417800C-6,-6S				120	
		M5M417800C-7,-7S				105	
I_{CC2}	Supply current from Vcc, stand-by (Note 5)		$\overline{RAS}$= $\overline{CAS}$ =V_{IH}, output open			2	mA
			$\overline{RAS}$= $\overline{CAS}$≧Vcc -0.2V			0.5	
I_{CC3} (AV)	Average supply current from Vcc, refreshing (Note 3)	M5M417800C-5,-5S	$\overline{RAS}$ cycling, $\overline{CAS}$= V_{IH} t_{RC}=min. output open			145	mA
		M5M417800C-6,-6S				120	
		M5M417800C-7,-7S				105	
I_{CC4}(AV)	Average supply current from Vcc, Fast-Page-Mode (Note 3,4)	M5M417800C-5,-5S	$\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling t_{PC}=min. output open			80	mA
		M5M417800C-6,-6S				70	
		M5M417800C-7,-7S				60	
I_{CC6}(AV)	Average supply current from Vcc, $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3)	M5M417800C-5,-5S	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling t_{RC}=min. output open			145	mA
		M5M417800C-6,-6S				120	
		M5M417800C-7,-7S				105	

Note 2: Current flowing into an IC is positive, out is negative.
3: I_{CC1} (AV), I_{CC3} (AV), I_{CC4} (AV) and I_{CC6} (AV) are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4: I_{CC1} (AV) and I_{CC4} (AV) are dependent on output loading. Specified values are obtained with the output open.

CAPACITANCE (Ta=0~70°C, Vcc=5V±10%, Vss=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$C_{I(A)}$	Input capacitance, address inputs	V_I=Vss f=1MHz V_I=25mVrms			5	pF
$C_{I(\overline{OE})}$	Input capacitance, $\overline{OE}$ input				7	pF
$C_{I(\overline{W})}$	Input capacitance, write control input				7	pF
$C_{I(\overline{RAS})}$	Input capacitance, $\overline{RAS}$ input				7	pF
$C_{I(\overline{CAS})}$	Input capacitance, $\overline{CAS}$ input				7	pF
$C_{I/O}$	Input/output capacitance, data ports				8	pF

PRELIMINARY
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FAST PAGE MODE 16777216-BIT (2097152-WORD BY 8-BIT) DYNAMIC RAM

SWITCHING CHARACTERISTICS (Ta=0~70°C, Vcc=5V±10%, Vss=0V, unless otherwise noted, see notes 5,12,13)

Symbol	Parameter		Limits						Unit
			M5M417800C-5,-5S		M5M417800C-6,-6S		M5M417800C-7,-7S		
			Min	Max	Min	Max	Min	Max	
tCAC	Access time from $\overline{CAS}$	(Note 6,7)		13		15		20	ns
tRAC	Access time from $\overline{RAS}$	(Note 6,8)		50		60		70	ns
tAA	Column address access time	(Note 6,9)		25		30		35	ns
tCPA	Access time from $\overline{CAS}$ precharge	(Note 6,10)		30		35		40	ns
tOEA	Access time from $\overline{OE}$	(Note 6)		13		15		20	ns
tCLZ	Output low impedance time from $\overline{CAS}$ low	(Note 6)	5		5		5		ns
tOFF	Output disable time after $\overline{CAS}$ high	(Note 11)	0	13	0	15	0	15	ns
tOEZ	Output disable time after $\overline{OE}$ high	(Note 11)	0	13	0	15	0	15	ns

Note 5:An initial pause of 500μs is required after power-up followed by a minimum of eight initialization $\overline{RAS}$ cycles. The initialization cycles should be done either by $\overline{RAS}$-only refresh cycles or by $\overline{CAS}$ before $\overline{RAS}$ refresh cycles only.
Note the $\overline{RAS}$ may be cycled during the initial pause. And any 8 $\overline{RAS}$ or $\overline{RAS}$/$\overline{CAS}$ cycles are required after prolonged periods (greater than 32ms) of $\overline{RAS}$ inactivity before proper device operation is achieved.
After the initialization cycles, $\overline{RAS}$ should be kept either higher than VIH(min) or lower than VIL(max) except $\overline{RAS}$ transition time.

6:Measured with a load circuit equivalent to 2TTL loads and 100pF.

7:Assumes that tRCD≧tRCD(max) and tASC≧tASC(max).

8:Assumes that tRCD≦tRCD(max) and tRAD≦tRAD(max). If tRCD or tRAD is greater than the maximum recommended value shown in this table, tRAC will increase by amount that tRCD exceeds the value shown.

9:Assumes that tRAD≧tRAD(max) and tASC≦tASC(max).

10:Assumes that tCP≦tCP(max) and tASC≧tASC(max).

11:tOFF(max) and tOEZ (max) defines the time at which the output achieves the high impedance state (IOUT ≦|±10μA|) and is not reference to VOH(min) or VOL(max).

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh, and Fast-Page Mode Cycles)

(Ta=0~70°C, Vcc=5V±10%, Vss=0V, unless otherwise noted, see notes 12,13)

Symbol	Parameter		Limits						Unit
			M5M417800C-5,-5S		M5M417800C-6,-6S		M5M417800C-7,-7S		
			Min	Max	Min	Max	Min	Max	
tREF	Refresh cycle time			32		32		32	ms
tRP	$\overline{RAS}$ high pulse width		30		40		50		ns
tRCD	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low	(Note 14)	18	37	20	45	20	50	ns
tCRP	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low		10		10		10		ns
tRPC	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low		0		0		0		ns
tCPN	$\overline{CAS}$ high pulse width		10		10		10		ns
tRAD	Column address delay time from $\overline{RAS}$ low	(Note 15)	13	25	15	30	15	35	ns
tASR	Row address setup time before $\overline{RAS}$ low		0		0		0		ns
tASC	Column address setup time before $\overline{CAS}$ low	(Note 16)	0	10	0	10	0	10	ns
tRAH	Row address hold time after $\overline{RAS}$ low		8		10		10		ns
tCAH	Column address hold time after $\overline{CAS}$ low		13		15		15		ns
tDZC	Delay time, data to $\overline{CAS}$ low	(Note 17)	0		0		0		ns
tDZO	Delay time, data to $\overline{OE}$ low	(Note 17)	0		0		0		ns
tCDD	Delay time, $\overline{CAS}$ high to data	(Note 18)	13		15		15		ns
tODD	Delay time, $\overline{OE}$ high to data	(Note 18)	13		15		15		ns
tT	Transition time	(Note 19)	1	50	1	50	1	50	ns

Note 12:The timing requirements are assumed tT=5ns.

13:VIH(min) and VIL(max) are reference levels for measuring timing of input signals.

14:tRCD(max) is specified as a reference point only. If tRCD is less than tRCD(max), access time is tRAC. If tRCD is greater than tRCD(max), access time is controlled exclusively by tCAC or tAA. tRCD(min) is specified as tRCD(min) =tRAH(min) +2tH+tASC(min).

15:tRAD(max) is specified as a reference point only. If tRAD≧tRAD(max) and tASC≦tASC(max), access time is controlled exclusively by tAA.

16:tASC(max) is specified as a reference point only. If tRCD≧tRCD(max) and tASC≧tASC(max), access time is controlled exclusively by tCAC.

17:Either tDZC or tDZO must be satisfied.

18:Either tCDD or tODD must be satisfied.

19:tT is measured between VIH(min) and VIL(max).

PRELIMINARY
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Read and Refresh Cycles

Symbol	Parameter	Limits						Unit
		M5M417800C-5,-5S		M5M417800C-6,-6S		M5M417800C-7,-7S		
		Min	Max	Min	Max	Min	Max	
tRC	Read cycle time	90		110		130		ns
tRAS	$\overline{RAS}$ low pulse width	50	10000	60	10000	70	10000	ns
tCAS	$\overline{CAS}$ low pulse width	13	10000	15	10000	20	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low	50		60		70		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low	13		15		20		ns
tRCS	Read setup time after $\overline{CAS}$ high	0		0		0		ns
tRCH	Read hold time after $\overline{CAS}$ low (Note 20)	0		0		0		ns
tRRH	Read hold time after $\overline{RAS}$ low (Note 20)	10		10		10		ns
tRAL	Column address to $\overline{RAS}$ hold time	25		30		35		ns
tOCH	$\overline{CAS}$ hold time after $\overline{OE}$ low	13		15		20		ns
tORH	$\overline{RAS}$ hold time after $\overline{OE}$ low	13		15		20		ns

Note 20: Either tRCH or tRRH must be satisfied for a read cycle.

Write Cycle (Early Write and Delayed Write)

Symbol	Parameter	Limits						Unit
		M5M417800C-5,-5S		M5M417800C-6,-6S		M5M417800C-7,-7S		
		Min	Max	Min	Max	Min	Max	
tWC	Write cycle time	90		110		130		ns
tRAS	$\overline{RAS}$ low pulse width	50	10000	60	10000	70	10000	ns
tCAS	$\overline{CAS}$ low pulse width	13	10000	15	10000	20	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low	50		60		70		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low	13		15		20		ns
tWCS	Write setup time before $\overline{CAS}$ low (Note 22)	0		0		0		ns
tWCH	Write hold time after $\overline{CAS}$ low	8		10		10		ns
tCWL	$\overline{CAS}$ hold time after $\overline{W}$ low	13		15		20		ns
tRWL	$\overline{RAS}$ hold time after $\overline{W}$ low	13		15		20		ns
tWP	Write pulse width	8		10		10		ns
tDS	Data setup time before $\overline{CAS}$ low or $\overline{W}$ low	0		0		0		ns
tDH	Data hold time after $\overline{CAS}$ low or $\overline{W}$ low	8		10		15		ns
tOEH	$\overline{OE}$ hold time after $\overline{W}$ low	13		15		20		ns

PRELIMINARY
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FAST PAGE MODE 16777216-BIT (2097152-WORD BY 8-BIT) DYNAMIC RAM

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter	Limits						Unit
		M5M417800C-5,-5S		M5M417800C-6,-6S		M5M417800C-7,-7S		
		Min	Max	Min	Max	Min	Max	
t_{RWC}	Read write/read modify write cycle time (Note 21)	131		155		180		ns
t_{RAS}	$\overline{RAS}$ low pulse width	91	10000	105	10000	120	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width	54	10000	60	10000	70	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	91		105		120		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low	54		60		70		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low	0		0		0		ns
t_{CWD}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (Note 22)	36		40		45		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (Note 22)	73		85		95		ns
t_{AWD}	Delay time, address to $\overline{W}$ low (Note 22)	48		55		60		ns
t_{CWL}	$\overline{CAS}$ hold time after $\overline{W}$ low	13		15		20		ns
t_{RWL}	$\overline{RAS}$ hold time after $\overline{W}$ low	13		15		20		ns
t_{WP}	Write pulse width	8		10		10		ns
t_{DS}	Data setup time before $\overline{W}$ low	0		0		0		ns
t_{DH}	Data hold time after $\overline{W}$ low	8		10		15		ns
t_{OEH}	$\overline{OE}$ hold time after $\overline{W}$ low	13		15		15		ns

Note 21: t_{RWC} is specified as $t_{RWC(min)}=t_{RAC(max)}+t_{ODD(min)}+t_{RWL(min)}+t_{RP(min)}+5t_T$.

22: t_{WCS}, t_{CWD}, t_{RWD} and t_{AWD} and, t_{CPWD} are specified as reference points only. If $t_{WCS} \geqq t_{WCS(min)}$ the cycle is an early write cycle and the DQ pins will remain high impedance throughout the entire cycle. If $t_{CWD} \geqq t_{CWD(min)}$, $t_{RWD} \geqq t_{RWD(min)}$, $t_{AWD} \geqq t_{AWD(min)}$ and $t_{CPWD} \geqq t_{CPWD(min)}$ (for fast page mode cycle only), the cycle is a read-modify-write cycle and the DQ will contain the data read from the selected address. If neither of the above condition (delayed write) of the DQ (at access time and until $\overline{CAS}$ or $\overline{OE}$ goes back to VIH) is indeterminate.

Fast-Page Mode Cycle (Read, Early Write, Read -Write, Read-Modify-Write Cycle) (Note 23)

Symbol	Parameter	Limits						Unit
		M5M417800C-5,-5S		M5M417800C-6,-6S		M5M417800C-7,-7S		
		Min	Max	Min	Max	Min	Max	
t_{PC}	Fast page mode read/write cycle time	35		40		45		ns
t_{PRWC}	Fast page mode read write/read modify write cycle time	76		85		95		ns
t_{RAS}	$\overline{RAS}$ low pulse width for read write cycle (Note 24)	85	125000	100	125000	115	125000	ns
t_{CP}	$\overline{CAS}$ high pulse width (Note 25)	8	12	10	15	10	15	ns
t_{CPRH}	$\overline{RAS}$ hold time after $\overline{CAS}$ precharge	30		35		40		ns
t_{CPWD}	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low (Note 22)	53		60		65		ns

Note 23: All previously specified timing requirements and switching characteristics are applicable to their respective fast page mode cycle.

24: $t_{RAS(min)}$ is specified as two cycles of $\overline{CAS}$ input are performed.

25: $t_{CP(max)}$ is specified as a reference point only.

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 26)

Symbol	Parameter	Limits						Unit
		M5M417800C-5,-5S		M5M417800C-6,-6S		M5M417800C-7,-7S		
		Min	Max	Min	Max	Min	Max	
t_{CSR}	$\overline{CAS}$ setup time before $\overline{RAS}$ low	10		10		10		ns
t_{CHR}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	10		10		15		ns
t_{RSR}	Read setup time before $\overline{RAS}$ low	10		10		10		ns
t_{RHR}	Read hold time after $\overline{RAS}$ low	10		10		15		ns

Note 26: Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles instead of eight $\overline{RAS}$ cycles are necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

PRELIMINARY
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FAST PAGE MODE 16777216-BIT (2097152-WORD BY 8-BIT) DYNAMIC RAM

SELF REFRESH SPECIFICATIONS

Self refresh devices are denoted by "S" after speed item, like -5S/-6S/-7S. The other characteristics and requirements than the below are same as normal devices.

ELECTRICAL CHARACTERISTICS (Ta=0~70°C, Vcc=5V±10%, Vss=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
$I_{CC8\ (AV)}$	Average supply current from Vcc Slow-Refresh cycle (Note 5)	M5M417800C (S)	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling or $\overline{RAS}$ cycling & $\overline{CAS}$ ≦0.2V $\overline{OE}$ & $\overline{WE}$ ≦ 0.2V or $\overline{OE}$ & $\overline{WE}$ ≧ Vcc-0.2V $A_0 \sim A_{11}$ ≦ 0.2V or $A_0 \sim A_{11}$ ≧ Vcc-0.2V t_{REF}=128ms (2048cycles) output = OPEN $t_{RAS}=t_{RAS}$min. ~1 μs			500	μA
$I_{CC9\ (AV)}$*	Average supply current from Vcc Self-Refresh cycle (Note 5)	M5M417800C (S)	$\overline{RAS}$ = $\overline{CAS}$ ≦ 0.2V output = OPEN			200	μA

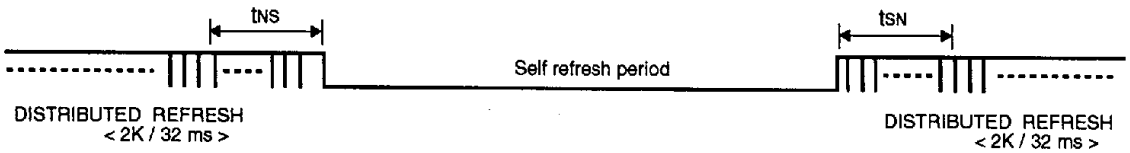
TIMING REQUIREMENTS (Ta=0~70°C, Vcc=5V±10%, Vss=0V, unless otherwise noted, see notes 12, 13)

Symbol	Parameter	Limits						Unit
		M5M417800C-5S		M5M417800C-6S		M5M417800C-7S		
		Min	Max	Min	Max	Min	Max	
t_{RASS}	Self Refresh $\overline{RAS}$ low pulse width	100		100		100		μs
t_{RPS}	Self Refresh $\overline{RAS}$ high precharge time	90		110		130		ns
t_{CHS}	Self Refresh $\overline{RAS}$ hold time	-50		-50		-50		ns
t_{RSR}	Read setup time before $\overline{RAS}$ low	10		10		10		ns
t_{RHR}	Read hold time after $\overline{RAS}$ low	10		10		15		ns

SELF REFRESH ENTRY & EXIT CONDITIONS

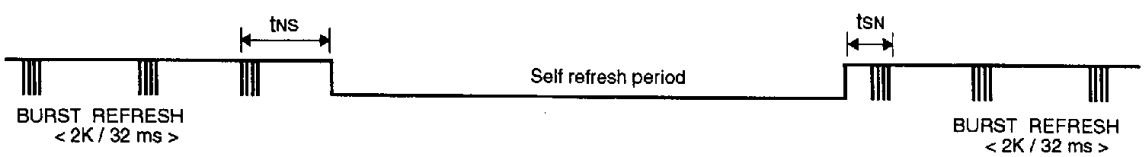
(1) In case of distributed refresh

The last / first full refresh cycles (2K) must be made within t_{NS} / t_{SN} before / after self refresh, on the condition of t_{NS}≦32ms and t_{SN}≦32ms.



(2) In case of burst refresh

The last / first full refresh cycles (2K) must be made within t_{NS} / t_{SN} before / after self refresh, on the condition of $t_{NS}+t_{SN}$≦32ms.

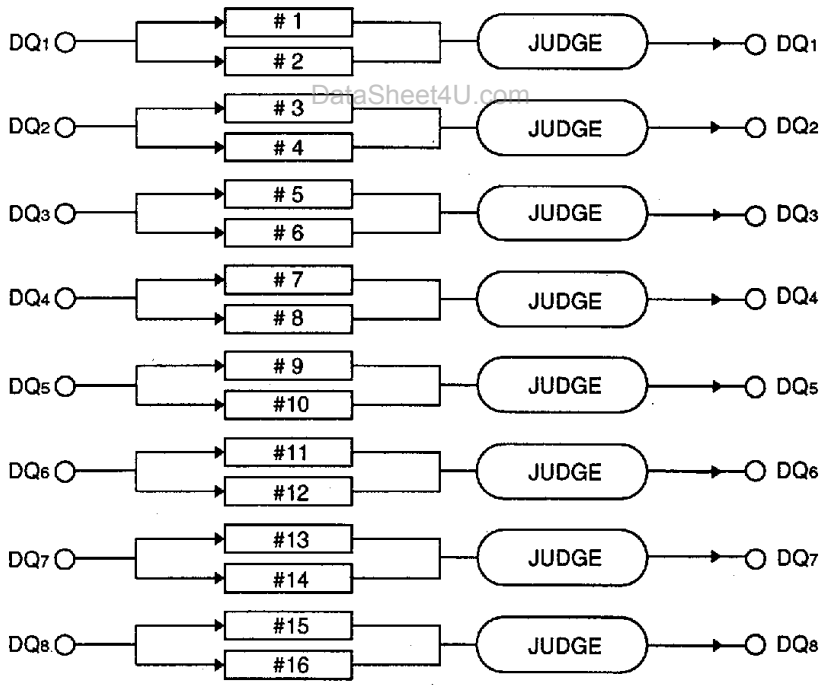


PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

TEST Mode SET Cycle

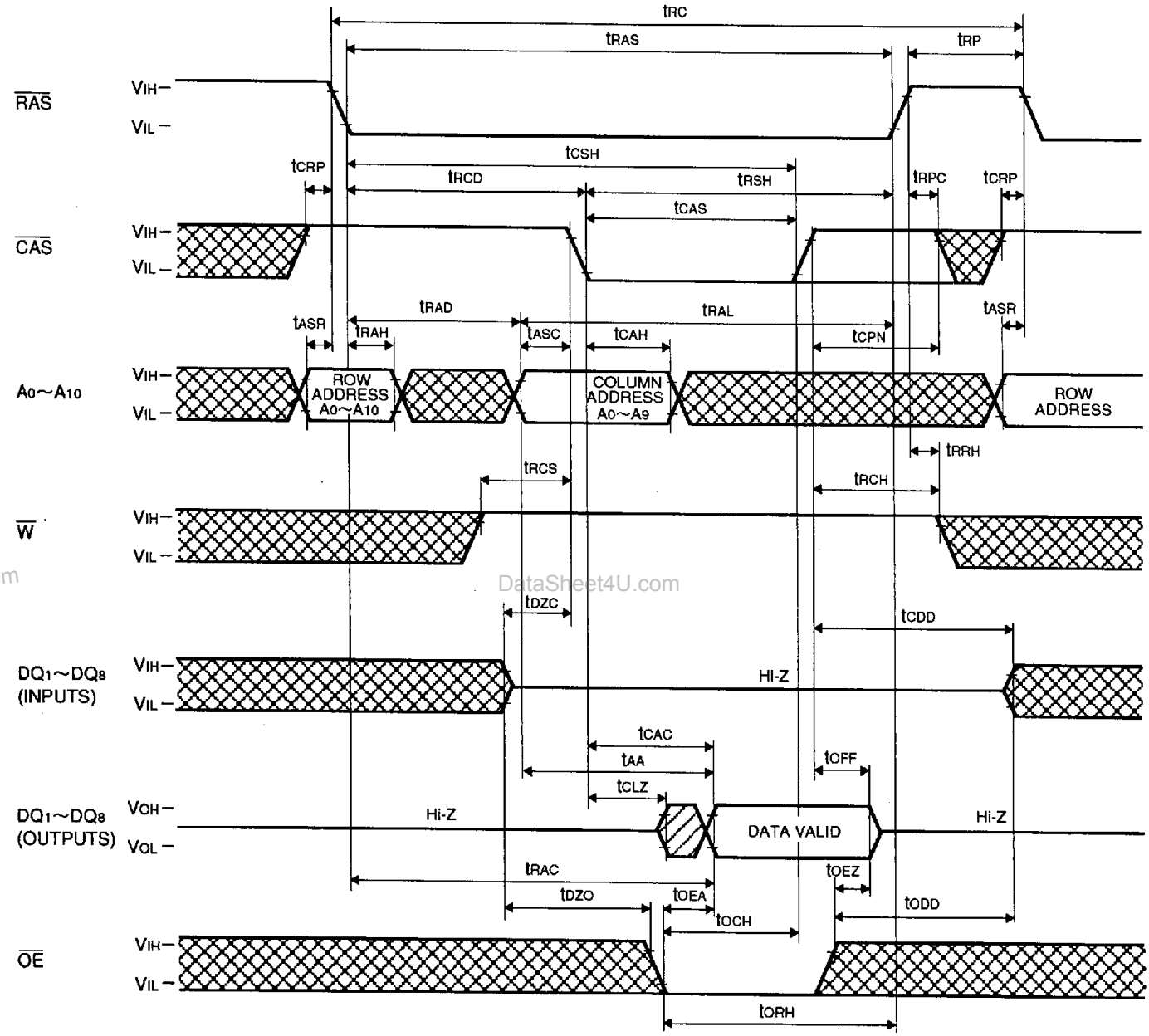
Symbol	Parameter	Limits						Unit
		M5M417800C-5,-5S		M5M417800C-6,-6S		M5M417800C-7,-7S		
		Min	Max	Min	Max	Min	Max	
tWSR	$\overline{W}$ setup time before $\overline{RAS}$ low	10		10		10		ns
tWHR	$\overline{W}$ hold time after $\overline{RAS}$ low	10		10		15		ns

Note 27: The test mode function is initiated by a $\overline{W}$ and $\overline{CAS}$ before $\overline{RAS}$ cycle (WCBR cycle) as specified in timing diagram.
The test mode function is terminated by either a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle (CBR refresh cycle) or a $\overline{RAS}$ only refresh cycle.
During the test mode, the device is internally organized as 16-bits wide (1M bytes depth). No addressing of CA0 is required.
During a write cycle, data must be applied to all DQ (input) pins. The data can be different between DQ pins. The data on each DQ pin is written into 2-bits memory cells, respectively. During a read cycle, each DQ (output) pin shows the test result of the 2-bits, respectively. High state indicates that they are same. Low state indicates that they are not same.
During the test mode operation, only WCBR cycle can be used to perform refresh.



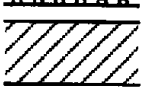
Timing Diagrams (Note 28)

Read Cycle



Note 28

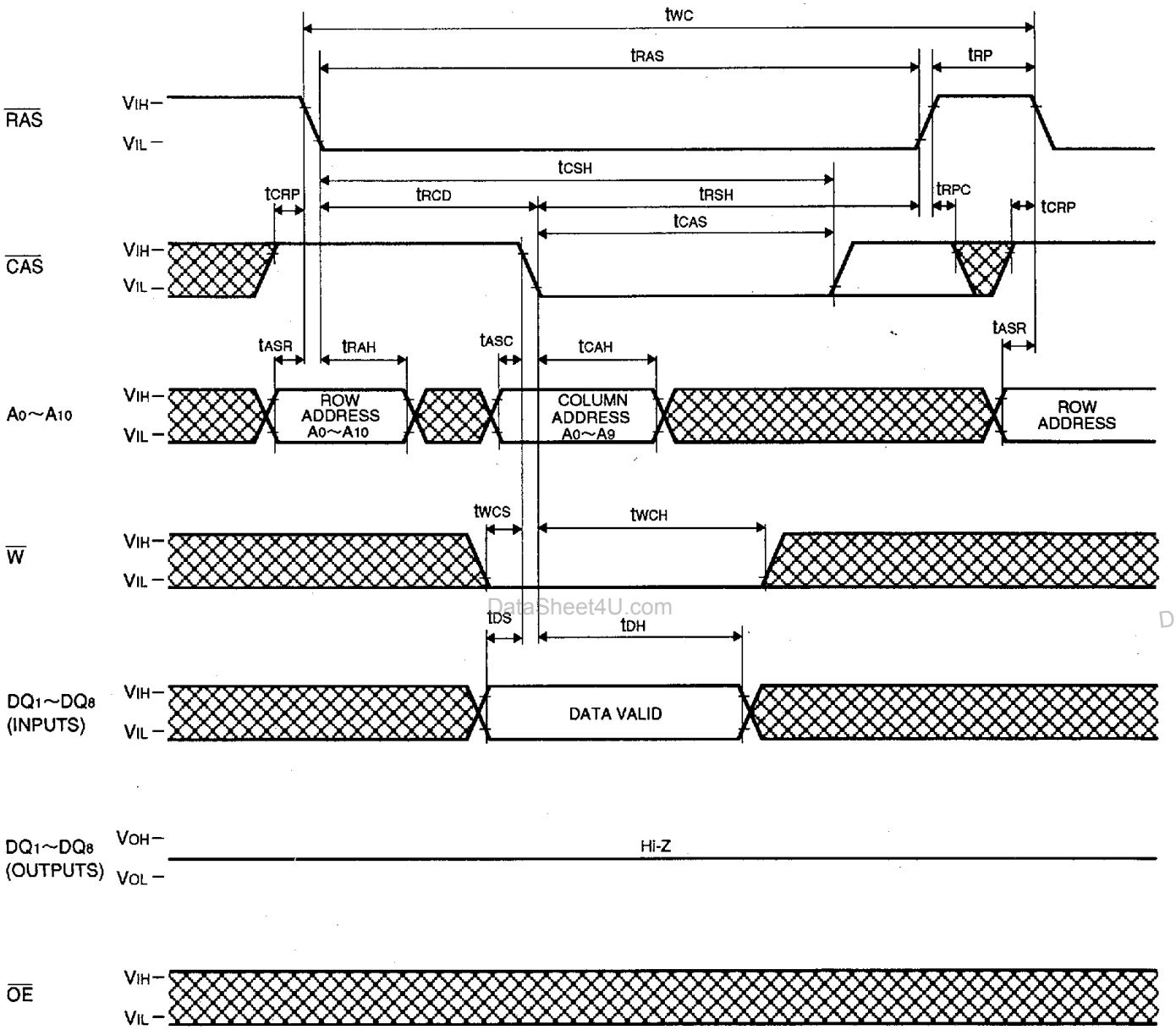
Indicates the don't care input.
VIH(min)≦VIN≦VIH(max) or VIL(min)≦VIN≦VIL(max)



Indicates the invalid output.

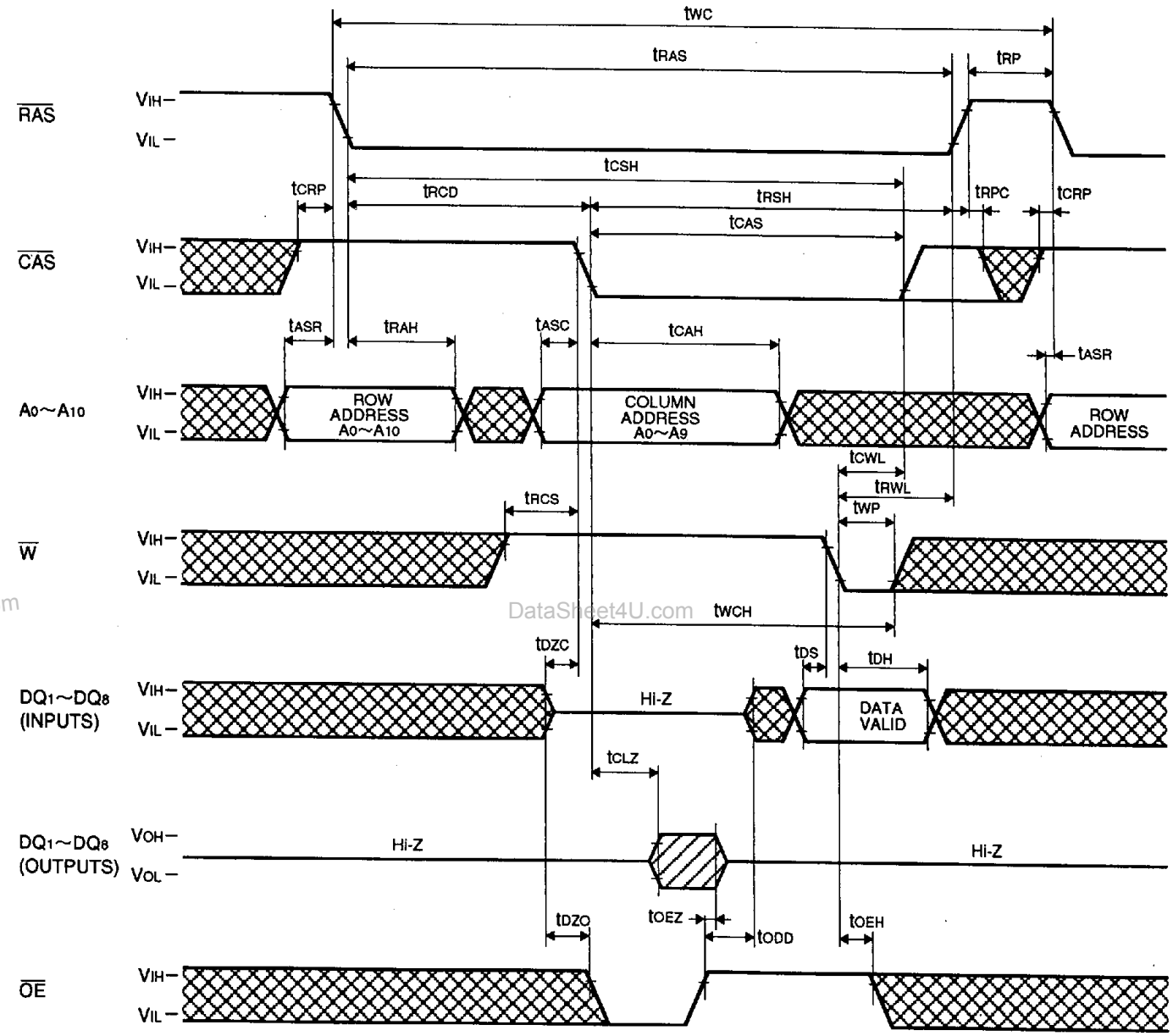
PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change

Write Cycle (Early write)



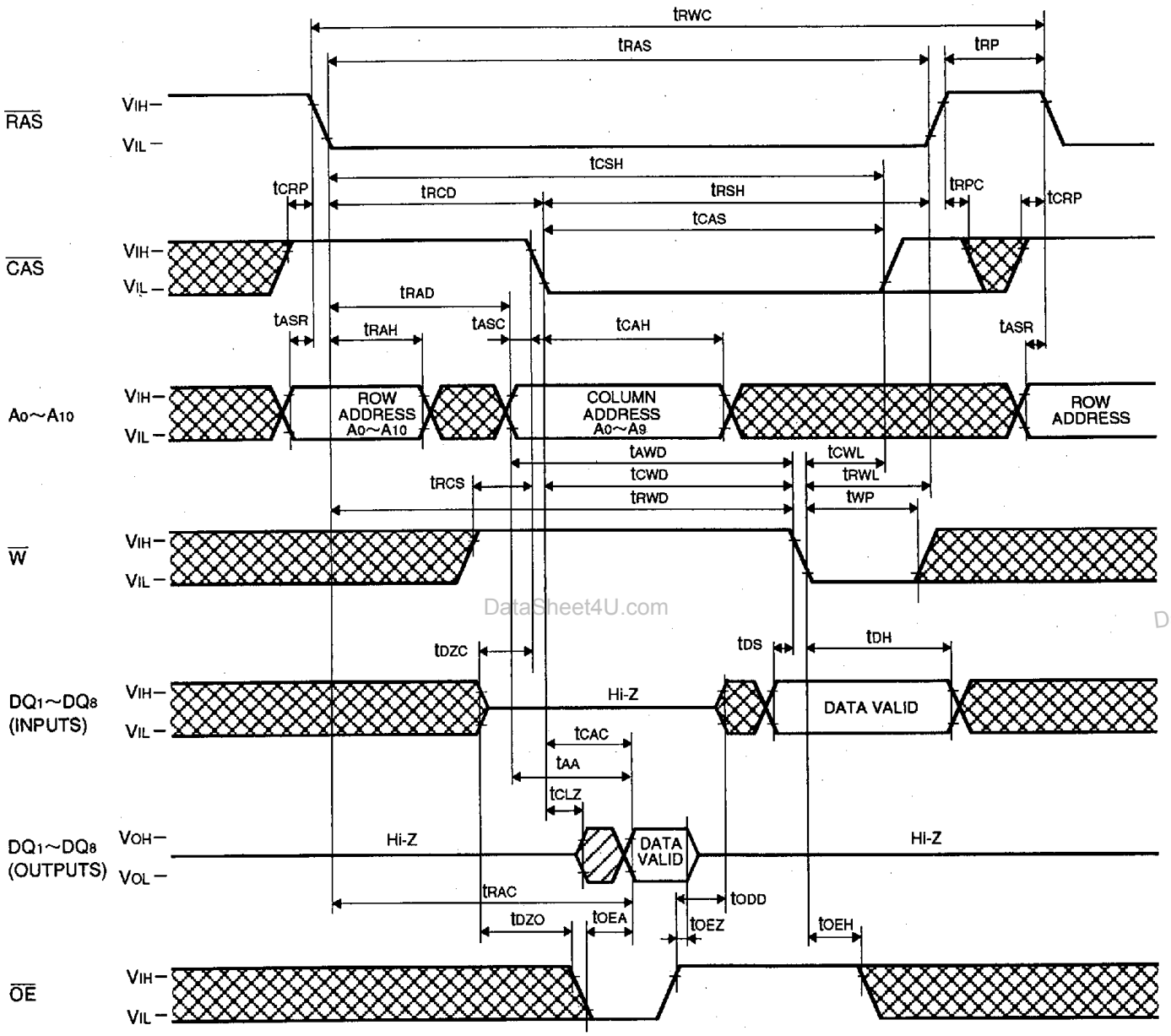
PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Write Cycle (Delayed write)



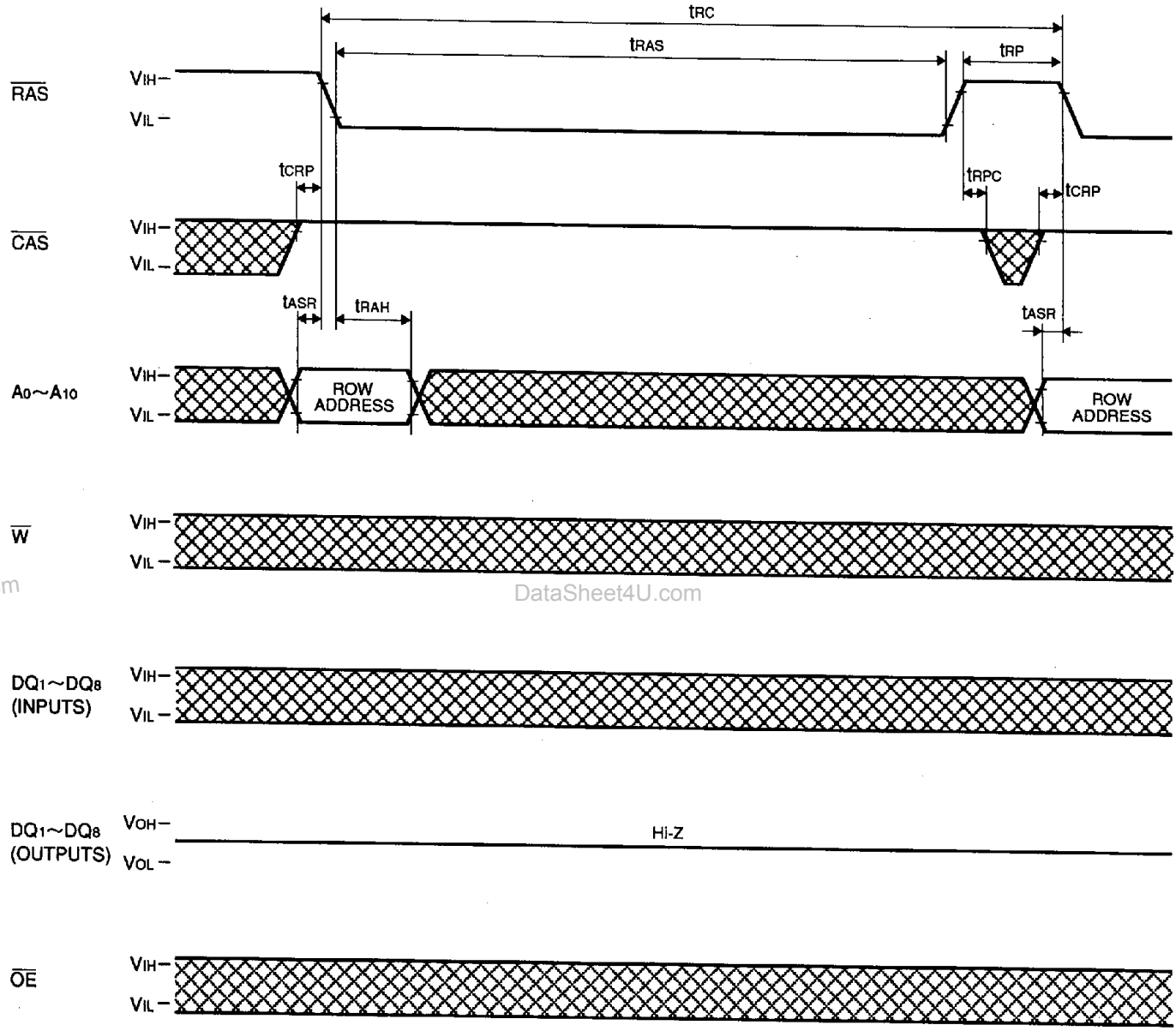
PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Read-Write, Read-Modify-Write Cycle



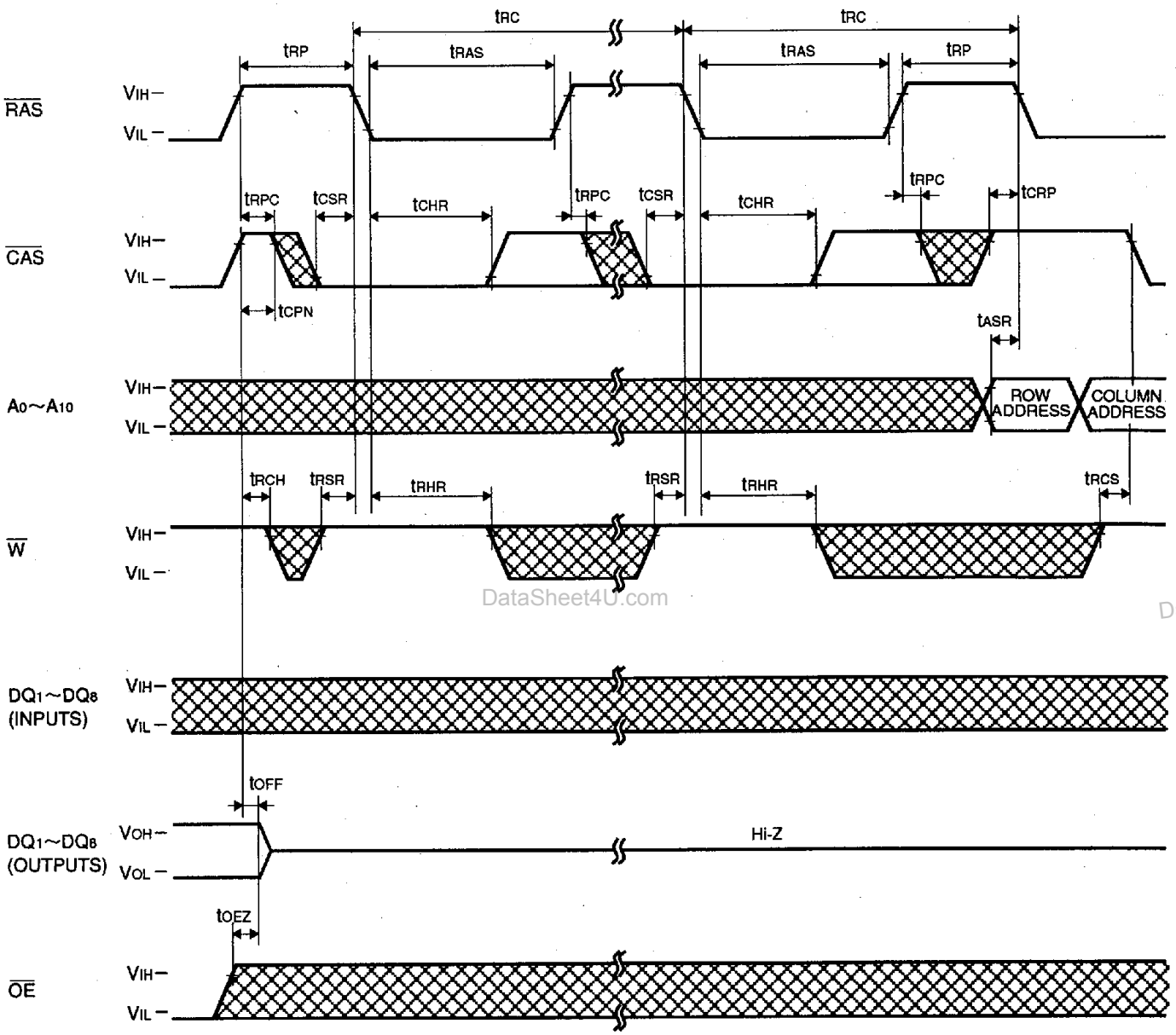
PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

$\overline{RAS}$-only Refresh Cycle



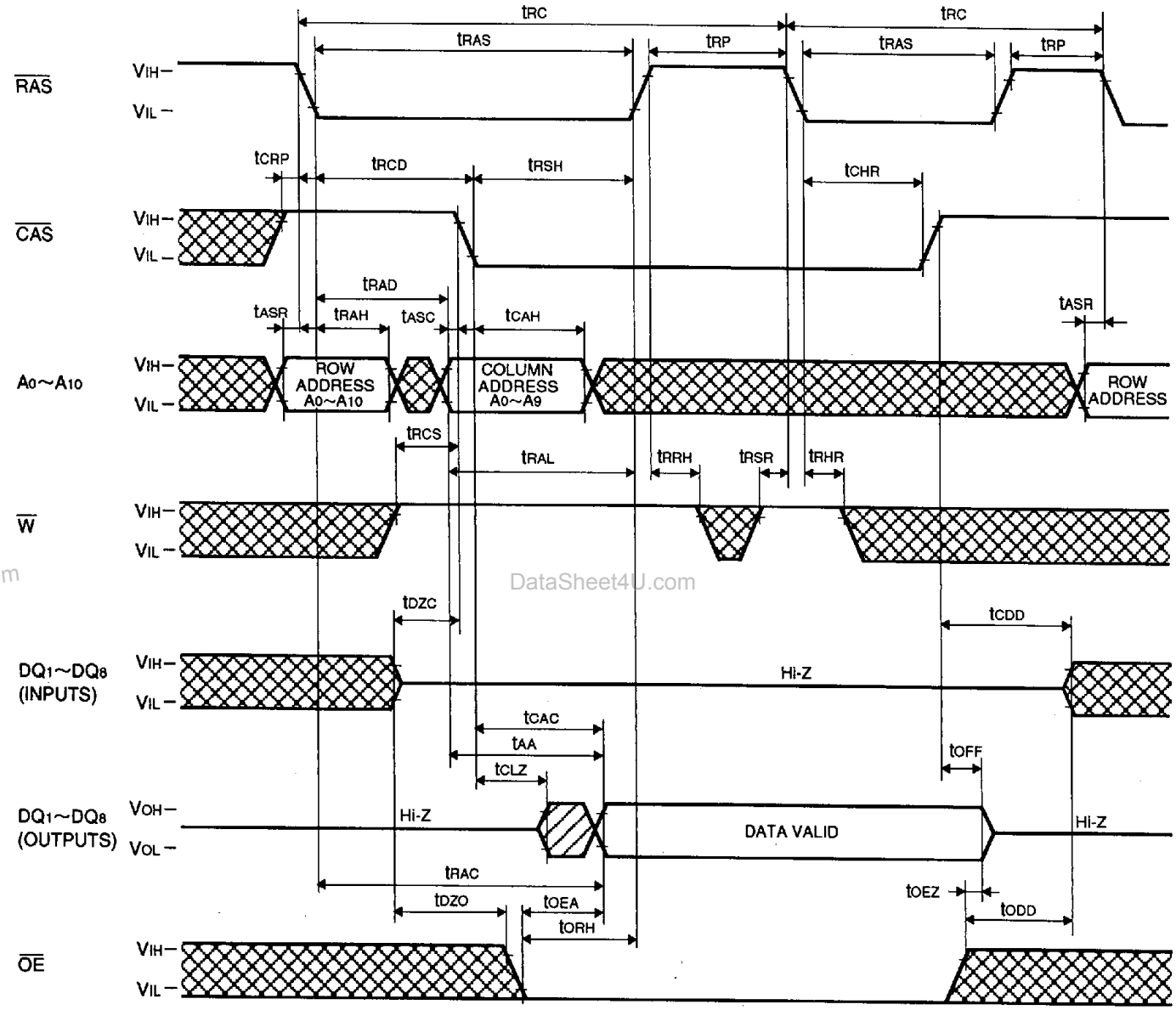
PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle, Slow Refresh Cycle



PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

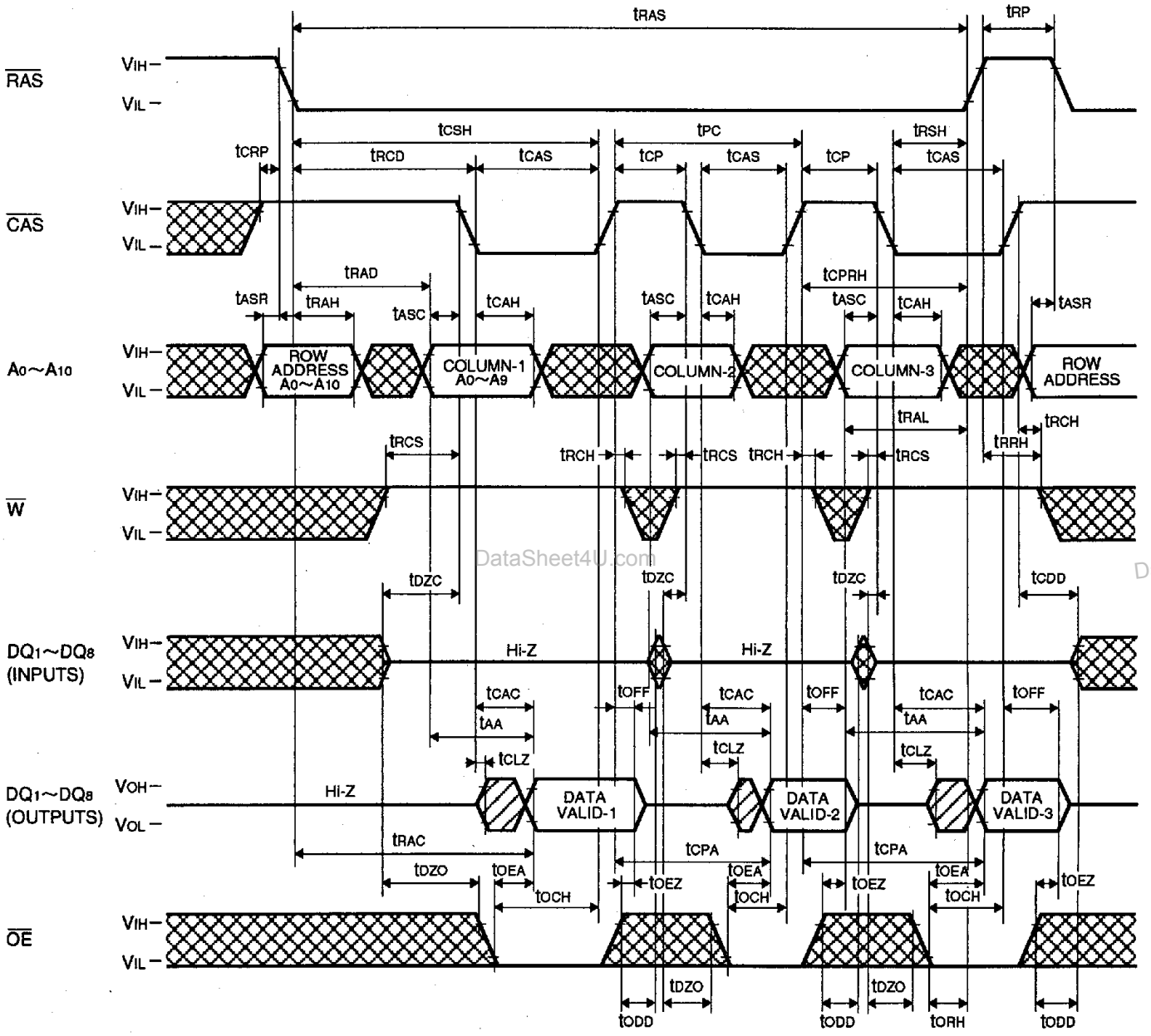
Hidden Refresh Cycle (Read) (Note 29)



Note 29: Early write, delayed write, read write or read modify write cycle is applicable instead of read cycle.
Timing requirements and output state are the same as that of each cycle shown above.
And in any cycle, tRSR&tRHR should be satisfied not to enter TEST MODE .

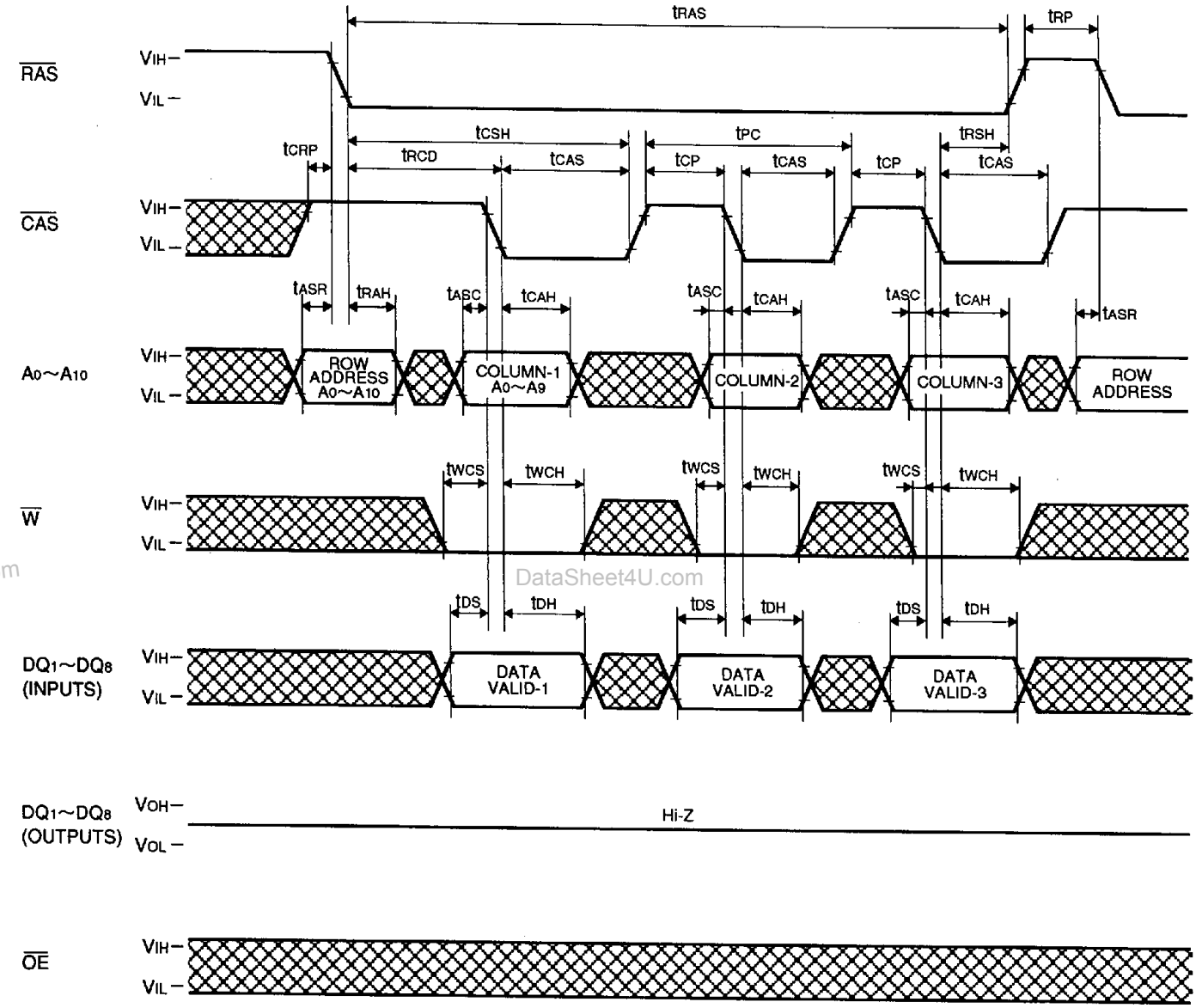
PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Fast Page Mode Read Cycle



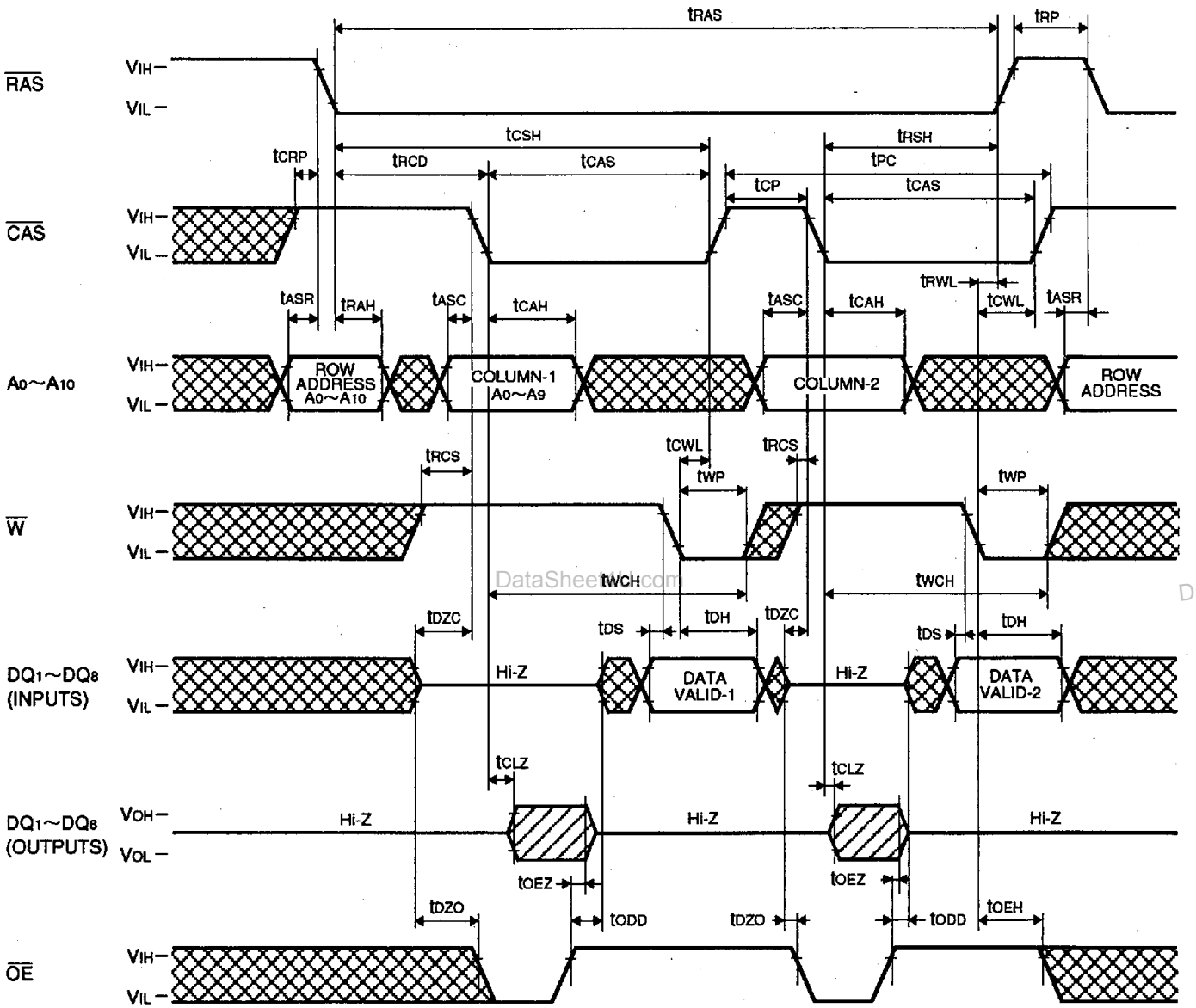
PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Fast Page Mode Write Cycle (Early Write)



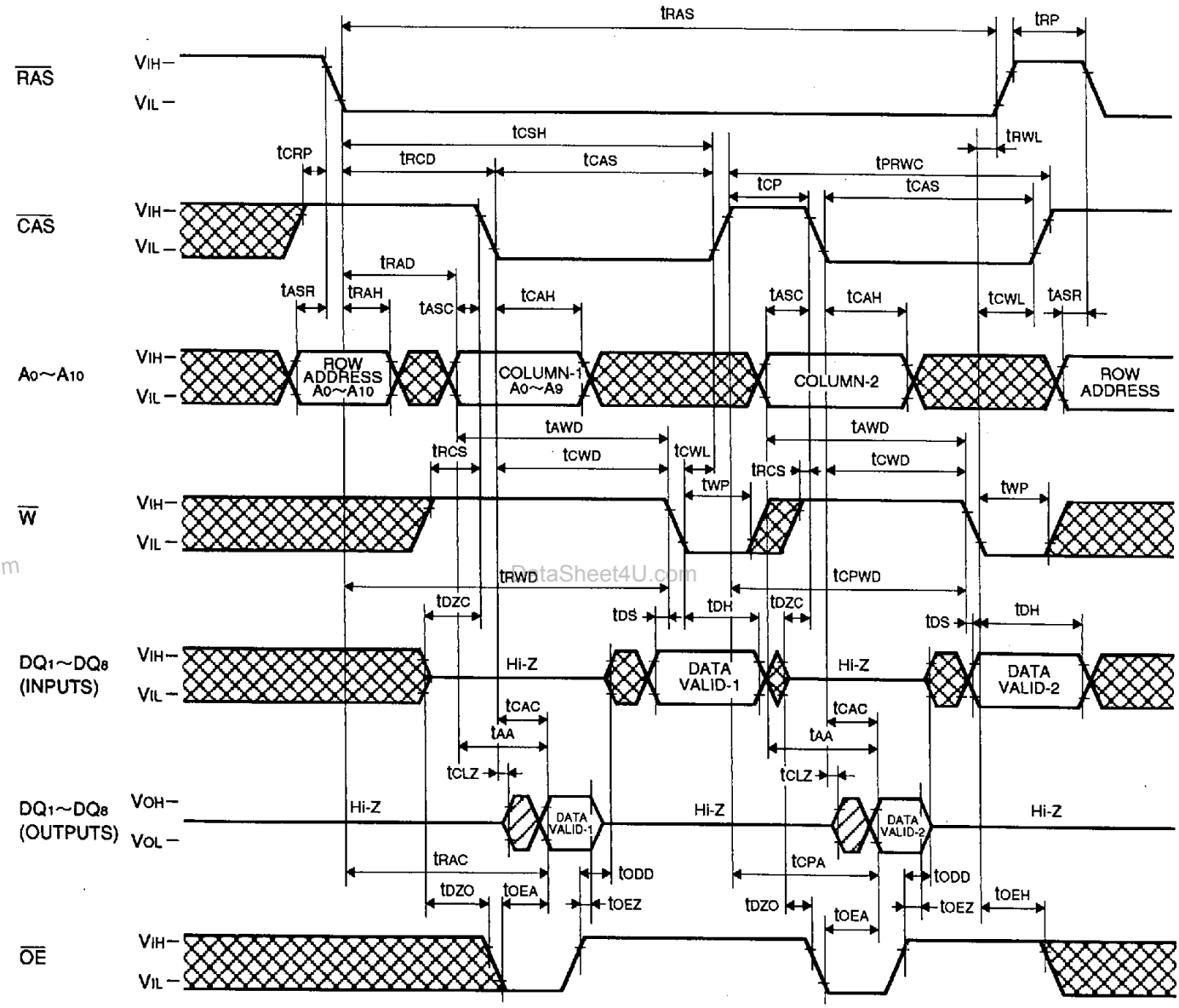
PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Fast-Page Mode Write Cycle (Delayed Write)

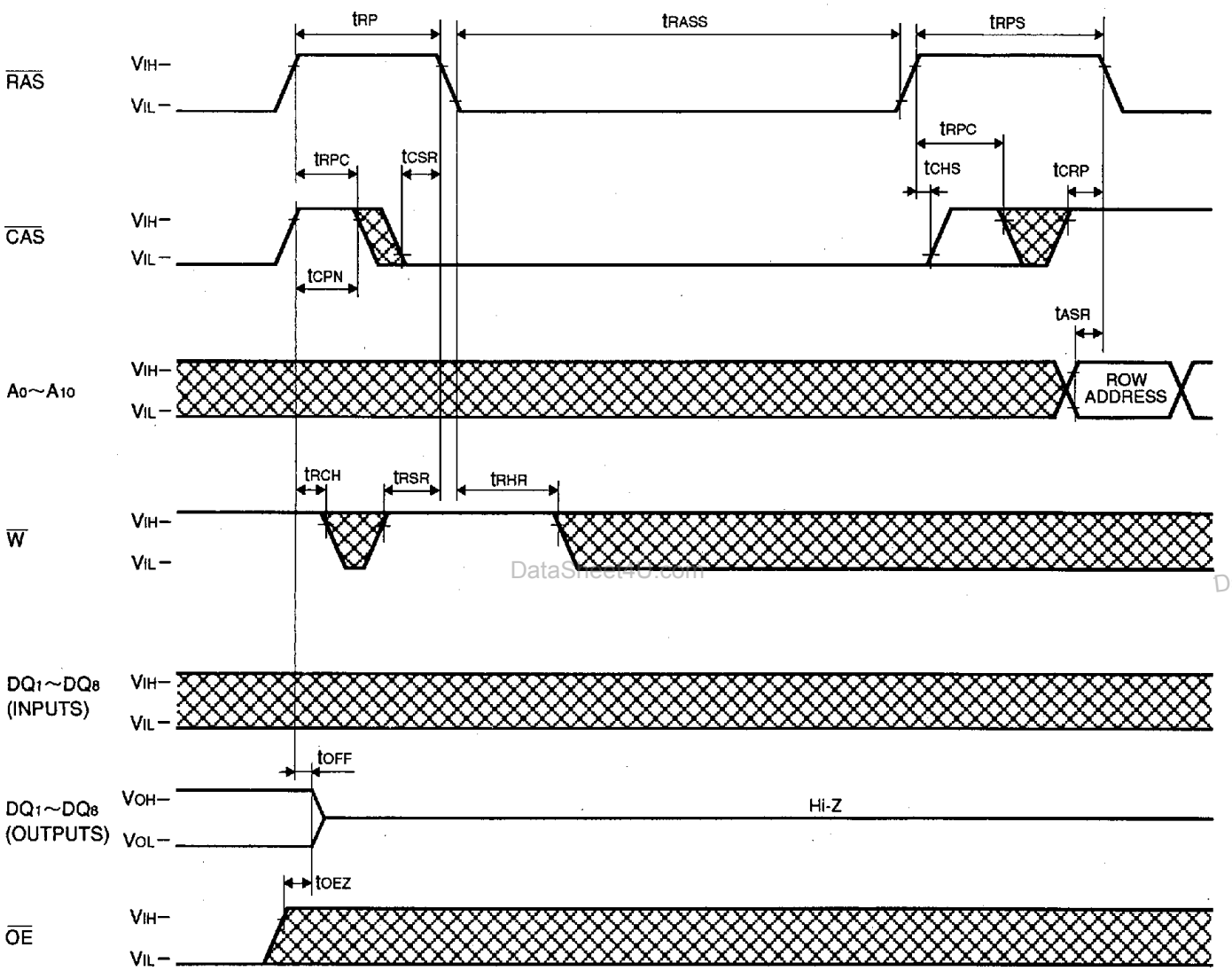


PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Fast Page Mode Read-Write, Read-Modify-Write Cycle

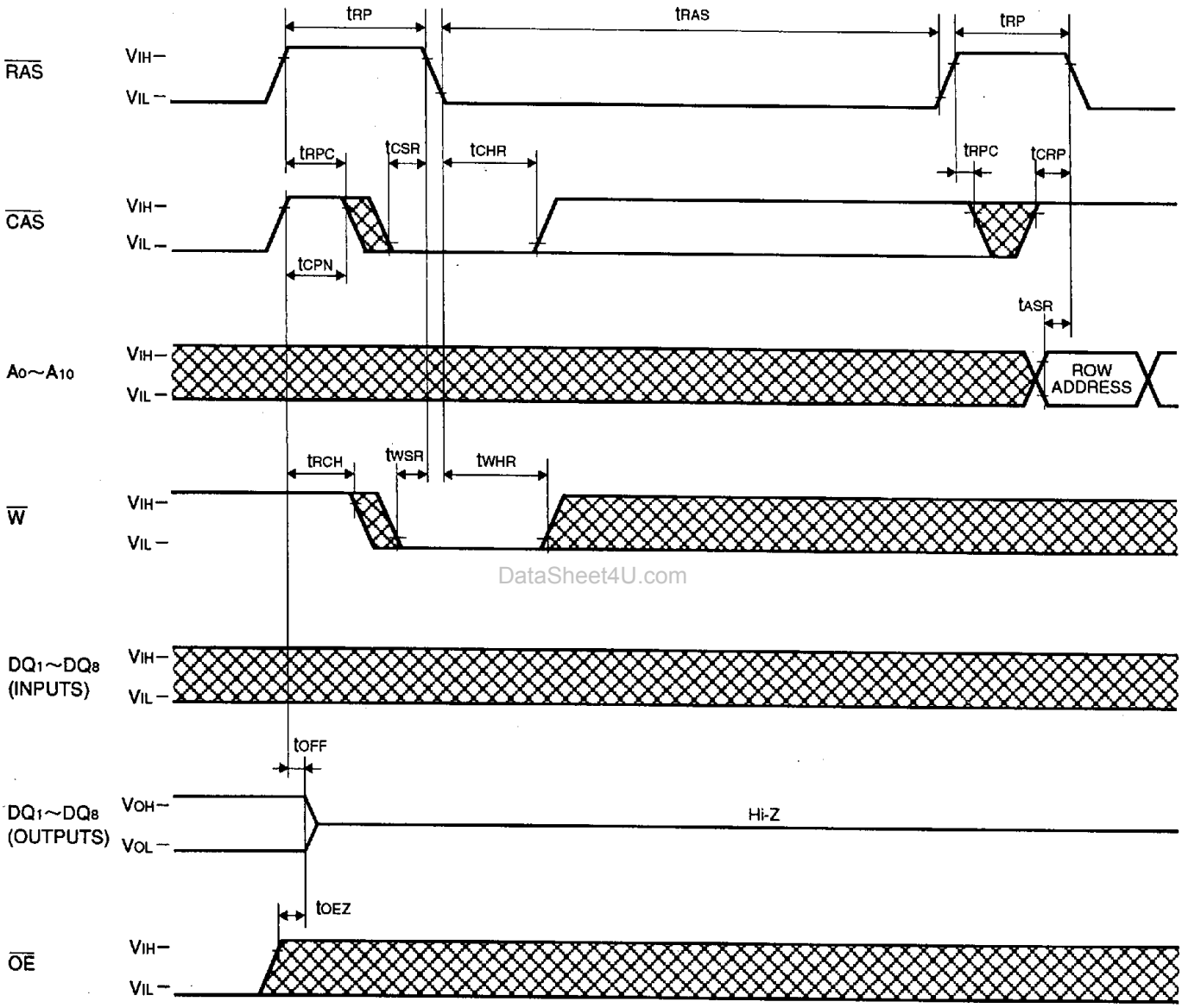


Self Refresh Cycle



PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

TEST Mode SET Cycle



Note 30: This cycle can be used for initialized cycle after power-up, however entried into Test Mode.