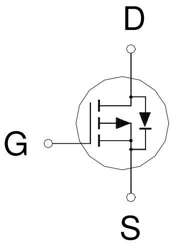
P-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

BV_{DSS}	-30V
$R_{DSON\ (MAX.)}$	44mΩ
I_D	-4A



Pb-Free Lead Plating & Halogen Free

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V_{GS}	±12	V
Continuous Drain Current	T_A = 25 °C	I_D	-4	A
	T_A = 70 °C		-3	
Pulsed Drain Current[1]		I_{DM}	-16	
Power Dissipation	T_A = 25 °C	P_D	1.25	W
	T_A = 70 °C		0.8	
Operating Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150	°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Ambient[3]	$R_{\theta JA}$		100	°C / W
Junction-to-Lead[4]	$R_{\theta JL}$		55	

[1] Pulse width limited by maximum junction temperature.

[2] Duty cycle ≤ 1%

[3] 100°C / W when mounted on a 1 in^2 pad of 2 oz copper.

[4] $R_{\theta JA}$ is the sum of the thermal impedance from junction to lead $R_{\theta JL}$ and lead to ambient.

ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = -250μA	-30			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -250μA	-0.3	-0.75	-1.2	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0V, V_{GS} = ±12V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -24V, V_{GS} = 0V			-1	μA
		V_{DS} = -20V, V_{GS} = 0V, T_J = 125 °C			-10	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = -5V, V_{GS} = -4.5V	-4			A
Drain-Source On-State Resistance[1]	$R_{DS(ON)}$	V_{GS} = -10V, I_D = -4.5A		32	38	mΩ
		V_{GS} = -4.5V, I_D = -4A		39	44	
		V_{GS} = -2.5V, I_D = -3A		60	75	
Forward Transconductance[1]	g_{fs}	V_{DS} = -5V, I_D = -4A		13		S
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0V, V_{DS} = -15V, f = 1MHz		1170		pF
Output Capacitance	C_{oss}			185		
Reverse Transfer Capacitance	C_{rss}			137		
Total Gate Charge[1,2]	Q_g	V_{DS} = -15V, V_{GS} = -4.5V, I_D = -4A		14.2		nC
Gate-Source Charge[1,2]	Q_{gs}			3.2		
Gate-Drain Charge[1,2]	Q_{gd}			4.1		
Turn-On Delay Time[1,2]	$t_{d(on)}$	V_{DS} = -15V, I_D = -1A, V_{GS} = -4.5V, R_{GS} = 6Ω		10		nS
Rise Time[1,2]	t_r			10		
Turn-Off Delay Time[1,2]	$t_{d(off)}$			45		
Fall Time[1,2]	t_f			15		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25 °C)						
Continuous Current	I_S				-3	A
Pulsed Current[3]	I_{SM}				-12	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0V			-1.2	V

[1] Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.

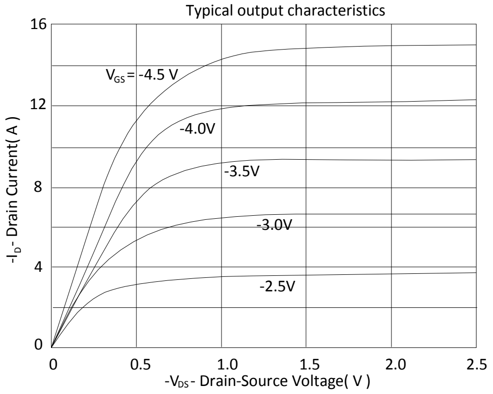
[2] Independent of operating temperature.

[3] Pulse width limited by maximum junction temperature.

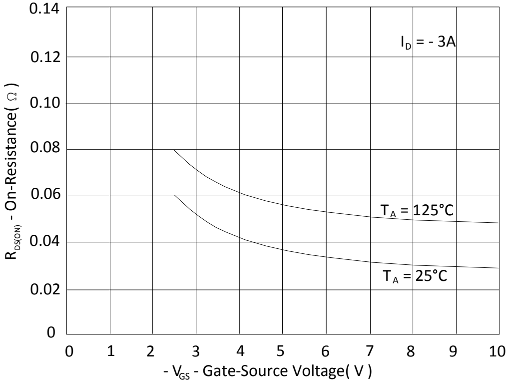
EMC will review datasheet by quarter, and update new version.

TYPICAL CHARACTERISTICS

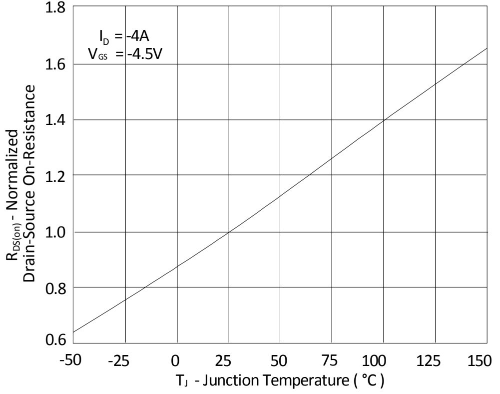
Typical output characteristics



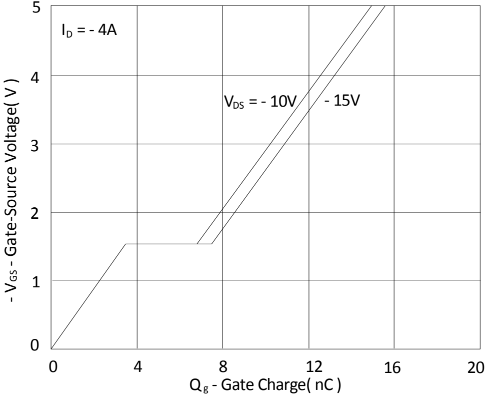
On-Resistance Variation with Gate-Source Voltage



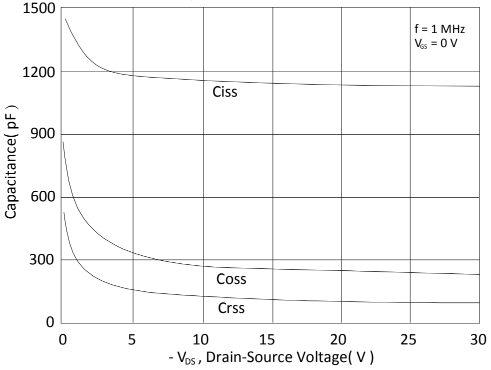
Normalized on-Resistance v.s. Junction Temperature



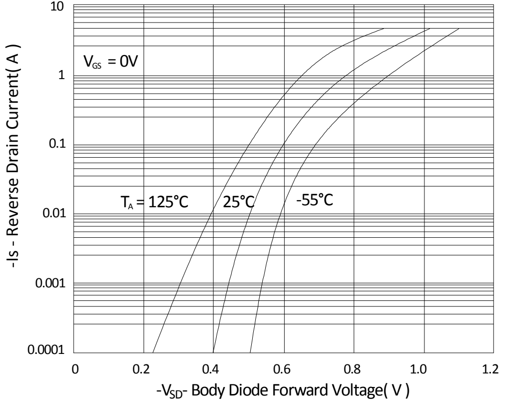
Gate Charge Characteristics

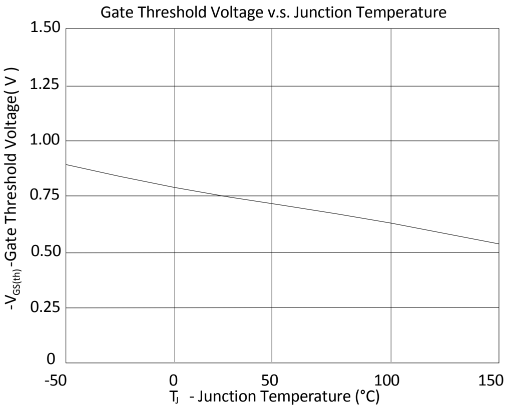


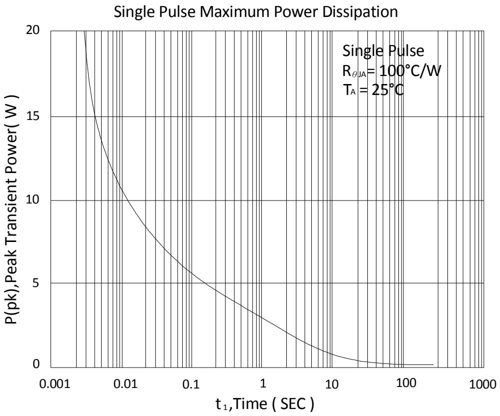
Capacitance Characteristics

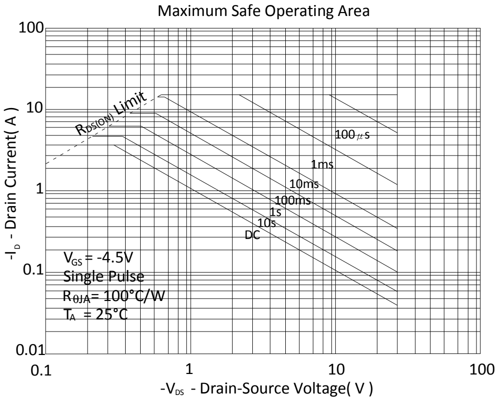


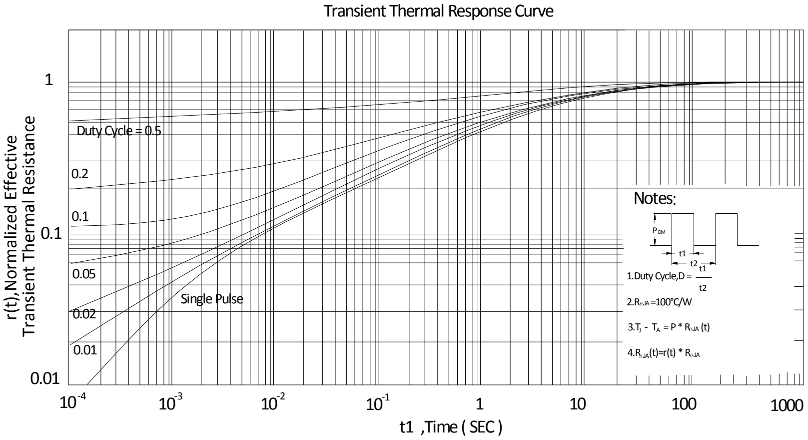
Body Diode Forward Voltage Variation
with Source Current and Temperature




Gate Threshold Voltage v.s. Junction Temperature

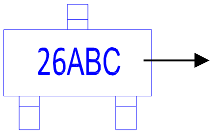

Single Pulse Maximum Power Dissipation


Maximum Safe Operating Area


Transient Thermal Response Curve

Ordering & Marking Information:

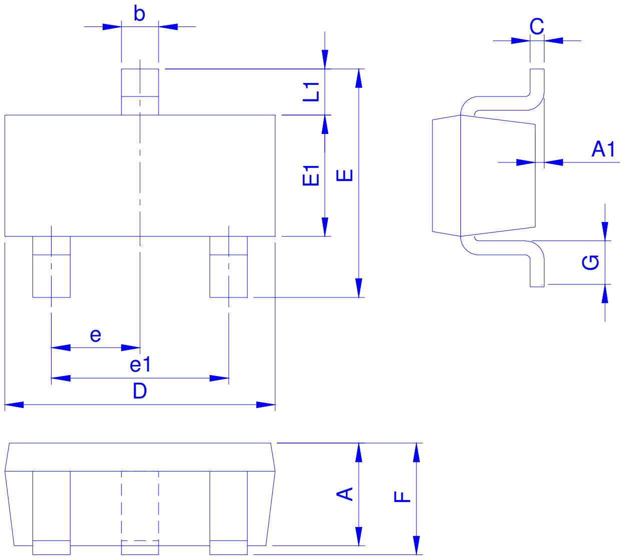
Device Name: EMF44P03J for SOT23-3



26: Device Code, 26 for EMF44P03J

ABC: Date Code

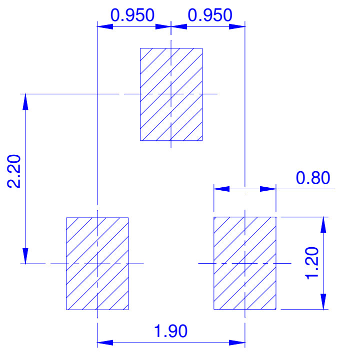
Outline Drawing



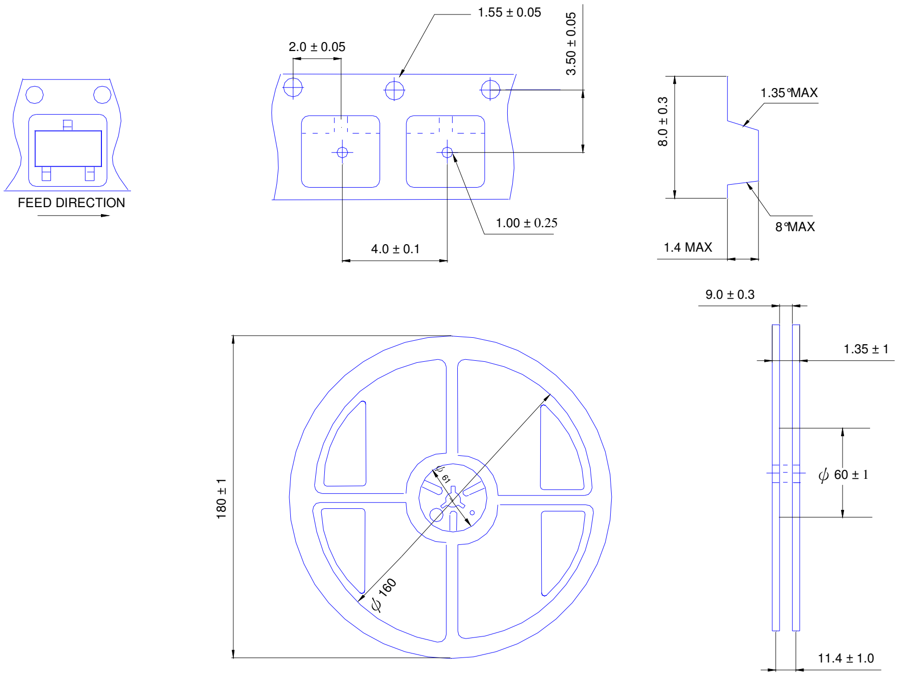
Dimension in mm

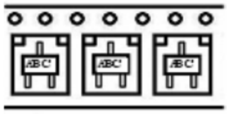
Dimension	A	A1	b	C	D	E	E1	e	e1	F	G	L1
Min.	0.70	-	0.30	0.080	2.80	2.10	1.20	0.90	1.80	0.80	0.30	0.54
Typ.	0.95	-	0.40	0.127	2.90	2.50	1.30	0.95	1.90	0.95	0.40	0.57
Max.	1.20	0.15	0.50	0.202	3.10	3.00	1.80	1.00	2.00	1.25	0.60	0.70

Footprint



◆ Tape&Reel Information:3000pcs/Reel



產品別	SOT23-3
Reel 尺寸	7”
編帶方式	FEED DIRECTION → 
前空格	50
後空格	50
裝箱數	
滿捲數量	3K
捲/內盒比	5：1
內盒滿箱數	15K
內/外箱比	12：1
外箱滿箱數	180K