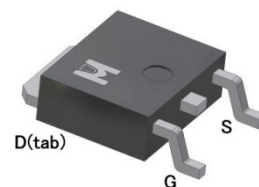


N-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

BV_{DSS}	15V
$R_{DS(on)} (MAX.)$	7m Ω
I_D	65A



UIS, Rg 100% Tested

Pb-Free Lead Plating & Halogen Free



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V_{GS}	± 8	V
Continuous Drain Current	$T_C = 25^\circ\text{C}$	I_D	65	A
	$T_C = 100^\circ\text{C}$		41	
Pulsed Drain Current ¹		I_{DM}	160	
Avalanche Current		I_{AS}	35	
Avalanche Energy	$L = 0.1\text{mH}, I_D = 35\text{A}, R_G = 25\Omega$	E_{AS}	61.25	mJ
Power Dissipation	$T_C = 25^\circ\text{C}$	P_D	50	W
	$T_C = 100^\circ\text{C}$		20	
Operating Junction & Storage Temperature Range		T_{j}, T_{stg}	-55 to 150	$^\circ\text{C}$

100% UIS testing in condition of $V_D = 15\text{V}$, $L = 0.1\text{mH}$, $V_G = 10\text{V}$, $I_L = 20\text{A}$, Rated $V_{DS} = 15\text{V}$ N-CH

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	$R_{\theta JC}$		2.5	$^\circ\text{C} / \text{W}$
Junction-to-Ambient ³	$R_{\theta JA}$		75	

¹Pulse width limited by maximum junction temperature.

²Duty cycle $\leq 1\%$

³75 $^\circ\text{C} / \text{W}$ when mounted on a 1 in² pad of 2 oz copper.

ELECTRICAL CHARACTERISTICS ($T_J = 25\text{ }^{\circ}\text{C}$, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0V, I _D = 250μA	15			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250μA	0.35	0.6	0.9	
Gate-Body Leakage	I _{GSS}	V _{DS} = 0V, V _{GS} = ±8V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 12V, V _{GS} = 0V			1	μA
		V _{DS} = 10V, V _{GS} = 0V, T _J = 125 °C			10	
On-State Drain Current ¹	I _{D(ON)}	V _{DS} = 5V, V _{GS} = 4.5V	65			A
Drain-Source On-State Resistance ¹	R _{DS(ON)}	V _{GS} = 4.5V, I _D = 18A		5.8	7	mΩ
		V _{GS} = 2.5V, I _D = 15A		6.5	8	
		V _{GS} = 1.8V, I _D = 10A		7.5	10	
Forward Transconductance ¹	g _{fs}	V _{DS} = 5V, I _D = 18A		22		S
DYNAMIC						
Input Capacitance	C _{iss}	V _{GS} = 0V, V _{DS} = 10V, f = 1MHz		2091		pF
Output Capacitance	C _{oss}			250		
Reverse Transfer Capacitance	C _{rss}			172		
Gate Resistance	R _g	V _{GS} = 15mV, V _{DS} = 0V, f = 1MHz		1.8		Ω
Total Gate Charge ^{1,2}	Q _g	V _{DS} = 10V, V _{GS} = 4.5V, I _D = 18A		19		nC
Gate-Source Charge ^{1,2}	Q _{gs}			2.3		
Gate-Drain Charge ^{1,2}	Q _{gd}			4		
Turn-On Delay Time ^{1,2}	t _{d(on)}	V _{DS} = 10V, I _D = 1A, V _{GS} = 4.5V, R _{GS} = 6Ω		10		nS
Rise Time ^{1,2}	t _r			15		
Turn-Off Delay Time ^{1,2}	t _{d(off)}			50		
Fall Time ^{1,2}	t _f			18		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T _c = 25 °C)						
Continuous Current	I _S				65	A
Forward Voltage ¹	V _{SD}	I _F = I _S , V _{GS} = 0V			1.3	V
Reverse Recovery Time	t _{rr}			30		nS
Reverse Recovery Charge	Q _{rr}			20		nC

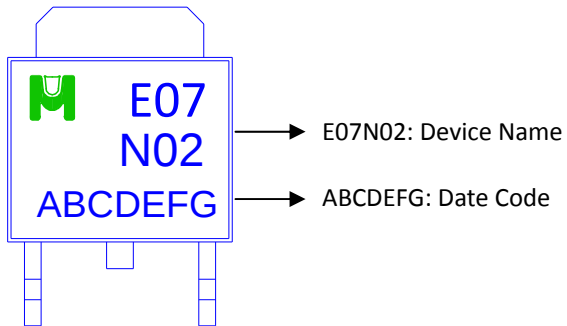
¹Pulse test : Pulse Width $\leq 300\text{ }\mu\text{sec}$, Duty Cycle $\leq 2\%$.

²Independent of operating temperature.

³Pulse width limited by maximum junction temperature.

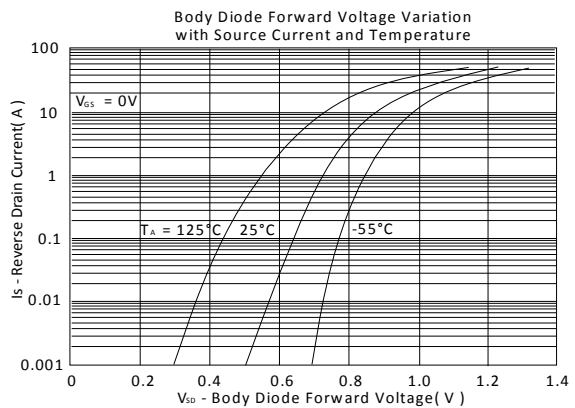
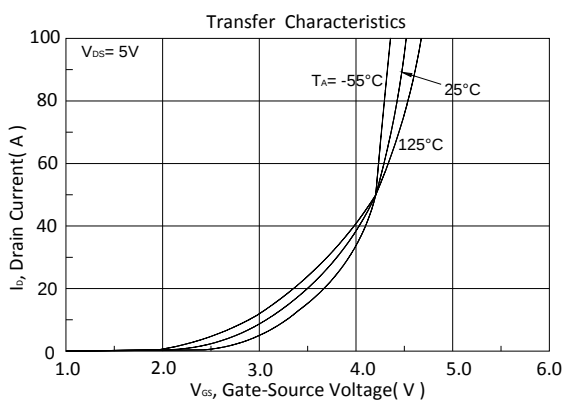
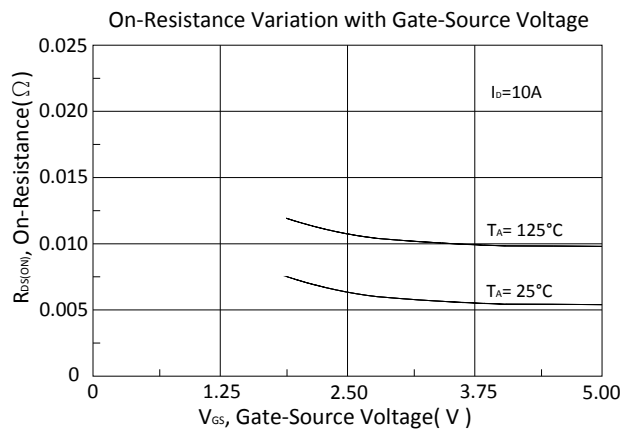
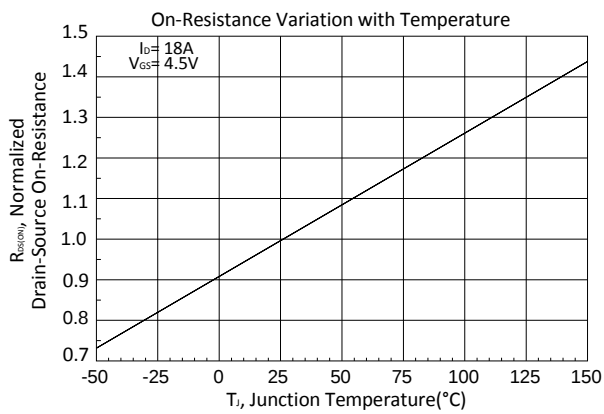
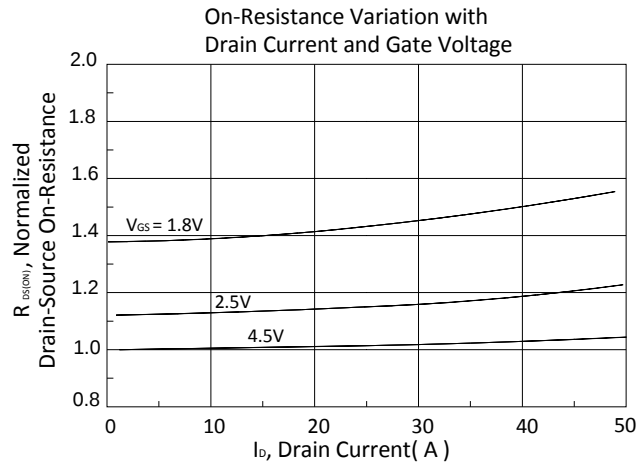
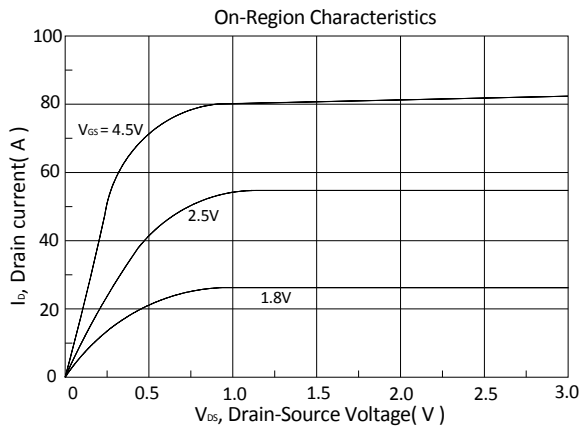
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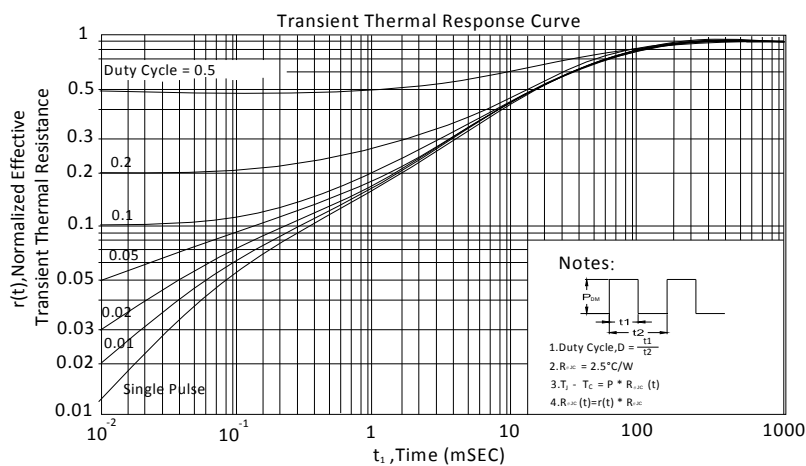
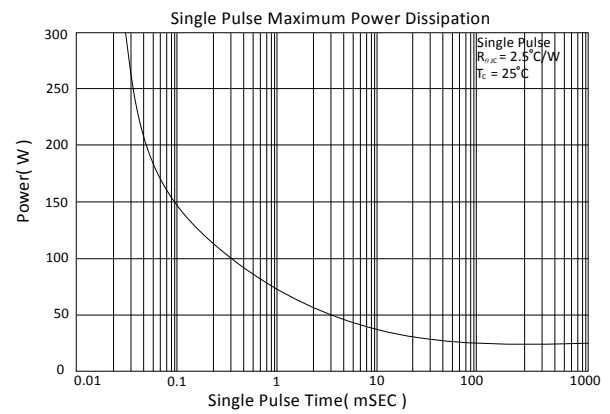
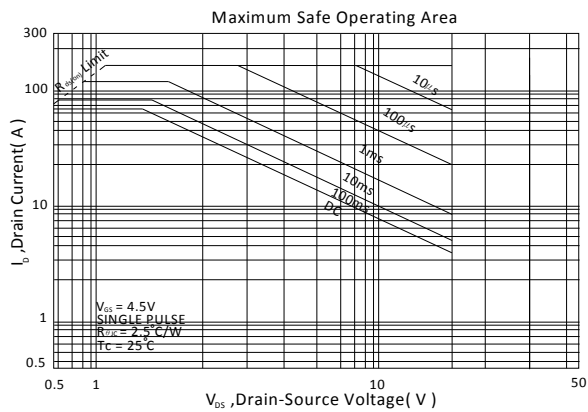
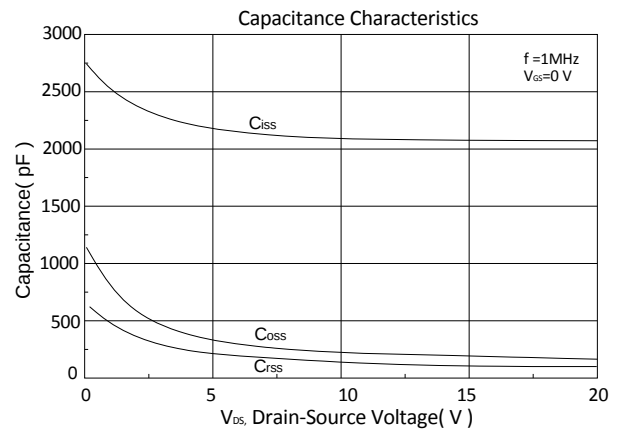
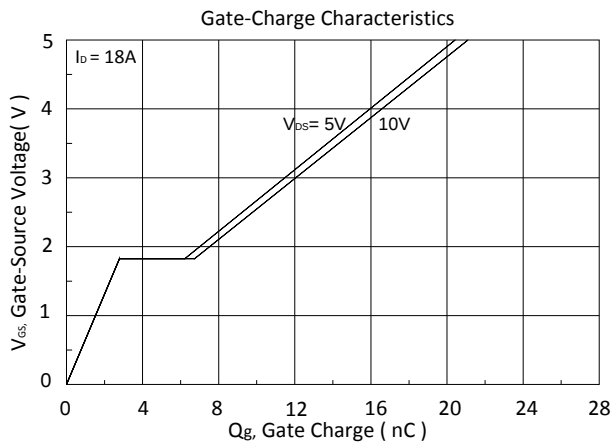
Device Name: EME07N02A for DPAK (TO-252)



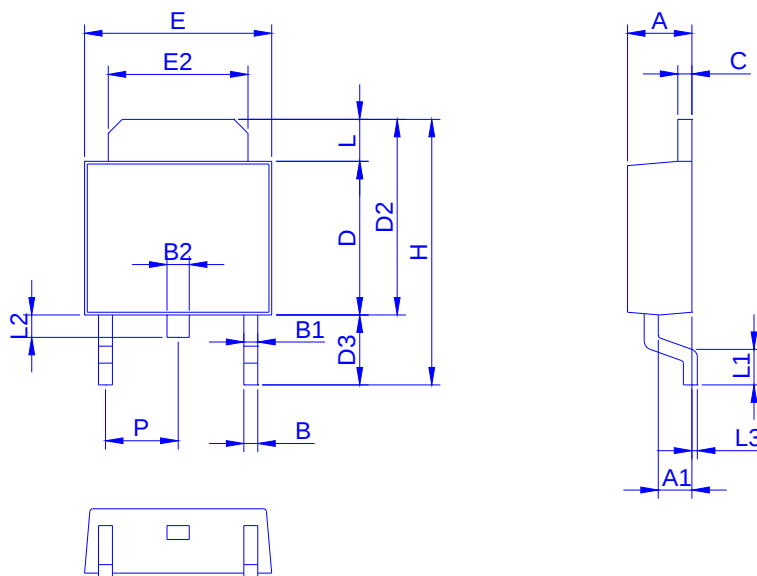


TYPICAL CHARACTERISTICS





Outline Drawing



Dimension	A	A1	B	B1	B2	C	D	D2	D3	E	E2	H	L	L1	L2	L3	P
Min.	2.10	0.95	0.30	0.40	0.60	0.40	5.30	6.70	2.20	6.40	4.80	9.20	0.89	0.90	0.50	0.00	2.10
Max.	2.50	1.30	0.85	0.94	1.00	0.60	6.20	7.30	3.00	6.70	5.45	10.15	1.70	1.65	1.10	0.30	2.50

Footprint

