杰力科技股份有限公司
Excelliance MOS Corporation

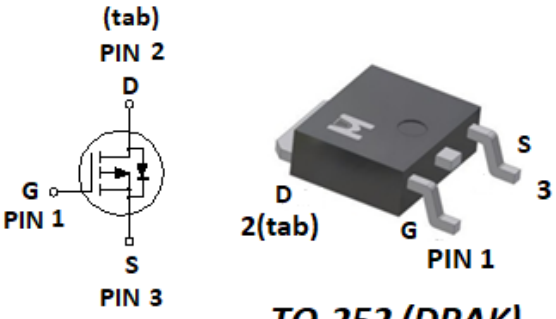
EMB20P06A

Single P-Channel Logic Level Enhancement Mode Field Effect Transistor

▪Product Summary:

	P-CH
BV_{DSS}	-60V
$R_{DSON\ (MAX.)}$@V_{GS}=-10V	18mΩ
$R_{DSON\ (MAX.)}$@V_{GS}=-4.5V	22mΩ
I_D @T_C=25°C	-50A

▪ Pin Description:



TO-252 (DPAK)

Single P Channel MOSFET
UIS, Rg 100% Tested
RoHS & Halogen Free & TSCA Compliant

▪ ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current[1]	T_C = 25 °C	I_D	-50	A
	T_C = 100 °C		-32	
	T_A = 25 °C		-8	
	T_A = 70 °C		-6	
Pulsed Drain Current[1]		I_{DM}	-92	
Avalanche Current[1]		I_{AS}	-58	
Avalanche Energy[1]	L = 0.1mH	E_{AS}	168	mJ
Repetitive Avalanche Energy[2]	L = 0.05mH	E_{AR}	84.1	
Power Dissipation[1]	T_C = 25 °C	P_D	92.6	W
	T_C = 100 °C		37	
Power Dissipation[1]	T_A = 25 °C		2.7	W
	T_A = 70 °C		1.7	
Operating Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150	℃

▪ 100% UIS testing in condition of VD=-30V, L=0.1mH, VG=10V, IL=35A, Rated VDS=-60V P-CH

▪THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE		SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case		$R_{\theta JC}$		1.35	°C / W
Junction-to-Ambient[3]	t≦10s	$R_{\theta JA}$		14	
	Steady-State	$R_{\theta JA}$		46	

[1]Pulse width limited by maximum junction temperature.

[2]Duty cycle < 1%

[3]The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25°C.

[4]Guarantee by Engineering test

▪ ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = -250μA	-60			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -250μA	-1.2	-1.6	-2.5	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0V, V_{GS} = ±20V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -60V, V_{GS} = 0V			-1	μA
		V_{DS} = -60V, V_{GS} = 0V, T_J = 125 °C			-25	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = -5V, V_{GS} = -10V	-50			A
Drain-Source On-State Resistance[1]	$R_{DS(ON)}$	V_{GS} = -10V, I_D = -20A		15	18	mΩ
		V_{GS} = -4.5V, I_D = -10A		18	22	
Forward Transconductance[1]	g_{fs}	V_{DS} = -5V, I_D = -20A		71		S
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0V, V_{DS} = -30V, f = 1MHz		5494		pF
Output Capacitance	C_{oss}			251		
Reverse Transfer Capacitance	C_{rss}			151		
Gate Resistance	R_g	f = 1MHz		1.9		Ω
Total Gate Charge[1,2]	Q_g(V_{GS}=10V)	V_{DS} = -30V, V_{GS} = -10V, I_D = -20A		115		nC
	Q_g(V_{GS}=4.5V)			52		
Gate-Source Charge[1,2]	Q_{gs}			18		
Gate-Drain Charge[1,2]	Q_{gd}			18		
Turn-On Delay Time[1,2]	$t_{d(on)}$	V_{DS} = -30V, V_{GS} = -10V, I_D = -5A , Rg = 3Ω		10		nS
Rise Time[1,2]	t_r			11		
Turn-Off Delay Time[1,2]	$t_{d(off)}$			121		
Fall Time[1,2]	t_f			41		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS						
Continuous Current	I_S				-50	A
Pulsed Current[3]	I_{SM}				-92	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0V			-1.2	V
Reverse Recovery Time	t_{rr}	I_F = I_S, dI_F/dt = 100A / μS		24.1		nS
Peak Reverse Recovery Current	$I_{RM(REC)}$			2.31		A
Reverse Recovery Charge	Q_{rr}			27.9		nC

[1]Pulse test : Pulse Width ≦ 300 usec, Duty Cycle ≦ 2%.

[2]Independent of operating temperature.

[3]Pulse width limited by maximum junction temperature.

[4]Guarantee by FT test Item

[5]Guarantee by Engineering test

▪TYPICAL CHARACTERISTICS

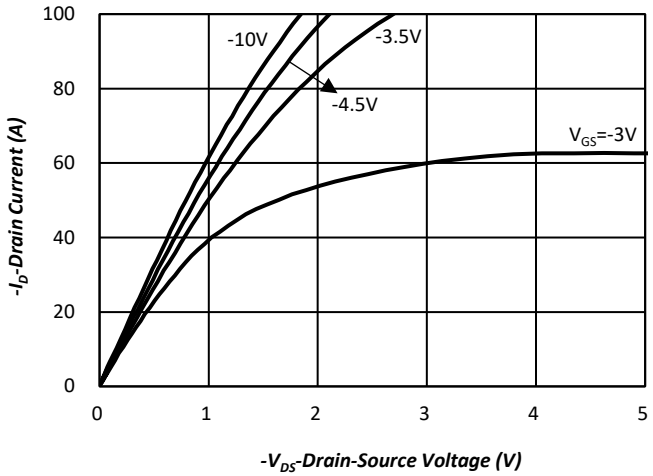


Fig.1 Typical Output Characteristics

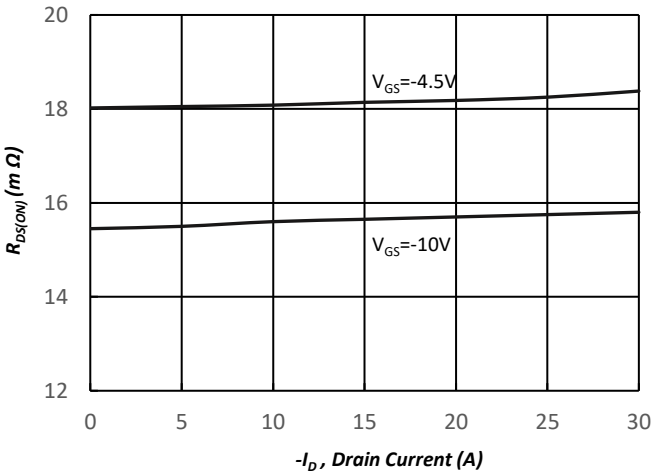


Fig.2 On-Resistance Variation with Drain Current and Gate Voltage

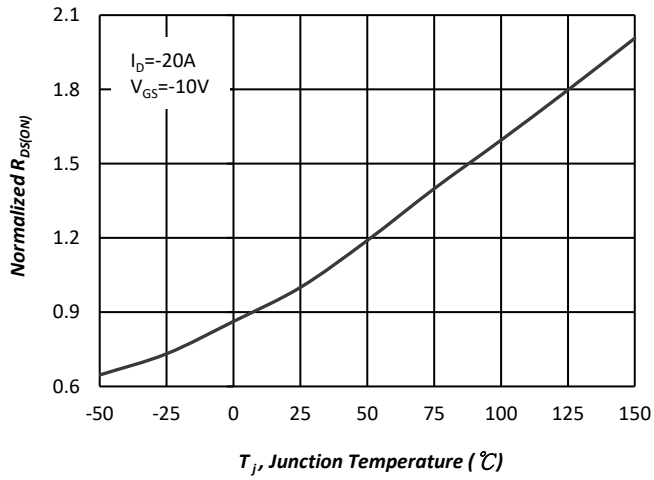


Fig.3 Normalized On-Resistance v.s. Junction Temperature

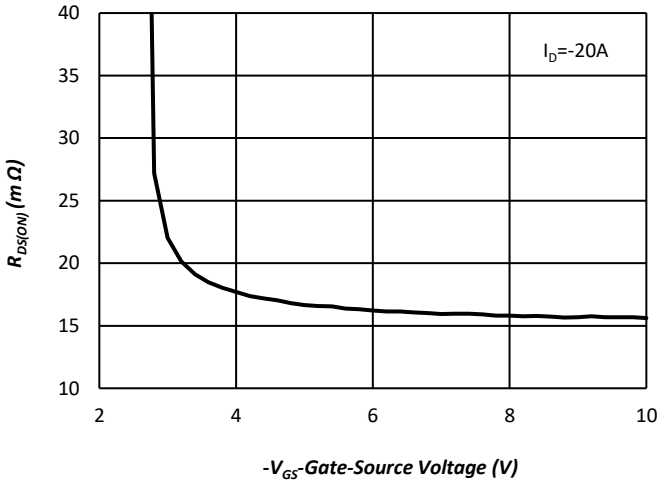


Fig.4 On-Resistance v.s. Gate Voltage

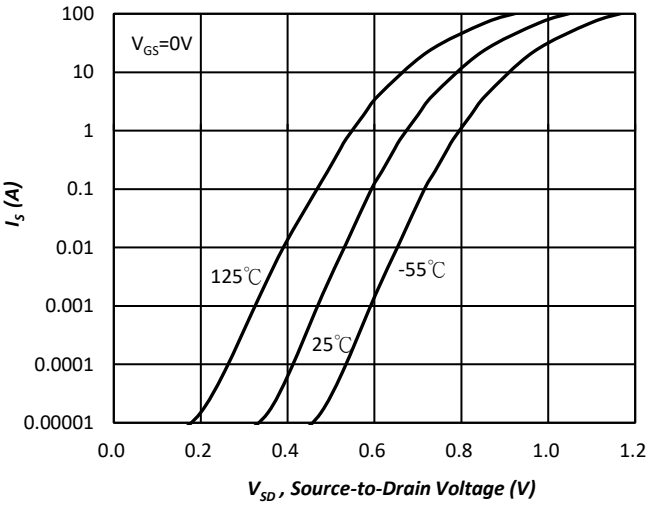


Fig.5 Forward Characteristic of Reverse Diode

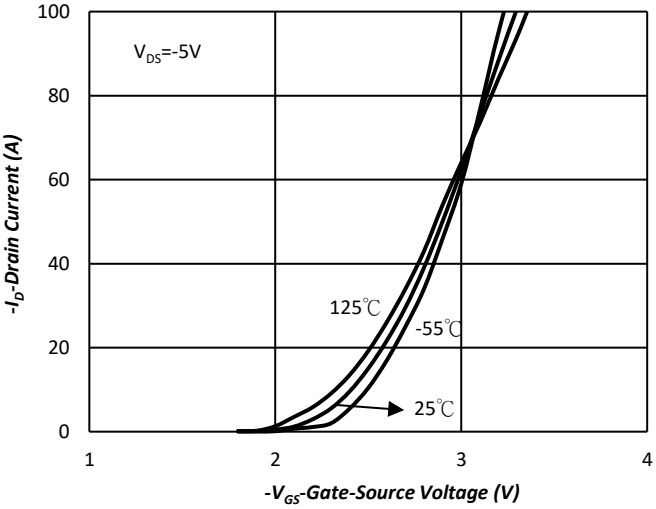


Fig.6 Transfer Characteristics

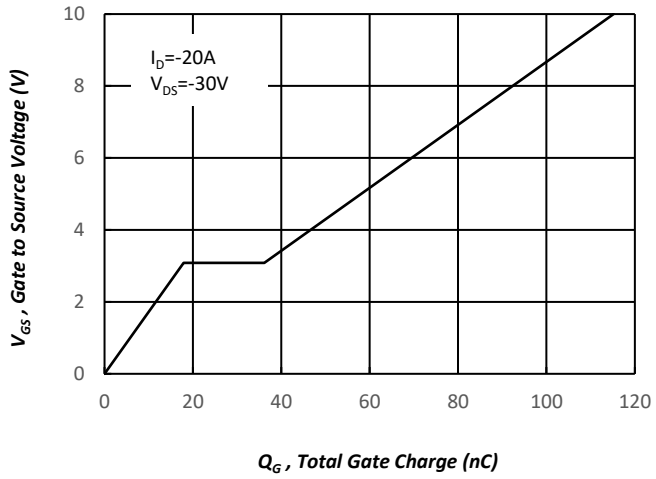


Fig.7 Gate Charge Characteristics

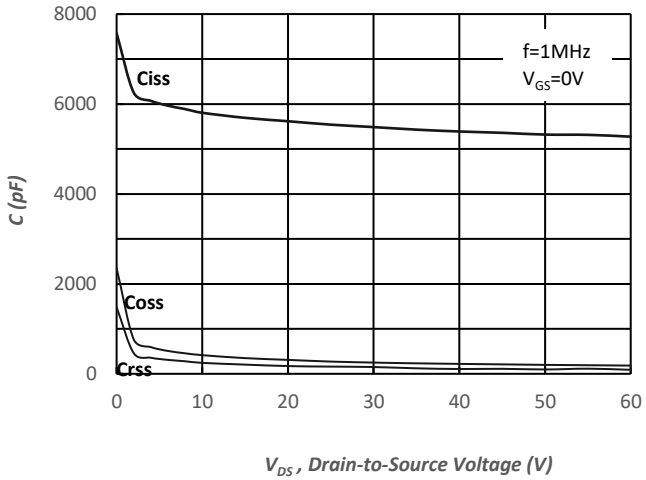


Fig.8 Typical Capacitance Characteristics

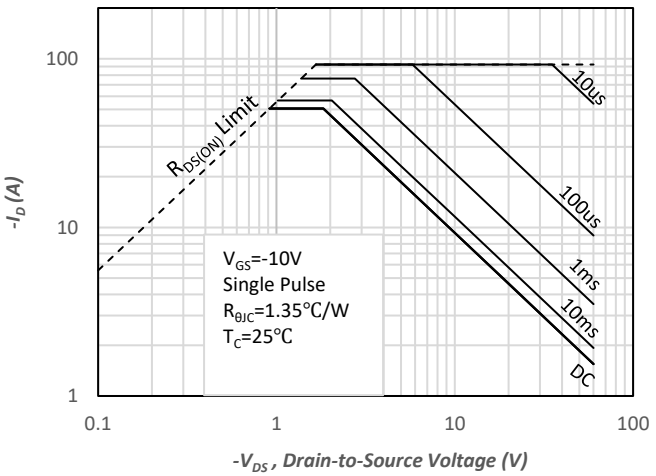


Fig 9. Maximum Safe Operating Area

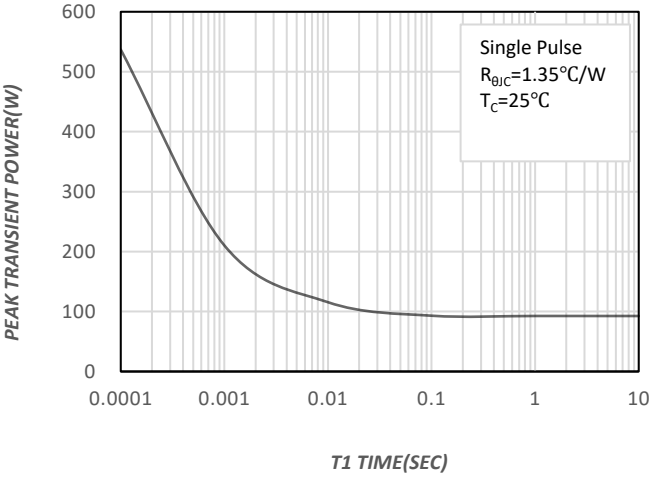


Fig 10. Single Pulse Maximum Power Dissipation

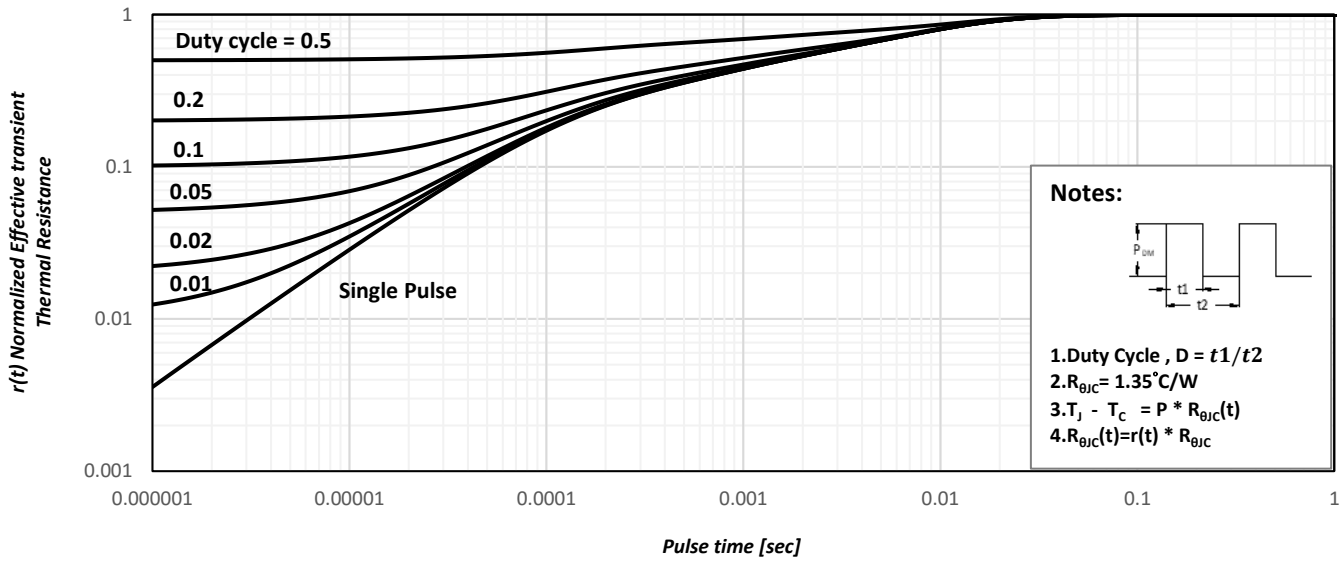
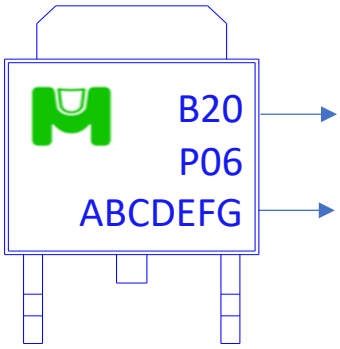


Fig 11. Effective Transient Thermal Impedance

Ordering & Marking Information:

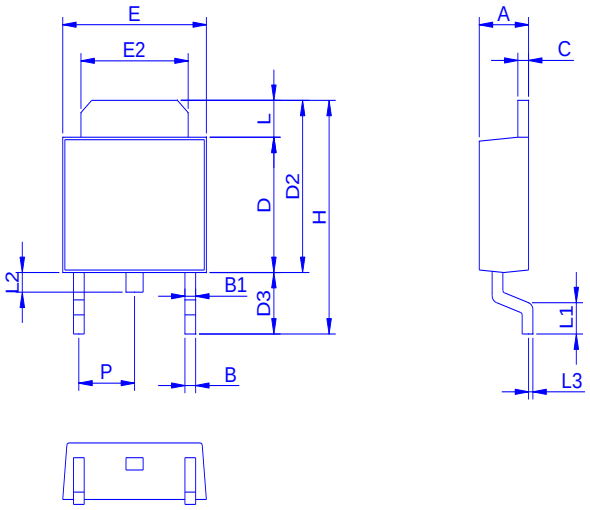
Device Name:EMB20P06A for TO-252 [DPAK]



B20P06: Device Name

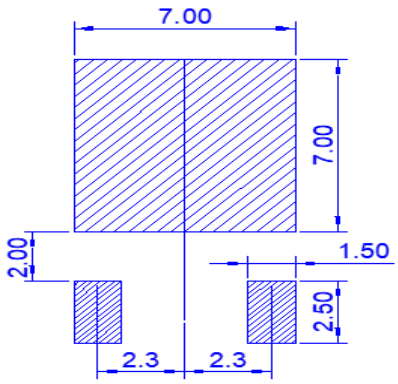
ABCDEFG: Date Code
A: Assembly House
B: Year(A:2008 B:2009 C:2010….)
C: Month(A:01 B:02 C:03 D:04 E:05 F:06 G:07 H:08 I:09 J:10 K:11 L:12)
DEFG: Serial No.

Outline Drawing

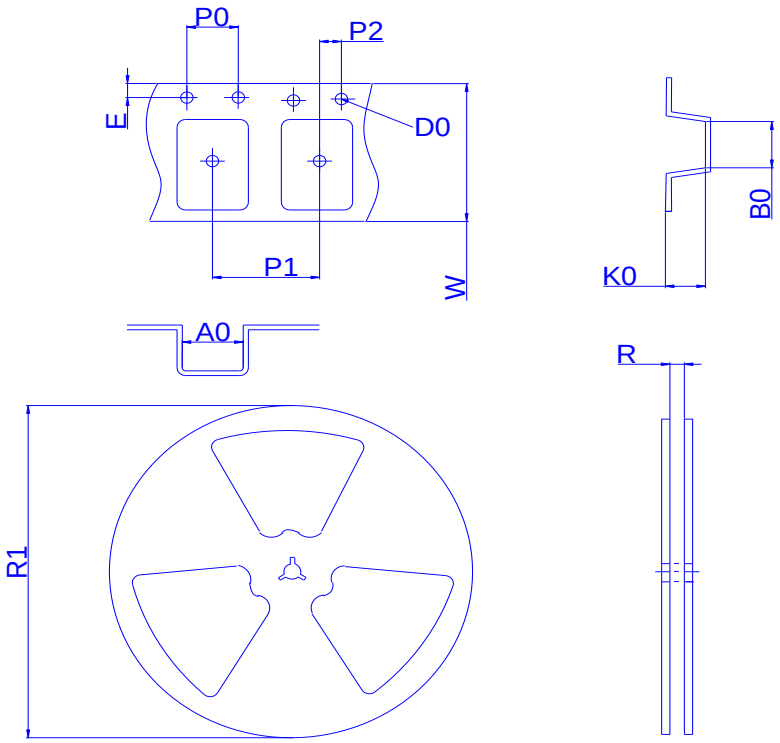


Dimension	A	B	B1	C	D	D2	D3	E	E2	H	L	L1	L2	L3	P
Min	2.1	0.62	0.65	0.45	5.96	6.8	2.6	6.3	4.9	9.3	0.8	1.2	0.5	0	2.1
Typ.	2.25	0.76	0.9	0.67	6.1	7.15	2.8	6.5	5.2	9.9	1.1	1.65	0.8	0.1	2.25
Max	2.4	0.9	1.15	0.89	6.24	7.5	3	6.7	5.5	10.5	1.4	2.1	1.1	0.2	2.4

Footprint



◆ **Tape&Reel Information:2500pcs/Reel**



Package	TO252-2
Reel	13"
Device orientation	FEED DIRECTION

Dimension in mm

Dimension	Carrier tape									Reel	
	A0	B0	D0	E	K0	P0	P1	P2	W	R	R1
Typ.	6.9	10.5	1.55	1.75	2.7	4	8	2	16	17	330
±	1	1	0.2	0.1	0.2	0.2	0.1	0.1	0.3	2	2