

PAGE MODE FLASH MEMORY

CMOS

128M (8M× 16) BIT

MBM29QM12DH-60

DESCRIPTION

The MBM29QM12DH is 128 M-bit, 3.0 V-only Page mode and dual operation Flash memory organized as 8M words of 16 bits each. The device is offered in 56-pin TSOP and 80-ball FBGA package. This device is designed to be programmed in-system with the standard system 3.0 V V_{cc} supply. 12.0 V V_{pp} and 5.0 V V_{cc} are not required for write or erase operations. The device can also be reprogrammed in standard EPROM programmers.

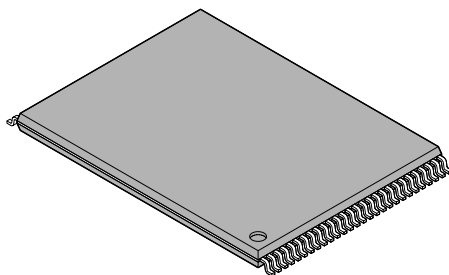
(Continued)

PRODUCT LINE UP

Part No.	MBM29QM12DH60	
V _{cc} = 3.0 V $\begin{smallmatrix} +0.6\text{ V} \\ -0.3\text{ V} \end{smallmatrix}$	V _{ccq} = 2.7 V to 3.6 V	V _{ccq} = 1.65 V to 1.95 V
Max Random Address Access Time (ns)	60	70
Max Page Address Access Time (ns)	20	30
Max $\overline{\text{CE}}$ Access Time (ns)	60	70
Max $\overline{\text{OE}}$ Access Time (ns)	20	30

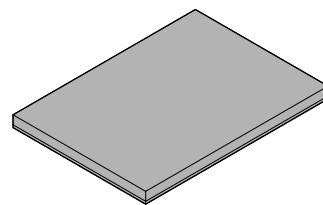
PACKAGES

56-pin plastic TSOP (1)



(FPT-56P-M01)

80-pin plastic FBGA



(BGA-80P-M04)

MBM29QM12DH-60

(Continued)

The device provides truly high performance non-volatile Flash memory solution. The device offers fast page access times of 20 ns with random access times of 60 ns, allowing operation of high-speed microprocessors without wait states. To eliminate bus contention the device has separate chip enable (\overline{CE}), write enable (\overline{WE}), and output enable (\overline{OE}) controls. The page size is 8 words.

The dual operation function provides simultaneous operation by dividing the memory space into four banks. The device can improve overall system performance by allowing a host system to program or erase in one bank, then immediately and simultaneously read from the other bank with zero latency. This releases the system from waiting for the completion of program or erase operations.

The device is command set compatible with JEDEC standard E²PROMs. Commands are written to the command register using standard microprocessor write timings. Register contents serve as input to an internal state-machine which controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from 5.0 V and 12.0 V Flash or EPROM devices.

The device is programmed by executing the program command sequence. This will invoke the Embedded Program Algorithm which is an internal algorithm that automatically times the program pulse widths and verifies proper cell margins. Typically, each 32K words sector can be programmed and verified in about 0.3 seconds. Erase is accomplished by executing the erase command sequence. This will invoke the Embedded Erase Algorithm which is an internal algorithm that automatically preprograms the array if it is not already programmed before executing the erase operation. During erase, the device automatically times the erase pulse widths and verifies proper cell margins.

Any individual sector is typically erased and verified in 0.5 second. (If already preprogrammed.)

The device also features a sector erase architecture. The sector mode allows each sector to be erased and reprogrammed without affecting other sectors. The device is erased when shipped from the factory.

The device features single 3.0 V power supply operation for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations. A low V_{CC} detector automatically inhibits write operations on the loss of power. The end of program or erase is detected by $\overline{\text{Data}}$ Polling of DQ₇, by the Toggle Bit feature on DQ₆, output pin. Once the end of a program or erase cycle has been completed, the device internally resets to the read mode.

Fujitsu's Flash technology combines years of Flash memory manufacturing experience to produce the highest levels of quality, reliability, and cost effectiveness. The device memory electrically erases all bits within a sector simultaneously via Fowler-Nordhiem tunneling. The words are programmed one word at a time using the EPROM programming mechanism of hot electron injection.

■ FEATURES

- **0.13 μm Process Technology**
- **Single 3.0 V read, program and erase**
Minimized system level power requirements
- **Simultaneous Read/Write operations (Dual Bank)**
- **FlexBank™ *1**
Bank A: 16 Mbit (4 KW \times 8 and 32 KW \times 31)
Bank B: 48 Mbit (32 KW \times 96)
Bank C: 48 Mbit (32 KW \times 96)
Bank D: 16 Mbit (4 KW \times 8 and 32 KW \times 31)
- **Enhanced $V_{I/O}$ (V_{CCQ}) Feature**
Input / Output voltage generated on the device is determined based on the $V_{I/O}$ level
 $V_{I/O}$ (V_{CCQ}) range : 2.7 V to 3.6 V or 1.65 V to 1.95 V
- **High Performance Page Mode**
20 ns maximum page access time (60 ns random access time) (3 V $V_{I/O}$)
- **8 words Page (\times 16)**
- **Compatible with JEDEC-standard commands**
Uses same software commands as E²PROMs
- **Minimum 100,000 program/erase cycles**
- **Sector erase architecture**
Eight 4K words, two hundred fifty-four 32K words, eight 8K words sectors.
Any combination of sectors can be concurrently erased. Also supports full chip erase
- **Dual Boot Block**
164K words boot block sectors, 8 at the top of the address range and 8 at the bottom of the address range
- **HiddenROM region**
64 words for factory and 64 words for customer of HiddenROM, accessible through a new “HiddenROM Enable” command sequence
Factory serialized and protected to provide a secure electronic serial number (ESN)
- **$\overline{\text{WP}}/\text{ACC}$ input pin**
At V_{IL} , allows protection of “outermost” 2 \times 4K words on both ends of boot sectors, regardless of sector protection/unprotection status
At V_{IH} , allows removal of boot sector protection
At V_{ACC} , increases program performance
- **Embedded Erase™ *2 Algorithms**
Automatically preprograms and erases the chip or any sector
- **Embedded Program™ *2 Algorithms**
Automatically writes and verifies data at specified address
- **$\overline{\text{Data}}$ Polling and Toggle Bit feature for detection of program or erase cycle completion**
- **Ready/Busy output ($\text{RY}/\overline{\text{BY}}$)**
Hardware method for detection of program or erase cycle completion
- **Automatic sleep mode**
When addresses remain stable, the device automatically switches itself to low power mode.
- **Low V_{CC} write inhibit \leq 2.5 V**

(Continued)

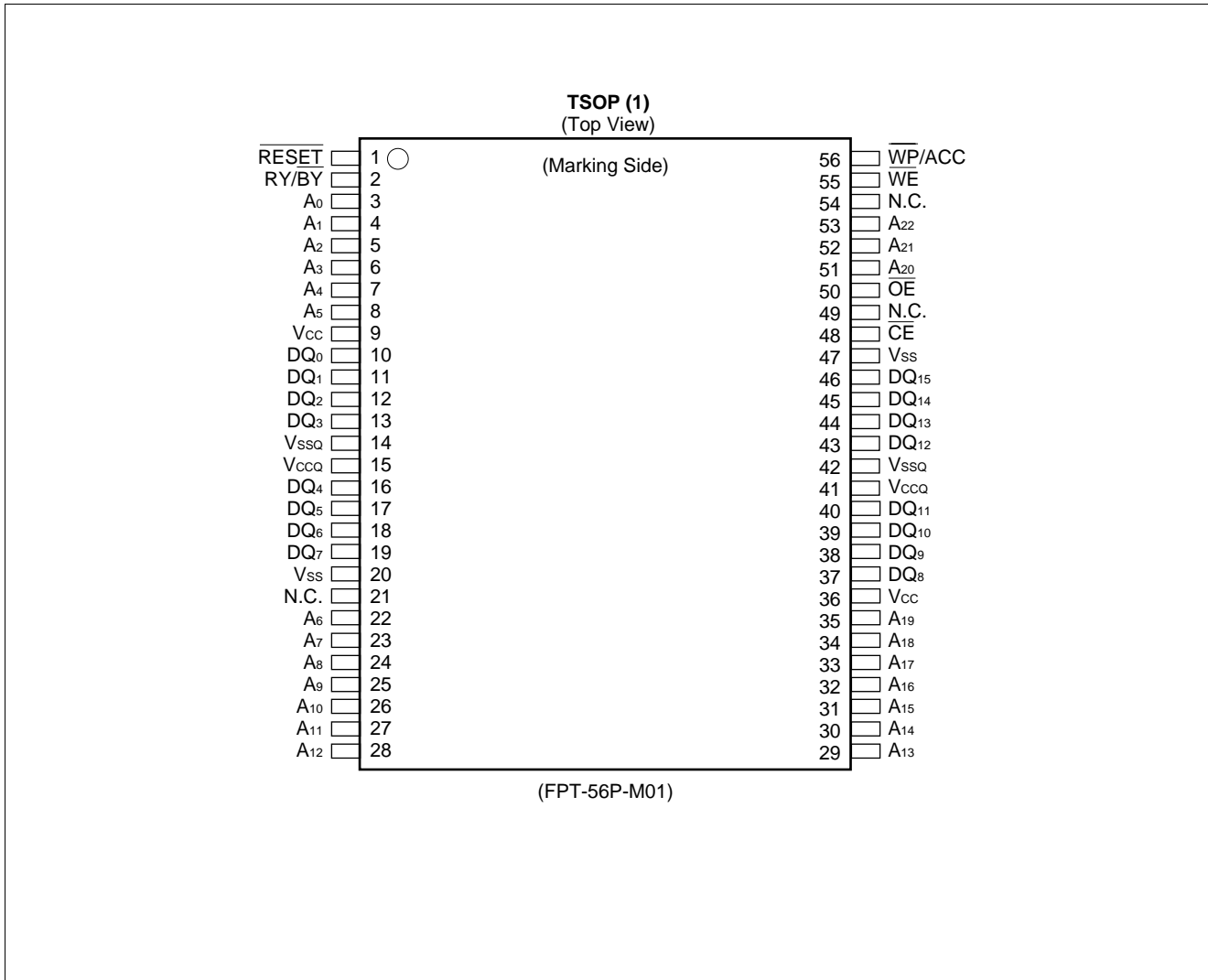
(Continued)

- **Program Suspend/Resume**
Suspends the program operation to allow a read in another byte
- **Erase Suspend/Resume**
Suspends the erase operation to allow a read data and/or program in another sector within the same device
- **In accordance with CFI (Common Flash Memory Interface)**
- **Hardware Reset Pin ($\overline{\text{RESET}}$)**
Hardware method to reset the device for reading array data
- **New Sector Protection**
Persistent Sector Protection
Password Sector Protection

*1 : FlexBank™ is a trademark of Fujitsu Limited, Japan.

*2 : Embedded Erase™ and Embedded Program™ are trademarks of Advanced Micro Devices, Inc.

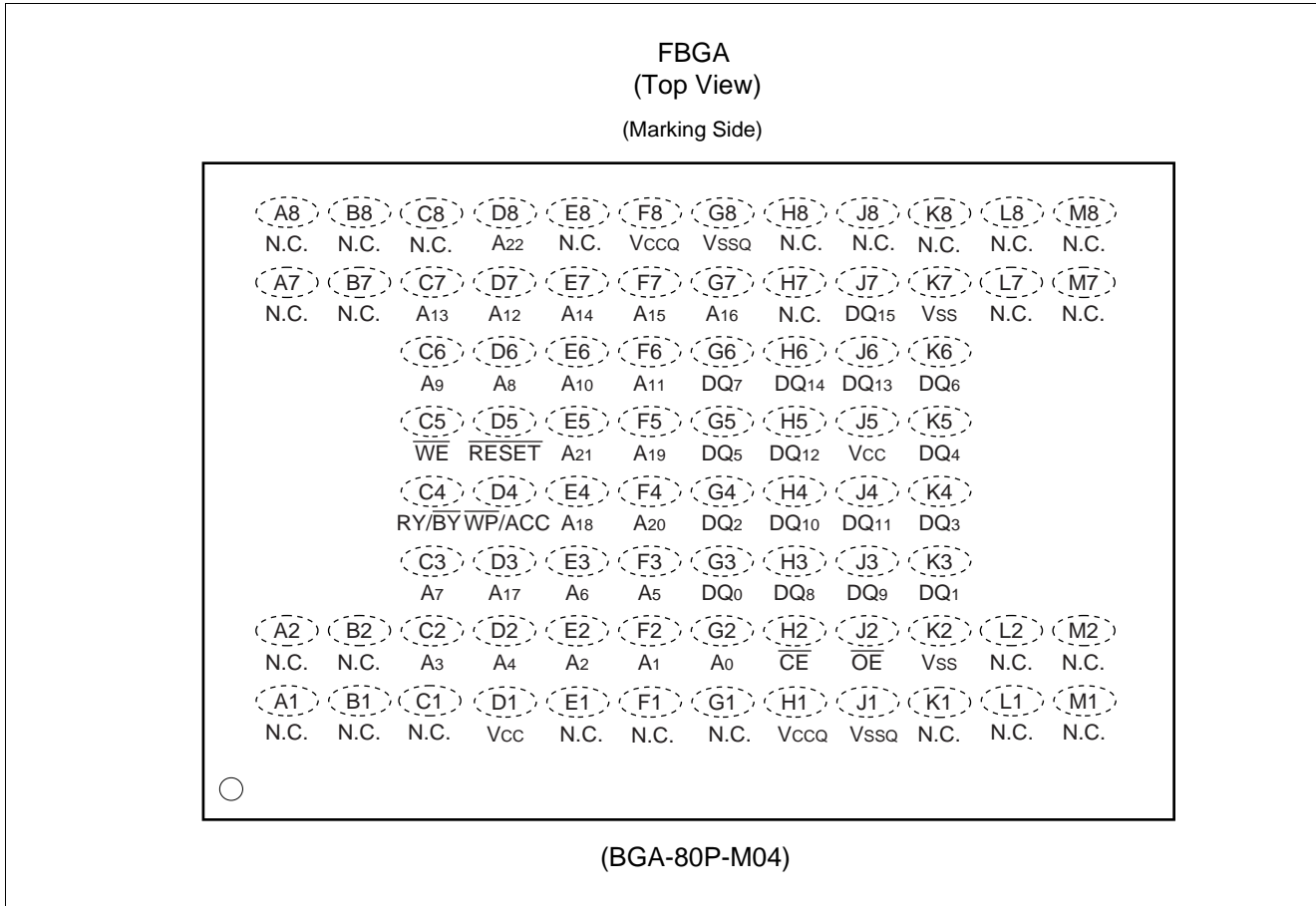
■ PIN ASSIGNMENT



(Continued)

MBM29QM12DH-60

(Continued)

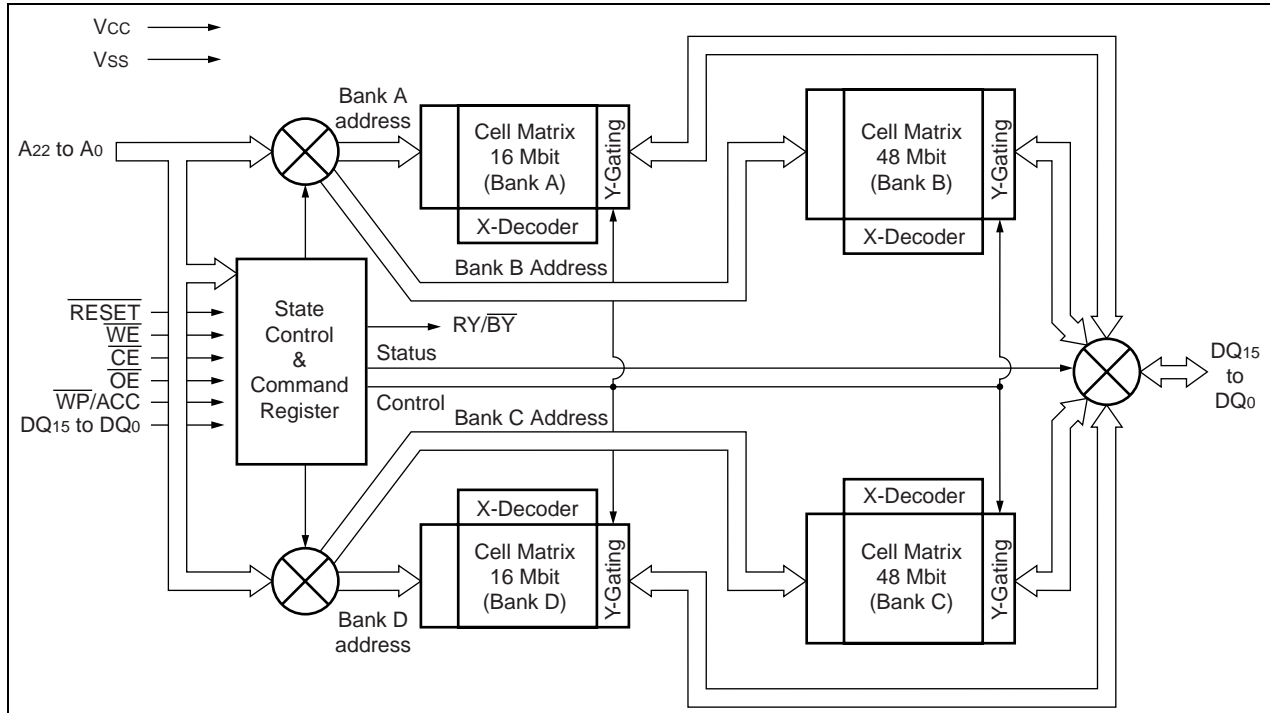


■ PIN DESCRIPTIONS

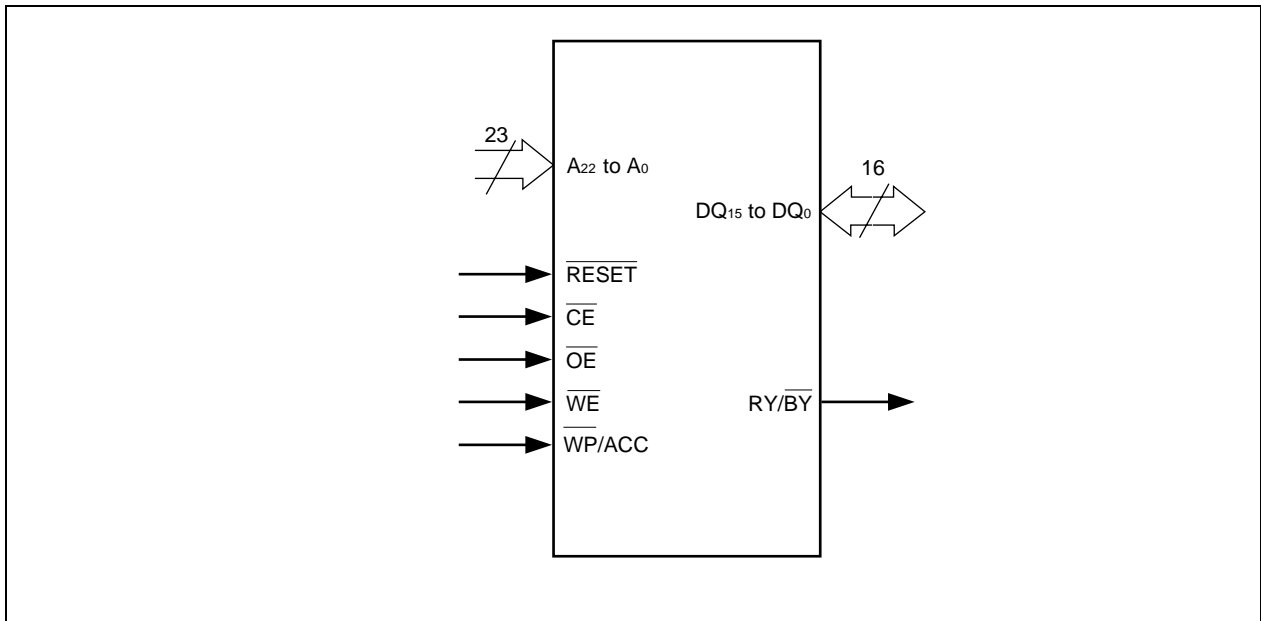
MBM29QM12DH Pin Configuration Table

Pin	Function
A22 to A0	Address Inputs
DQ15 to DQ0	Data Inputs/Outputs
\overline{CE}	Chip Enable
\overline{OE}	Output Enable
\overline{WE}	Write Enable
\overline{RESET}	Hardware Reset
$\overline{WP/ACC}$	Hardware Write Protection/ Program Acceleration
RY/ \overline{BY}	Ready/Busy output
N.C.	Pin Not Connected Internally
Vss	Device Ground
Vcc	Device Power Supply
Vssq	Input & Output Buffer Ground
Vccq	Input & Output Buffer Power Supply

■ BLOCK DIAGRAM




■ LOGIC SYMBOL




MBM29QM12DH-60

■ DEVICE BUS OPERATION

MBM29QM12DH User Bus Operations Table

Operation	\overline{CE}	\overline{OE}	\overline{WE}	A ₀	A ₁	A ₂	A ₃	A ₄	A ₅	A ₆	A ₇	A ₉	DQ ₁₅ to DQ ₀	\overline{RESET}	$\overline{WP/ACC}$
Auto-Select Manufacturer Code* ¹	L	L	H	L	L	L	L	X	X	L	L	V _{ID}	Code	H	X
Auto-Select Device Code* ¹	L	L	H	H	L	L	L	X	X	L	L	V _{ID}	Code	H	X
Extended Auto-Select Device Code* ²	L	L	H	L	H	H	H	X	X	L	L	V _{ID}	Code	H	X
	L	L	H	H	H	H	H	X	X	L	L	V _{ID}	Code	H	X
Read* ³	L	L	H	A ₀	A ₁	A ₂	A ₃	A ₄	A ₅	A ₆	A ₇	A ₉	D _{OUT}	H	X
Standby	H	X	X	X	X	X	X	X	X	X	X	X	High-Z	H	X
Output Disable	L	H	H	X	X	X	X	X	X	X	X	X	High-Z	H	X
Write (Program/Erase)	L	H	L	A ₀	A ₁	A ₂	A ₃	A ₄	A ₅	A ₆	A ₇	A ₉	D _{IN}	H	X
Enable Sector Group Protection* ^{3,*4}	L	V _{ID}		L	H	L	L	L	L	L	L	V _{ID}	X	H	X
Verify Sector Group Protection* ^{3,*4}	L	L	H	L	H	L	L	L	L	L	L	V _{ID}	Code	H	H
Boot Block Sector Write Protection* ⁶	X	X	X	X	X	X	X	X	X	X	X	X	X	H	L
Temporary Sector Group Unprotection* ⁵	X	X	X	X	X	X	X	X	X	X	X	X	X	V _{ID}	X
Reset	X	X	X	X	X	X	X	X	X	X	X	X	High-Z	L	X

Legend: L = V_{IL}, H = V_{IH}, X = V_{IL} or V_{IH},  = Pulse input. See DC Characteristics for voltage levels.

*1 : Manufacturer and device codes may also be accessed via a command register write sequence. See “MBM29QM12DH Command Definitions Table” in “■ DEVICE BUS OPERATION”.

*2 : \overline{WE} can be V_{IL} if \overline{OE} is V_{IL}, \overline{OE} at V_{IH} initiates the write operations.

*3 : Refer to section on Sector Protection.

*4 : V_{CCQ} = 2.7 V to 3.6 V for 60 ns
V_{CCQ} = 1.65 V to 1.95 V for 70 ns.

*5 : Also used for the extended sector group protection.

*6 : Protect “outermost” 2 × 4K words on both ends of the boot block sectors (SA0, SA1, SA268, SA269) .

MBM29QM12DH Command Definitions Table

Command Sequence	Bus Write Cycles Req'd	First Bus Write Cycle		Second Bus Write Cycle		Third Bus Write Cycle		Fourth Bus Read/Write Cycle		Fifth Bus Write Cycle		Sixth Bus Write Cycle		Seventh Bus Write Cycle	
		Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data
Read/Reset	1	XXXh	F0h	RA	RD	—	—	—	—	—	—	—	—	—	—
Read/Reset	3	555h	AAh	2AAh	55h	555h	F0h	RA	RD	—	—	—	—	—	—
Autoselect	3	555h	AAh	2AAh	55h	(BA) 555h	90h	—	—	—	—	—	—	—	—
Program	4	555h	AAh	2AAh	55h	555h	A0h	PA	PD	—	—	—	—	—	—
Chip Erase	6	555h	AAh	2AAh	55h	555h	80h	555h	AAh	2AAh	55h	555h	10h	—	—
Sector Erase	6	555h	AAh	2AAh	55h	555h	80h	555h	AAh	2AAh	55h	SA	30h	—	—
Program/Erase Suspend	1	BA	B0h	—	—	—	—	—	—	—	—	—	—	—	—
Program/Erase Resume	1	BA	30h	—	—	—	—	—	—	—	—	—	—	—	—
Set to Fast Mode	3	555h	AAh	2AAh	55h	555h	20h	—	—	—	—	—	—	—	—
Fast Program	2	XXXh	A0h	PA	PD	—	—	—	—	—	—	—	—	—	—
Reset from Fast Mode *1	2	BA	90h	XXXh	*4 F0h	—	—	—	—	—	—	—	—	—	—
Extended Sector Group Protection *2	4	XXXh	60h	SGA+ WPH	60h	SGA+ WPH	40h	SGA+ WPH	SD	—	—	—	—	—	—
Query	1	(BA) 55h	98h	—	—	—	—	—	—	—	—	—	—	—	—
HiddenROM Entry	3	555h	AAh	2AAh	55h	555h	88h	—	—	—	—	—	—	—	—
HiddenROM Program *3	4	555h	AAh	2AAh	55h	555h	A0h	(HRA) PA	PD	—	—	—	—	—	—
HiddenROM Exit *3	4	555h	AAh	2AAh	55h	(HRBA) 555h	90h	XXXh	00h	—	—	—	—	—	—
HiddenROM Protect *3	6	555h	AAh	2AAh	55h	555h	60h	OPBP	68h	OPBP	48h	XXXh	RD (0)	—	—
Password Program	4	555h	AAh	2AAh	55h	555h	38h	XX0h	PD0	—	—	—	—	—	—
		555h	AAh	2AAh	55h	555h	38h	XX1h	PD1						
		555h	AAh	2AAh	55h	555h	38h	XX2h	PD2						
		555h	AAh	2AAh	55h	555h	38h	XX3h	PD3						
Password Unlock	7	555h	AAh	2AAh	55h	555h	28h	XX0h	PD0	XX1h	PD1	XX2h	PD2	XX3h	PD3
Password Verify	4	555h	AAh	2AAh	55h	555h	C8h	PWA	PWD	—	—	—	—	—	—

(Continued)

MBM29QM12DH-60

(Continued)

Command Sequence	Bus Write Cycles Req'd	First Bus Write Cycle		Second Bus Write Cycle		Third Bus Write Cycle		Fourth Bus Read/Write Cycle		Fifth Bus Write Cycle		Sixth Bus Write Cycle		Seventh Bus Write Cycle	
		Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data
Password Mode Locking Bit Program	6	555h	AAh	2AAh	55h	555h	60h	PL	68h	PL	48h	XXXh	RD (0)	—	—
Persistent Protection Mode Locking Bit Program	6	555h	AAh	2AAh	55h	555h	60h	SPML	68h	SPML	48h	XXXh	RD (0)	—	—
PPB Program	6	555h	AAh	2AAh	55h	555h	60h	SGA+ WP	68h	SGA+ WP	48h	XXXh	RD (0)	—	—
PPB Verify	4	555h	AAh	2AAh	55h	(BA) 555h	90h	SGA+ WP	RD (0)	—	—	—	—	—	—
All PPB Erase	4	555h	AAh	2AAh	55h	555h	60h	WP	60h	SGA+ WP	40h	XXXh	RD (0)	—	—
PPB Lock Bit Set	3	555h	AAh	2AAh	55h	555h	78h	—	—	—	—	—	—	—	—
PPB Lock Bit Verify	4	555h	AAh	2AAh	55h	(BA) 555h	58h	SA	RD (1)	—	—	—	—	—	—
DPB Write	4	555h	AAh	2AAh	55h	555h	48h	SA	X1h	—	—	—	—	—	—
DPB Erase	4	555h	AAh	2AAh	55h	555h	48h	SA	X0h	—	—	—	—	—	—
DPB Verify	4	555h	AAh	2AAh	55h	(BA) 555h	58h	SA	RD (0)	—	—	—	—	—	—

Legend:

- RA = Address of the memory location to be read
- PA = Address of the memory location to be programmed
Addresses are latched on the falling edge of the write pulse.
- SA = Address of the sector to be erased. The combination of A₂₂, A₂₁, A₂₀, A₁₉, A₁₈, A₁₇, A₁₆, A₁₅, A₁₄, A₁₃ and A₁₂ will uniquely select any sector.
- BA = Bank Address. Address set by A₂₂, A₂₁, A₂₀ will select Bank A, Bank B, Bank C and Bank D.
- RD = Data read from location RA during read operation.
- PD = Data to be programmed at location PA. Data is latched on the rising edge of write pulse.
- SGA = Sector group address to be protected.
- WPH = (A₇, A₆, A₅, A₄, A₃, A₂, A₁, A₀) is (0, 0, 0, 0, 0, 0, 1, 0)
- SD = Sector group protection verify data. Output 01h at protected sector group addresses and output 00h at unprotected sector group addresses.
- HRA = Address of the HiddenROM area Word Mode : 000000h to 00007Fh
- HRBA = Bank Address of the HiddenROM area (A₂₂ = A₂₁ = A₂₀ = V_{IL})
- RD (0) = Read Data bit. If programmed, DQ₀ = 1, if erase, DQ₀ = 0
- RD (1) = Read Data bit. If programmed, DQ₁ = 1, if erase, DQ₁ = 0
- OPBP = (A₇, A₆, A₅, A₄, A₃, A₂, A₁, A₀) is (0, 0, 0, 1, 1, 0, 1, 0)
- PWA/PWD = Password Address/Password Data
- PL = (A₇, A₆, A₅, A₄, A₃, A₂, A₁, A₀) is (0, 0, 0, 0, 1, 0, 1, 0)
- SPML = (A₇, A₆, A₅, A₄, A₃, A₂, A₁, A₀) is (0, 0, 0, 1, 0, 0, 1, 0)
- WP = (A₇, A₆, A₅, A₄, A₃, A₂, A₁, A₀) is (0, 0, 0, 0, 0, 0, 1, 0)

*1 : This command is valid during Fast Mode.

*2 : This command is valid while $\overline{\text{RESET}} = V_{\text{ID}}$.

*3 : This command is valid during HiddenROM mode.

*4 : The data "00h" is also acceptable.

*5 : Command combinations not described in "MBM29QM12DH Command Definitions Table" in "■ DEVICE BUS OPERATION" are illegal.

Notes : • Address bits A_{22} to $A_{11} = X = \text{"H"}$ or "L" for all address commands except for PA, SA, BA, SGA, OPBP, PWA, PL, SPML, WP, WPH.

• Bus operations are defined in "MBM29QM12DH User Bus Operations Table" and "MBM29QM12DH Command Definitions Table" in "■ DEVICE BUS OPERATION".

• The system should generate the following address patterns:

Word Mode : 555h or 2AAh to addresses A_{10} to A_0

• Both Read/Reset commands are functionally equivalent, resetting the device to the read mode.

MBM29QM12DH Sector Group Protection Verify Autoselect Codes Table

Type	A_{22} to A_{12}	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	Code (HEX)
Manufacture's Code	BA^{*2}	V_{IL}	V_{IL}	X	X	V_{IL}	V_{IL}	V_{IL}	V_{IL}	04h
Device Code	BA^{*2}	V_{IL}	V_{IL}	X	X	V_{IL}	V_{IL}	V_{IL}	V_{IH}	227Eh
Extended Device Code*3	BA^{*2}	V_{IL}	V_{IL}	X	X	V_{IH}	V_{IH}	V_{IH}	V_{IL}	2220h
		V_{IL}	V_{IL}	X	X	V_{IH}	V_{IH}	V_{IH}	V_{IH}	2200h
Sector Group Protection	Sector Group Addresses	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	01h*1
Extended Device Code (Indicator Bits)	BA^{*2}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{IH}	DQ ₇ - Factory Lock Bit 1 = Locked, 0 = Not Locked DQ ₆ - Customer Lock Bit 1 = Locked, 0 = Not Locked

*1 : Sector Group can be protected by "Sector Group Protection", "Extended Sector Group Protection", and "New Sector Protection(PPB Protection). Outputs 01h at protected sector group addresses and outputs 00h at unprotected sector group addresses.

*2 : When V_{ID} is applied to A_9 , both Bank 1 and Bank 2 are put into Autoselect mode, which makes simultaneous operation unable to be executed. Consequently, specifying the bank address is not required. However, the bank address needs to be indicated when Autoselect mode is read out at command mode, because then it becomes possible to activate simultaneous operation.

*3 : A read cycle at address (BA) 01h outputs device code. When 227Eh is output, it indicates that two additional codes, called Extended Device Codes, will be required. Therefore the system may continue reading out these Extended Device Codes at the address of (BA) 0Eh, as well as at (BA) 0Fh.

Extended Autoselect Code Table

Type	Code	DQ ₁₅	DQ ₁₄	DQ ₁₃	DQ ₁₂	DQ ₁₁	DQ ₁₀	DQ ₉	DQ ₈	DQ ₇	DQ ₆	DQ ₅	DQ ₄	DQ ₃	DQ ₂	DQ ₁	DQ ₀
Manufacturer's Code	04h	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
Device Code	227Eh	0	0	1	0	0	0	1	0	0	1	1	1	1	1	1	0
Extended Device Code	2220h	0	0	1	0	0	0	1	0	0	0	1	0	0	0	0	0
	2200h	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0
PPB Protection	01h	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
PPB Unprotection	00h	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

MBM29QM12DH-60

■ FLEXIBLE SECTOR-ERASE ARCHITECTURE

Sector Address Table (Bank A)

Bank	Sector	Sector Address										Sector Size (Kwords)	(× 16) Address Range	
		Bank Address			A ₁₉	A ₁₈	A ₁₇	A ₁₆	A ₁₅	A ₁₄	A ₁₃			A ₁₂
		A ₂₂	A ₂₁	A ₂₀										
Bank A	SA0	0	0	0	0	0	0	0	0	0	0	0	4	000000h to 000FFFh
	SA1	0	0	0	0	0	0	0	0	0	0	1	4	001000h to 001FFFh
	SA2	0	0	0	0	0	0	0	0	0	1	0	4	002000h to 002FFFh
	SA3	0	0	0	0	0	0	0	0	0	1	1	4	003000h to 003FFFh
	SA4	0	0	0	0	0	0	0	0	1	0	0	4	004000h to 004FFFh
	SA5	0	0	0	0	0	0	0	0	1	0	1	4	005000h to 005FFFh
	SA6	0	0	0	0	0	0	0	0	1	1	0	4	006000h to 006FFFh
	SA7	0	0	0	0	0	0	0	0	1	1	1	4	007000h to 007FFFh
	SA8	0	0	0	0	0	0	0	1	X	X	X	32	008000h to 00FFFFh
	SA9	0	0	0	0	0	0	1	0	X	X	X	32	010000h to 017FFFh
	SA10	0	0	0	0	0	0	1	1	X	X	X	32	018000h to 01FFFFh
	SA11	0	0	0	0	0	1	0	0	X	X	X	32	020000h to 027FFFh
	SA12	0	0	0	0	0	1	0	1	X	X	X	32	028000h to 02FFFFh
	SA13	0	0	0	0	0	1	1	0	X	X	X	32	030000h to 037FFFh
	SA14	0	0	0	0	0	1	1	1	X	X	X	32	038000h to 03FFFFh
	SA15	0	0	0	0	1	0	0	0	X	X	X	32	040000h to 047FFFh
	SA16	0	0	0	0	1	0	0	1	X	X	X	32	048000h to 04FFFFh
	SA17	0	0	0	0	1	0	1	0	X	X	X	32	050000h to 057FFFh
	SA18	0	0	0	0	1	0	1	1	X	X	X	32	058000h to 05FFFFh
	SA19	0	0	0	0	1	1	0	0	X	X	X	32	060000h to 067FFFh
	SA20	0	0	0	0	1	1	0	1	X	X	X	32	068000h to 06FFFFh
	SA21	0	0	0	0	1	1	1	0	X	X	X	32	070000h to 077FFFh
	SA22	0	0	0	0	1	1	1	1	X	X	X	32	078000h to 07FFFFh
	SA23	0	0	0	1	0	0	0	0	X	X	X	32	080000h to 087FFFh
	SA24	0	0	0	1	0	0	0	1	X	X	X	32	088000h to 08FFFFh
	SA25	0	0	0	1	0	0	1	0	X	X	X	32	090000h to 097FFFh
	SA26	0	0	0	1	0	0	1	1	X	X	X	32	098000h to 09FFFFh
	SA27	0	0	0	1	0	1	0	0	X	X	X	32	0A0000h to 0A7FFFh
	SA28	0	0	0	1	0	1	0	1	X	X	X	32	0A8000h to 0AFFFFh
	SA29	0	0	0	1	0	1	1	0	X	X	X	32	0B0000h to 0B7FFFh
	SA30	0	0	0	1	0	1	1	1	X	X	X	32	0B8000h to 0BFFFFh
	SA31	0	0	0	1	1	0	0	0	X	X	X	32	0C0000h to 0C7FFFh
	SA32	0	0	0	1	1	0	0	1	X	X	X	32	0C8000h to 0CFFFFh
	SA33	0	0	0	1	1	0	1	0	X	X	X	32	0D0000h to 0D7FFFh
	SA34	0	0	0	1	1	0	1	1	X	X	X	32	0D8000h to 0DFFFFh
	SA35	0	0	0	1	1	1	0	0	X	X	X	32	0E0000h to 0E7FFFh
	SA36	0	0	0	1	1	1	0	1	X	X	X	32	0E8000h to 0EFFFFh
	SA37	0	0	0	1	1	1	1	0	X	X	X	32	0F0000h to 0F7FFFh
SA38	0	0	0	1	1	1	1	1	X	X	X	32	0F8000h to 0FFFFFh	

Sector Address Table (Bank B)

Bank	Sector	Sector Address										Sector Size (Kwords)	(× 16) Address Range	
		Bank Address			A ₁₉	A ₁₈	A ₁₇	A ₁₆	A ₁₅	A ₁₄	A ₁₃			A ₁₂
		A ₂₂	A ₂₁	A ₂₀										
Bank B	SA39	0	0	1	0	0	0	0	0	X	X	X	32	100000h to 107FFFh
	SA40	0	0	1	0	0	0	0	1	X	X	X	32	108000h to 10FFFFh
	SA41	0	0	1	0	0	0	1	0	X	X	X	32	110000h to 117FFFh
	SA42	0	0	1	0	0	0	1	1	X	X	X	32	118000h to 11FFFFh
	SA43	0	0	1	0	0	1	0	0	X	X	X	32	120000h to 127FFFh
	SA44	0	0	1	0	0	1	0	1	X	X	X	32	128000h to 12FFFFh
	SA45	0	0	1	0	0	1	1	0	X	X	X	32	130000h to 137FFFh
	SA46	0	0	1	0	0	1	1	1	X	X	X	32	138000h to 13FFFFh
	SA47	0	0	1	0	1	0	0	0	X	X	X	32	140000h to 147FFFh
	SA48	0	0	1	0	1	0	0	1	X	X	X	32	148000h to 14FFFFh
	SA49	0	0	1	0	1	0	1	0	X	X	X	32	150000h to 157FFFh
	SA50	0	0	1	0	1	0	1	1	X	X	X	32	158000h to 15FFFFh
	SA51	0	0	1	0	1	1	0	0	X	X	X	32	160000h to 167FFFh
	SA52	0	0	1	0	1	1	0	1	X	X	X	32	168000h to 16FFFFh
	SA53	0	0	1	0	1	1	1	0	X	X	X	32	170000h to 177FFFh
	SA54	0	0	1	0	1	1	1	1	X	X	X	32	178000h to 17FFFFh
	SA55	0	0	1	1	0	0	0	0	X	X	X	32	180000h to 187FFFh
	SA56	0	0	1	1	0	0	0	1	X	X	X	32	188000h to 18FFFFh
	SA57	0	0	1	1	0	0	1	0	X	X	X	32	190000h to 197FFFh
	SA58	0	0	1	1	0	0	1	1	X	X	X	32	198000h to 19FFFFh
	SA59	0	0	1	1	0	1	0	0	X	X	X	32	1A0000h to 1A7FFFh
	SA60	0	0	1	1	0	1	0	1	X	X	X	32	1A8000h to 1AFFFFh
	SA61	0	0	1	1	0	1	1	0	X	X	X	32	1B0000h to 1B7FFFh
	SA62	0	0	1	1	0	1	1	1	X	X	X	32	1B8000h to 1BFFFFh
	SA63	0	0	1	1	1	0	0	0	X	X	X	32	1C0000h to 1C7FFFh
	SA64	0	0	1	1	1	0	0	1	X	X	X	32	1C8000h to 1CFFFFh
	SA65	0	0	1	1	1	0	1	0	X	X	X	32	1D0000h to 1D7FFFh
	SA66	0	0	1	1	1	0	1	1	X	X	X	32	1D8000h to 1DFFFFh
	SA67	0	0	1	1	1	1	0	0	X	X	X	32	1E0000h to 1E7FFFh
	SA68	0	0	1	1	1	1	0	1	X	X	X	32	1E8000h to 1EFFFFh
SA69	0	0	1	1	1	1	1	0	X	X	X	32	1F0000h to 1F7FFFh	
SA70	0	0	1	1	1	1	1	1	X	X	X	32	1F8000h to 1FFFFFh	
SA71	0	1	0	0	0	0	0	0	X	X	X	32	200000h to 207FFFh	
SA72	0	1	0	0	0	0	0	1	X	X	X	32	208000h to 20FFFFh	
SA73	0	1	0	0	0	0	1	0	X	X	X	32	210000h to 217FFFh	
SA74	0	1	0	0	0	0	1	1	X	X	X	32	218000h to 21FFFFh	
SA75	0	1	0	0	0	1	0	0	X	X	X	32	220000h to 227FFFh	
SA76	0	1	0	0	0	1	0	1	X	X	X	32	228000h to 22FFFFh	
SA77	0	1	0	0	0	1	1	0	X	X	X	32	230000h to 237FFFh	

(Continued)

MBM29QM12DH-60

Bank	Sector	Sector Address											Sector Size (Kwords)	(× 16) Address Range
		Bank Address			A ₁₉	A ₁₈	A ₁₇	A ₁₆	A ₁₅	A ₁₄	A ₁₃	A ₁₂		
		A ₂₂	A ₂₁	A ₂₀										
Bank B	SA78	0	1	0	0	0	1	1	1	X	X	X	32	238000h to 23FFFFh
	SA79	0	1	0	0	1	0	0	0	X	X	X	32	240000h to 247FFFh
	SA80	0	1	0	0	1	0	0	1	X	X	X	32	248000h to 24FFFFh
	SA81	0	1	0	0	1	0	1	0	X	X	X	32	250000h to 257FFFh
	SA82	0	1	0	0	1	0	1	1	X	X	X	32	258000h to 25FFFFh
	SA83	0	1	0	0	1	1	0	0	X	X	X	32	260000h to 267FFFh
	SA84	0	1	0	0	1	1	0	1	X	X	X	32	268000h to 26FFFFh
	SA85	0	1	0	0	1	1	1	0	X	X	X	32	270000h to 277FFFh
	SA86	0	1	0	0	1	1	1	1	X	X	X	32	278000h to 27FFFFh
	SA87	0	1	0	1	0	0	0	0	X	X	X	32	280000h to 287FFFh
	SA88	0	1	0	1	0	0	0	1	X	X	X	32	288000h to 28FFFFh
	SA89	0	1	0	1	0	0	1	0	X	X	X	32	290000h to 297FFFh
	SA90	0	1	0	1	0	0	1	1	X	X	X	32	298000h to 29FFFFh
	SA91	0	1	0	1	0	1	0	0	X	X	X	32	2A0000h to 2A7FFFh
	SA92	0	1	0	1	0	1	0	1	X	X	X	32	2A8000h to 2AFFFFh
	SA93	0	1	0	1	0	1	1	0	X	X	X	32	2B0000h to 2B7FFFh
	SA94	0	1	0	1	0	1	1	1	X	X	X	32	2B8000h to 2BFFFFh
	SA95	0	1	0	1	1	0	0	0	X	X	X	32	2C0000h to 2C7FFFh
	SA96	0	1	0	1	1	0	0	1	X	X	X	32	2C8000h to 2CFFFFh
	SA97	0	1	0	1	1	0	1	0	X	X	X	32	2D0000h to 2D7FFFh
	SA98	0	1	0	1	1	0	1	1	X	X	X	32	2D8000h to 2DFFFFh
	SA99	0	1	0	1	1	1	0	0	X	X	X	32	2E0000h to 2E7FFFh
	SA100	0	1	0	1	1	1	0	1	X	X	X	32	2E8000h to 2EFFFFh
	SA101	0	1	0	1	1	1	1	0	X	X	X	32	2F0000h to 2F7FFFh
	SA102	0	1	0	1	1	1	1	1	X	X	X	32	2F8000h to 2FFFFFh
	SA103	0	1	1	0	0	0	0	0	X	X	X	32	300000h to 307FFFh
	SA104	0	1	1	0	0	0	0	1	X	X	X	32	308000h to 30FFFFh
	SA105	0	1	1	0	0	0	1	0	X	X	X	32	310000h to 317FFFh
	SA106	0	1	1	0	0	0	1	1	X	X	X	32	318000h to 31FFFFh
	SA107	0	1	1	0	0	1	0	0	X	X	X	32	320000h to 327FFFh
	SA108	0	1	1	0	0	1	0	1	X	X	X	32	328000h to 32FFFFh
	SA109	0	1	1	0	0	1	1	0	X	X	X	32	330000h to 337FFFh
SA110	0	1	1	0	0	1	1	1	X	X	X	32	338000h to 33FFFFh	
SA111	0	1	1	0	1	0	0	0	X	X	X	32	340000h to 347FFFh	
SA112	0	1	1	0	1	0	0	1	X	X	X	32	348000h to 34FFFFh	
SA113	0	1	1	0	1	0	1	0	X	X	X	32	350000h to 357FFFh	
SA114	0	1	1	0	1	0	1	1	X	X	X	32	358000h to 35FFFFh	
SA115	0	1	1	0	1	1	0	0	X	X	X	32	360000h to 367FFFh	
SA116	0	1	1	0	1	1	0	1	X	X	X	32	368000h to 36FFFFh	

(Continued)

(Continued)

Bank	Sector	Sector Address											Sector Size (Kwords)	(× 16) Address Range
		Bank Address			A ₁₉	A ₁₈	A ₁₇	A ₁₆	A ₁₅	A ₁₄	A ₁₃	A ₁₂		
		A ₂₂	A ₂₁	A ₂₀										
Bank B	SA117	0	1	1	0	1	1	1	0	X	X	X	32	370000h to 377FFFh
	SA118	0	1	1	0	1	1	1	1	X	X	X	32	378000h to 37FFFFh
	SA119	0	1	1	1	0	0	0	0	X	X	X	32	380000h to 387FFFh
	SA120	0	1	1	1	0	0	0	1	X	X	X	32	388000h to 38FFFFh
	SA121	0	1	1	1	0	0	1	0	X	X	X	32	390000h to 397FFFh
	SA122	0	1	1	1	0	0	1	1	X	X	X	32	398000h to 39FFFFh
	SA123	0	1	1	1	0	1	0	0	X	X	X	32	3A0000h to 3A7FFFh
	SA124	0	1	1	1	0	1	0	1	X	X	X	32	3A8000h to 3AFFFFh
	SA125	0	1	1	1	0	1	1	0	X	X	X	32	3B0000h to 3B7FFFh
	SA126	0	1	1	1	0	1	1	1	X	X	X	32	3B8000h to 3BFFFFh
	SA127	0	1	1	1	1	0	0	0	X	X	X	32	3C0000h to 3C7FFFh
	SA128	0	1	1	1	1	0	0	1	X	X	X	32	3C8000h to 3CFFFFh
	SA129	0	1	1	1	1	0	1	0	X	X	X	32	3D0000h to 3D7FFFh
	SA130	0	1	1	1	1	0	1	1	X	X	X	32	3D8000h to 3DFFFFh
	SA131	0	1	1	1	1	1	0	0	X	X	X	32	3E0000h to 3E7FFFh
	SA132	0	1	1	1	1	1	0	1	X	X	X	32	3E8000h to 3EFFFFh
	SA133	0	1	1	1	1	1	1	0	X	X	X	32	3F0000h to 3F7FFFh
SA134	0	1	1	1	1	1	1	1	X	X	X	32	3F8000h to 3FFFFFh	

MBM29QM12DH-60

Sector Address Table (Bank C)

Bank	Sector	Sector Address											Sector Size (Kwords)	(× 16) Address Range	
		Bank Address			A ₁₉	A ₁₈	A ₁₇	A ₁₆	A ₁₅	A ₁₄	A ₁₃	A ₁₂			
		A ₂₂	A ₂₁	A ₂₀											
Bank C	SA135	1	0	0	0	0	0	0	0	0	X	X	X	32	400000h to 407FFFh
	SA136	1	0	0	0	0	0	0	1	X	X	X	32	408000h to 40FFFFh	
	SA137	1	0	0	0	0	0	1	0	X	X	X	32	410000h to 417FFFh	
	SA138	1	0	0	0	0	0	1	1	X	X	X	32	418000h to 41FFFFh	
	SA139	1	0	0	0	0	1	0	0	X	X	X	32	420000h to 427FFFh	
	SA140	1	0	0	0	0	1	0	1	X	X	X	32	428000h to 42FFFFh	
	SA141	1	0	0	0	0	1	1	0	X	X	X	32	430000h to 437FFFh	
	SA142	1	0	0	0	0	1	1	1	X	X	X	32	438000h to 43FFFFh	
	SA143	1	0	0	0	1	0	0	0	X	X	X	32	440000h to 447FFFh	
	SA144	1	0	0	0	1	0	0	1	X	X	X	32	448000h to 44FFFFh	
	SA145	1	0	0	0	1	0	1	0	X	X	X	32	450000h to 457FFFh	
	SA146	1	0	0	0	1	0	1	1	X	X	X	32	458000h to 45FFFFh	
	SA147	1	0	0	0	1	1	0	0	X	X	X	32	460000h to 467FFFh	
	SA148	1	0	0	0	1	1	0	1	X	X	X	32	468000h to 46FFFFh	
	SA149	1	0	0	0	1	1	1	0	X	X	X	32	470000h to 477FFFh	
	SA150	1	0	0	0	1	1	1	1	X	X	X	32	478000h to 47FFFFh	
	SA151	1	0	0	1	0	0	0	0	X	X	X	32	480000h to 487FFFh	
	SA152	1	0	0	1	0	0	0	1	X	X	X	32	488000h to 48FFFFh	
	SA153	1	0	0	1	0	0	1	0	X	X	X	32	490000h to 497FFFh	
	SA154	1	0	0	1	0	0	1	1	X	X	X	32	498000h to 49FFFFh	
	SA155	1	0	0	1	0	1	0	0	X	X	X	32	4A0000h to 4A7FFFh	
	SA156	1	0	0	1	0	1	0	1	X	X	X	32	4A8000h to 4AFFFFh	
	SA157	1	0	0	1	0	1	1	0	X	X	X	32	4B0000h to 4B7FFFh	
	SA158	1	0	0	1	0	1	1	1	X	X	X	32	4B8000h to 4BFFFFh	
	SA159	1	0	0	1	1	0	0	0	X	X	X	32	4C0000h to 4C7FFFh	
	SA160	1	0	0	1	1	0	0	1	X	X	X	32	4C8000h to 4CFFFFh	
	SA161	1	0	0	1	1	0	1	0	X	X	X	32	4D0000h to 4D7FFFh	
	SA162	1	0	0	1	1	0	1	1	X	X	X	32	4D8000h to 4DFFFFh	
	SA163	1	0	0	1	1	1	0	0	X	X	X	32	4E0000h to 4E7FFFh	
	SA164	1	0	0	1	1	1	0	1	X	X	X	32	4E8000h to 4EFFFFh	
SA165	1	0	0	1	1	1	1	0	X	X	X	32	4F0000h to 4F7FFFh		
SA166	1	0	0	1	1	1	1	1	X	X	X	32	4F8000h to 4FFFFFh		
SA167	1	0	1	0	0	0	0	0	X	X	X	32	500000h to 507FFFh		
SA168	1	0	1	0	0	0	0	1	X	X	X	32	508000h to 50FFFFh		
SA169	1	0	1	0	0	0	1	0	X	X	X	32	510000h to 517FFFh		
SA170	1	0	1	0	0	0	1	1	X	X	X	32	518000h to 51FFFFh		
SA171	1	0	1	0	0	1	0	0	X	X	X	32	520000h to 527FFFh		
SA172	1	0	1	0	0	1	0	1	X	X	X	32	528000h to 52FFFFh		
SA173	1	0	1	0	0	1	1	0	X	X	X	32	530000h to 537FFFh		

(Continued)

Bank	Sector	Sector Address										Sector Size (Kwords)	(× 16) Address Range	
		Bank Address			A ₁₉	A ₁₈	A ₁₇	A ₁₆	A ₁₅	A ₁₄	A ₁₃			A ₁₂
		A ₂₂	A ₂₁	A ₂₀										
Bank C	SA174	1	0	1	0	0	1	1	1	X	X	X	32	538000h to 53FFFFh
	SA175	1	0	1	0	1	0	0	0	X	X	X	32	540000h to 547FFFh
	SA176	1	0	1	0	1	0	0	1	X	X	X	32	548000h to 54FFFFh
	SA177	1	0	1	0	1	0	1	0	X	X	X	32	550000h to 557FFFh
	SA178	1	0	1	0	1	0	1	1	X	X	X	32	558000h to 55FFFFh
	SA179	1	0	1	0	1	1	0	0	X	X	X	32	560000h to 567FFFh
	SA180	1	0	1	0	1	1	0	1	X	X	X	32	568000h to 56FFFFh
	SA181	1	0	1	0	1	1	1	0	X	X	X	32	570000h to 577FFFh
	SA182	1	0	1	0	1	1	1	1	X	X	X	32	578000h to 57FFFFh
	SA183	1	0	1	1	0	0	0	0	X	X	X	32	580000h to 587FFFh
	SA184	1	0	1	1	0	0	0	1	X	X	X	32	588000h to 58FFFFh
	SA185	1	0	1	1	0	0	1	0	X	X	X	32	590000h to 597FFFh
	SA186	1	0	1	1	0	0	1	1	X	X	X	32	598000h to 59FFFFh
	SA187	1	0	1	1	0	1	0	0	X	X	X	32	5A0000h to 5A7FFFh
	SA188	1	0	1	1	0	1	0	1	X	X	X	32	5A8000h to 5AFFFFh
	SA189	1	0	1	1	0	1	1	0	X	X	X	32	5B0000h to 5B7FFFh
	SA190	1	0	1	1	0	1	1	1	X	X	X	32	5B8000h to 5BFFFFh
	SA191	1	0	1	1	1	0	0	0	X	X	X	32	5C0000h to 5C7FFFh
	SA192	1	0	1	1	1	0	0	1	X	X	X	32	5C8000h to 5CFFFFh
	SA193	1	0	1	1	1	0	1	0	X	X	X	32	5D0000h to 5D7FFFh
	SA194	1	0	1	1	1	0	1	1	X	X	X	32	5D8000h to 5DFFFFh
	SA195	1	0	1	1	1	1	0	0	X	X	X	32	5E0000h to 5E7FFFh
	SA196	1	0	1	1	1	1	0	1	X	X	X	32	5E8000h to 5EFFFFh
	SA197	1	0	1	1	1	1	1	0	X	X	X	32	5F0000h to 5F7FFFh
SA198	1	0	1	1	1	1	1	1	X	X	X	32	5F8000h to 5FFFFFh	
SA199	1	1	0	0	0	0	0	0	X	X	X	32	600000h to 607FFFh	
SA200	1	1	0	0	0	0	0	1	X	X	X	32	608000h to 60FFFFh	
SA201	1	1	0	0	0	0	1	0	X	X	X	32	610000h to 617FFFh	
SA202	1	1	0	0	0	0	1	1	X	X	X	32	618000h to 61FFFFh	
SA203	1	1	0	0	0	1	0	0	X	X	X	32	620000h to 627FFFh	
SA204	1	1	0	0	0	1	0	1	X	X	X	32	628000h to 62FFFFh	
SA205	1	1	0	0	0	1	1	0	X	X	X	32	630000h to 637FFFh	
SA206	1	1	0	0	0	1	1	1	X	X	X	32	638000h to 63FFFFh	
SA207	1	1	0	0	1	0	0	0	X	X	X	32	640000h to 647FFFh	
SA208	1	1	0	0	1	0	0	1	X	X	X	32	648000h to 64FFFFh	
SA209	1	1	0	0	1	0	1	0	X	X	X	32	650000h to 657FFFh	
SA210	1	1	0	0	1	0	1	1	X	X	X	32	658000h to 65FFFFh	
SA211	1	1	0	0	1	1	0	0	X	X	X	32	660000h to 667FFFh	
SA212	1	1	0	0	1	1	0	1	X	X	X	32	668000h to 66FFFFh	

(Continued)

MBM29QM12DH-60

(Continued)

Bank	Sector	Sector Address											Sector Size (Kwords)	(× 16) Address Range
		Bank Address			A ₁₉	A ₁₈	A ₁₇	A ₁₆	A ₁₅	A ₁₄	A ₁₃	A ₁₂		
		A ₂₂	A ₂₁	A ₂₀										
Bank C	SA213	1	1	0	0	1	1	1	0	X	X	X	32	670000h to 677FFFh
	SA214	1	1	0	0	1	1	1	1	X	X	X	32	678000h to 67FFFFh
	SA215	1	1	0	1	0	0	0	0	X	X	X	32	680000h to 687FFFh
	SA216	1	1	0	1	0	0	0	1	X	X	X	32	688000h to 68FFFFh
	SA217	1	1	0	1	0	0	1	0	X	X	X	32	690000h to 697FFFh
	SA218	1	1	0	1	0	0	1	1	X	X	X	32	698000h to 69FFFFh
	SA219	1	1	0	1	0	1	0	0	X	X	X	32	6A0000h to 6A7FFFh
	SA220	1	1	0	1	0	1	0	1	X	X	X	32	6A8000h to 6AFFFFh
	SA221	1	1	0	1	0	1	1	0	X	X	X	32	6B0000h to 6B7FFFh
	SA222	1	1	0	1	0	1	1	1	X	X	X	32	6B8000h to 6BFFFFh
	SA223	1	1	0	1	1	0	0	0	X	X	X	32	6C0000h to 6C7FFFh
	SA224	1	1	0	1	1	0	0	1	X	X	X	32	6C8000h to 6CFFFFh
	SA225	1	1	0	1	1	0	1	0	X	X	X	32	6D0000h to 6D7FFFh
	SA226	1	1	0	1	1	0	1	1	X	X	X	32	6D8000h to 6DFFFFh
	SA227	1	1	0	1	1	1	0	0	X	X	X	32	6E0000h to 6E7FFFh
	SA228	1	1	0	1	1	1	0	1	X	X	X	32	6E8000h to 6EFFFFh
	SA229	1	1	0	1	1	1	1	0	X	X	X	32	6F0000h to 6F7FFFh
SA230	1	1	0	1	1	1	1	1	X	X	X	32	6F8000h to 6FFFFFh	

Sector Address Table (Bank D)

Bank	Sector	Sector Address											Sector Size (Kwords)	Address Range (× 16)
		Bank Address			A ₁₉	A ₁₈	A ₁₇	A ₁₆	A ₁₅	A ₁₄	A ₁₃	A ₁₂		
		A ₂₂	A ₂₁	A ₂₀										
Bank D	SA231	1	1	1	0	0	0	0	0	X	X	X	32	70000h to 707FFFh
	SA232	1	1	1	0	0	0	0	1	X	X	X	32	708000h to 70FFFFh
	SA233	1	1	1	0	0	0	1	0	X	X	X	32	710000h to 717FFFh
	SA234	1	1	1	0	0	0	1	1	X	X	X	32	718000h to 71FFFFh
	SA235	1	1	1	0	0	1	0	0	X	X	X	32	720000h to 727FFFh
	SA236	1	1	1	0	0	1	0	1	X	X	X	32	728000h to 72FFFFh
	SA237	1	1	1	0	0	1	1	0	X	X	X	32	730000h to 737FFFh
	SA238	1	1	1	0	0	1	1	1	X	X	X	32	738000h to 73FFFFh
	SA239	1	1	1	0	1	0	0	0	X	X	X	32	740000h to 747FFFh
	SA240	1	1	1	0	1	0	0	1	X	X	X	32	748000h to 74FFFFh
	SA241	1	1	1	0	1	0	1	0	X	X	X	32	750000h to 757FFFh
	SA242	1	1	1	0	1	0	1	1	X	X	X	32	758000h to 75FFFFh
	SA243	1	1	1	0	1	1	0	0	X	X	X	32	760000h to 767FFFh
	SA244	1	1	1	0	1	1	0	1	X	X	X	32	768000h to 76FFFFh
	SA245	1	1	1	0	1	1	1	0	X	X	X	32	770000h to 777FFFh
	SA246	1	1	1	0	1	1	1	1	X	X	X	32	778000h to 77FFFFh
	SA247	1	1	1	1	0	0	0	0	X	X	X	32	780000h to 787FFFh
	SA248	1	1	1	1	0	0	0	1	X	X	X	32	788000h to 78FFFFh
	SA249	1	1	1	1	0	0	1	0	X	X	X	32	790000h to 797FFFh
	SA250	1	1	1	1	0	0	1	1	X	X	X	32	798000h to 79FFFFh
	SA251	1	1	1	1	0	1	0	0	X	X	X	32	7A0000h to 7A7FFFh
	SA252	1	1	1	1	0	1	0	1	X	X	X	32	7A8000h to 7AFFFFh
	SA253	1	1	1	1	0	1	1	0	X	X	X	32	7B0000h to 7B7FFFh
	SA254	1	1	1	1	0	1	1	1	X	X	X	32	7B8000h to 7BFFFFh
	SA255	1	1	1	1	1	0	0	0	X	X	X	32	7C0000h to 7C7FFFh
	SA256	1	1	1	1	1	0	0	1	X	X	X	32	7C8000h to 7CFFFFh
	SA257	1	1	1	1	1	0	1	0	X	X	X	32	7D0000h to 7D7FFFh
	SA258	1	1	1	1	1	0	1	1	X	X	X	32	7D8000h to 7DFFFFh
	SA259	1	1	1	1	1	1	0	0	X	X	X	32	7E0000h to 7E7FFFh
SA260	1	1	1	1	1	1	0	1	X	X	X	32	7E8000h to 7EFFFFh	
SA261	1	1	1	1	1	1	1	0	X	X	X	32	7F0000h to 7F7FFFh	
SA262	1	1	1	1	1	1	1	1	0	0	0	4	7F8000h to 7F8FFFh	
SA263	1	1	1	1	1	1	1	1	0	0	1	4	7F9000h to 7F9FFFh	
SA264	1	1	1	1	1	1	1	1	0	1	0	4	7FA000h to 7FAFFFh	
SA265	1	1	1	1	1	1	1	1	0	1	1	4	7FB000h to 7FBFFFh	
SA266	1	1	1	1	1	1	1	1	1	0	0	4	7FC000h to 7FCFFFh	
SA267	1	1	1	1	1	1	1	1	1	0	1	4	7FD000h to 7FDFFFh	
SA268	1	1	1	1	1	1	1	1	1	1	0	4	7FE000h to 7FEFFFh	
SA269	1	1	1	1	1	1	1	1	1	1	1	4	7FF000h to 7FFFFFFh	

MBM29QM12DH-60

Sector Group Address Table

Sector Group	A ₂₂	A ₂₁	A ₂₀	A ₁₉	A ₁₈	A ₁₇	A ₁₆	A ₁₅	A ₁₄	A ₁₃	A ₁₂	Sectors
SGA0	0	0	0	0	0	0	0	0	0	0	0	SA0
SGA1	0	0	0	0	0	0	0	0	0	0	1	SA1
SGA2	0	0	0	0	0	0	0	0	0	1	0	SA2
SGA3	0	0	0	0	0	0	0	0	0	1	1	SA3
SGA4	0	0	0	0	0	0	0	0	1	0	0	SA4
SGA5	0	0	0	0	0	0	0	0	1	0	1	SA5
SGA6	0	0	0	0	0	0	0	0	1	1	0	SA6
SGA7	0	0	0	0	0	0	0	0	1	1	1	SA7
SGA8	0	0	0	0	0	0	0	1	X	X	X	SA8
SGA9	0	0	0	0	0	0	1	0	X	X	X	SA9
SGA10	0	0	0	0	0	0	1	1	X	X	X	SA10
SGA11	0	0	0	0	0	1	X	X	X	X	X	SA11 to SA14
SGA12	0	0	0	0	1	0	X	X	X	X	X	SA15 to SA18
SGA13	0	0	0	0	1	1	X	X	X	X	X	SA19 to SA22
SGA14	0	0	0	1	0	0	X	X	X	X	X	SA23 to SA26
SGA15	0	0	0	1	0	1	X	X	X	X	X	SA27 to SA30
SGA16	0	0	0	1	1	0	X	X	X	X	X	SA31 to SA34
SGA17	0	0	0	1	1	1	X	X	X	X	X	SA35 to SA38
SGA18	0	0	1	0	0	0	X	X	X	X	X	SA39 to SA42
SGA19	0	0	1	0	0	1	X	X	X	X	X	SA43 to SA46
SGA20	0	0	1	0	1	0	X	X	X	X	X	SA47 to SA50
SGA21	0	0	1	0	1	1	X	X	X	X	X	SA51 to SA54
SGA22	0	0	1	1	0	0	X	X	X	X	X	SA55 to SA58
SGA23	0	0	1	1	0	1	X	X	X	X	X	SA59 to SA62
SGA24	0	0	1	1	1	0	X	X	X	X	X	SA63 to SA66
SGA25	0	0	1	1	1	1	X	X	X	X	X	SA67 to SA70
SGA26	0	1	0	0	0	0	X	X	X	X	X	SA71 to SA74
SGA27	0	1	0	0	0	1	X	X	X	X	X	SA75 to SA78

(Continued)

MBM29QM12DH-60

Sector Group	A ₂₂	A ₂₁	A ₂₀	A ₁₉	A ₁₈	A ₁₇	A ₁₆	A ₁₅	A ₁₄	A ₁₃	A ₁₂	Sectors
SGA28	0	1	0	0	1	0	X	X	X	X	X	SA79 to SA82
SGA29	0	1	0	0	1	1	X	X	X	X	X	SA83 to SA86
SGA30	0	1	0	1	0	0	X	X	X	X	X	SA87 to SA90
SGA31	0	1	0	1	0	1	X	X	X	X	X	SA91 to SA94
SGA32	0	1	0	1	1	0	X	X	X	X	X	SA95 to SA98
SGA33	0	1	0	1	1	1	X	X	X	X	X	SA99 to SA102
SGA34	0	1	1	0	0	0	X	X	X	X	X	SA103 to SA106
SGA35	0	1	1	0	0	1	X	X	X	X	X	SA107 to SA110
SGA36	0	1	1	0	1	0	X	X	X	X	X	SA111 to SA114
SGA37	0	1	1	0	1	1	X	X	X	X	X	SA115 to SA118
SGA38	0	1	1	1	0	0	X	X	X	X	X	SA119 to SA122
SGA39	0	1	1	1	0	1	X	X	X	X	X	SA123 to SA126
SGA40	0	1	1	1	1	0	X	X	X	X	X	SA127 to SA130
SGA41	0	1	1	1	1	1	X	X	X	X	X	SA131 to SA134
SGA42	1	0	0	0	0	0	X	X	X	X	X	SA135 to SA138
SGA43	1	0	0	0	0	1	X	X	X	X	X	SA139 to SA142
SGA44	1	0	0	0	1	0	X	X	X	X	X	SA143 to SA146
SGA45	1	0	0	0	1	1	X	X	X	X	X	SA147 to SA150
SGA46	1	0	0	1	0	0	X	X	X	X	X	SA151 to SA154
SGA47	1	0	0	1	0	1	X	X	X	X	X	SA155 to SA158
SGA48	1	0	0	1	1	0	X	X	X	X	X	SA159 to SA162
SGA49	1	0	0	1	1	1	X	X	X	X	X	SA163 to SA166
SGA50	1	0	1	0	0	0	X	X	X	X	X	SA167 to SA170
SGA51	1	0	1	0	0	1	X	X	X	X	X	SA171 to SA174

(Continued)

MBM29QM12DH-60

(Continued)

Sector Group	A ₂₂	A ₂₁	A ₂₀	A ₁₉	A ₁₈	A ₁₇	A ₁₆	A ₁₅	A ₁₄	A ₁₃	A ₁₂	Sectors
SGA52	1	0	1	0	1	0	X	X	X	X	X	SA175 to SA178
SGA53	1	0	1	0	1	1	X	X	X	X	X	SA179 to SA182
SGA54	1	0	1	1	0	0	X	X	X	X	X	SA183 to SA186
SGA55	1	0	1	1	0	1	X	X	X	X	X	SA187 to SA190
SGA56	1	0	1	1	1	0	X	X	X	X	X	SA191 to SA194
SGA57	1	0	1	1	1	1	X	X	X	X	X	SA195 to SA198
SGA58	1	1	0	0	0	0	X	X	X	X	X	SA199 to SA202
SGA59	1	1	0	0	0	1	X	X	X	X	X	SA203 to SA206
SGA60	1	1	0	0	1	0	X	X	X	X	X	SA207 to SA210
SGA61	1	1	0	0	1	1	X	X	X	X	X	SA211 to SA214
SGA62	1	1	0	1	0	0	X	X	X	X	X	SA215 to SA218
SGA63	1	1	0	1	0	1	X	X	X	X	X	SA219 to SA222
SGA64	1	1	0	1	1	0	X	X	X	X	X	SA223 to SA226
SGA65	1	1	0	1	1	1	X	X	X	X	X	SA227 to SA230
SGA66	1	1	1	0	0	0	X	X	X	X	X	SA231 to SA234
SGA67	1	1	1	0	0	1	X	X	X	X	X	SA235 to SA238
SGA68	1	1	1	0	1	0	X	X	X	X	X	SA239 to SA242
SGA69	1	1	1	0	1	1	X	X	X	X	X	SA243 to SA246
SGA70	1	1	1	1	0	0	X	X	X	X	X	SA247 to SA250
SGA71	1	1	1	1	0	1	X	X	X	X	X	SA251 to SA254
SGA72	1	1	1	1	1	0	X	X	X	X	X	SA255 to SA258
SGA73	1	1	1	1	1	1	0	0	X	X	X	SA259
SGA74	1	1	1	1	1	1	0	1	X	X	X	SA260
SGA75	1	1	1	1	1	1	1	0	X	X	X	SA261
SGA76	1	1	1	1	1	1	1	1	0	0	0	SA262
SGA77	1	1	1	1	1	1	1	1	0	0	1	SA263
SGA78	1	1	1	1	1	1	1	1	0	1	0	SA264
SGA79	1	1	1	1	1	1	1	1	0	1	1	SA265
SGA80	1	1	1	1	1	1	1	1	1	0	0	SA266
SGA81	1	1	1	1	1	1	1	1	1	0	1	SA267
SGA82	1	1	1	1	1	1	1	1	1	1	0	SA268
SGA83	1	1	1	1	1	1	1	1	1	1	1	SA269

Common Flash Memory Interface Code Table

Description	A ₆ to A ₀	DQ ₁₅ to DQ ₀	Description	A ₆ to A ₀	DQ ₁₅ to DQ ₀
Query-unique ASCII string "QRY"	10h	0051h	Erase Block Region 4 Information	39h	0000h
	11h	0052h		3Ah	0000h
	12h	0059h		3Bh	0000h
		3Ch		0000h	
Primary OEM Command Set	13h	0002h	Query-unique ASCII string "PRI"	40h	0050h
02h: AMD/FJ standard type	14h	0000h		41h	0052h
Address for Primary Extended Table	15h	0040h		42h	0049h
Alternate OEM Command Set (00h = not applicable)	16h	0000h	Major version number, ASCII	43h	0031h
	17h	0000h	Minor version number, ASCII	44h	0033h
Address for Alternate OEM Extended Table	18h	0000h	Address Sensitive Unlock Ch = Required and 0.13 μm technology Dh = Not Required and 0.13 μm technology	45h	000Ch
V _{CC} Min voltage (write/erase) DQ ₇ to DQ ₄ : 1 V, DQ ₃ to DQ ₀ : 100 mV	19h	0000h			
V _{CC} Max voltage (write/erase) DQ ₇ to DQ ₄ : 1 V, DQ ₃ to DQ ₀ : 100 mV	1Ah	0000h	Erase Suspend 02h = To Read & Write	46h	0002h
V _{PP} Min voltage	1Bh	0027h	Sector Protection 00h = Not Supported X = Number of sectors in per group	47h	0001h
V _{PP} Max voltage	1Ch	0036h			
Typical timeout per single byte/word write 2 ^N μs	1Dh	0000h	Sector Temporary Unprotection 01h = Supported	48h	0001h
Typical timeout for Min size buffer write 2 ^N μs	1Eh	0000h	Sector Protection Algorithm	49h	0007h
Typical timeout per individual block erase 2 ^N ms	1Fh	0004h	Simultaneous Operation 00h = Not Supported, X = Total number of sectors in all Banks except Bank A	4Ah	00E7h
Typical timeout for full chip erase 2 ^N ms	20h	0000h			
Max timeout for byte/word write 2 ^N times typical	21h	0009h	Burst Mode Type 00h = Not Supported	4Bh	0000h
Max timeout for buffer write 2 ^N times typical	22h	0000h	Page Mode Type 00h = Not Supported	4Ch	0002h
Max timeout per individual block erase 2 ^N times typical	23h	0005h	V _{ACC} (Acceleration) Supply Minimum 00h = Not Supported, DQ ₇ to DQ ₄ : 1 V, DQ ₃ to DQ ₀ : 100 mV	4Dh	0085h
Max timeout for full chip erase 2 ^N times typical	24h	0000h			
Device Size = 2 ^N byte	25h	0004h	V _{ACC} (Acceleration) Supply Maximum 00h = Not Supported, DQ ₇ to DQ ₄ : 1 V, DQ ₃ to DQ ₀ : 100 mV	4Eh	0095h
Flash Device Interface description 01h : × 16	26h	0000h	Boot Type	4Fh	0001h
Max number of byte in multi-byte write = 2 ^N	27h	0018h	Program Suspend 01h = Supported	50h	0001h
	28h	0001h	Bank Organization	57h	0004h
Number of Erase Block Regions within device	29h	0000h	Bank A Region Information	58h	0027h
	2Ah	0000h	Bank B Region Information	59h	0060h
	2Bh	0000h	Bank C Region Information	5Ah	0060h
	2Ch	0003h	Bank D Region Information	5Bh	0027h
Erase Block Region 1 Information	2Dh	0007h			
	2Eh	0000h			
	2Fh	0020h			
	30h	0000h			
Erase Block Region 2 Information	31h	00FDh			
	32h	0000h			
	33h	0000h			
	34h	0001h			
Erase Block Region 3 Information	35h	0007h			
	36h	0000h			
	37h	0020h			
	38h	0000h			

FUNCTIONAL DESCRIPTION

Simultaneous Operation

The device features functions that enable reading of data from one memory bank while a program or erase operation is in progress in the other memory bank (simultaneous operation), in addition to conventional features (read, program, erase, erase-suspend read, and erase-suspend program). The bank can be selected by bank address (A_{22} , A_{21} , A_{20}) with zero latency. The device consists of the following four banks:

Bank A : 8×4 KW and 31×32 KW; Bank B : 96×32 KW; Bank C : 96×32 KW; Bank D : 8×4 KW and 31×32 KW.

The device can execute simultaneous operations between Bank 1, a bank chosen from among the four banks, and Bank 2, a bank consisting of the three remaining banks. (See "FlexBank™ Architecture Table" in "FUNCTIONAL DESCRIPTION".) This is what we call a "FlexBank", for example, the rest of banks B, C and D to let the system read while Bank A is in the process of program (or erase) operation. However, the different types of operations for the three banks are impossible, e.g. Bank A writing, Bank B erasing, and Bank C reading out. With this "FlexBank", as described in "Example of Virtual Banks Combination Table" in "FUNCTIONAL DESCRIPTION", the system gets to select from four combinations of data volume for Bank 1 and Bank 2, which works well to meet the system requirement. The simultaneous operation cannot execute multi-function mode in the same bank. "Simultaneous Operation Table" in "FUNCTIONAL DESCRIPTION" shows the possible combinations for simultaneous operation. (Refer to "Bank-to-Bank Read/Write Timing Diagram" in "TIMING DIAGRAM".)

FlexBank™ Architecture Table

Bank Splits	Bank 1		Bank 2	
	Volume	Combination	Volume	Combination
1	16 Mbit	Bank A	112 Mbit	Remainder (Bank B, C, D)
2	48 Mbit	Bank B	80 Mbit	Remainder (Bank A, C, D)
3	48 Mbit	Bank C	80 Mbit	Remainder (Bank A, B, D)
4	16 Mbit	Bank D	112 Mbit	Remainder (Bank A, B, C)

Example of Virtual Banks Combination Table

Bank Splits	Bank 1			Bank 2		
	Volume	Combination	Sector Size	Volume	Combination	Sector Size
1	16 Mbit	Bank A	8×4 Kwords + 31×32 Kwords	112 Mbits	Bank B + Bank C + Bank D	8×4 Kwords + 223×32 Kwords
2	32 Mbit	Bank A + Bank D	16×4 Kwords + 62×32 Kwords	96 Mbits	Bank B + Bank C	192×32 Kwords
3	48 Mbit	Bank B	96×32 Kwords	80 Mbits	Bank A + Bank C + Bank D	16×4 Kwords + 158×32 Kwords
4	64 Mbit	Bank A + Bank B	8×4 Kwords + 127×32 Kwords	64 Mbits	Bank C + Bank D	8×4 Kwords + 127×32 Kwords

Note : When multiple sector erase over several banks is operated, the system cannot read out of the bank to which a sector being erased belongs. For example, suppose that erasing is taking place at both Bank A and Bank B, neither Bank A nor Bank B is read out (they would output the sequence flag once they were selected.) Meanwhile the system would get to read from either Bank C or Bank D.

Simultaneous Operation Table

Case	Bank 1 Status	Bank 2 Status
1	Read mode	Read mode
2	Read mode	Autoselect mode
3	Read mode	Program mode
4	Read mode	Erase mode
5	Autoselect mode	Read mode
6	Program mode	Read mode
7	Erase mode	Read mode

Note : Bank 1 and Bank 2 are divided for the sake of convenience at Simultaneous Operation. Actually, the Bank consists of 4 banks, Bank A, Bank B, BankC and Bank D. Bank Address (BA) means to specify each of the Banks.

Read Mode

The device has two control functions which are required in order to obtain data at the outputs. \overline{CE} is the power control and should be used for a device selection. \overline{OE} is the output control and should be used to gate data to the output pins.

Address access time (t_{ACC}) is equal to delay from stable addresses to valid output data. The chip enable access time (t_{CE}) is the delay from stable addresses and stable \overline{CE} to valid data at the output pins. The output enable access time is the delay from the falling edge of \overline{OE} to valid data at the output pins (assuming the addresses have been stable for at least $t_{ACC} - t_{OE}$ time) . When reading out data without changing addresses after power-up, it is necessary to input hardware reset or to change \overline{CE} pin from "H" or "L"

Page Mode Read

The device is capable of fast page mode read. This mode provides faster read access speed by sequential access within a page. The Page size of the device is 8 words, within the appropriate Page being selected by the higher address bits A_{22} to A_3 and the LSB bits A_2 to A_0 determining the specific word within that page. This is an asynchronous operation with the microprocessor supplying the specific word location.

The random or initial page access is equal to t_{ACC} and subsequent page read access (as long as the locations specified by the microprocessor fall within that Page) is equivalent to t_{PACC} . Here again, \overline{CE} selects the device and \overline{OE} is the output control and should be used to gate data to the output pins if the device is selected. Fast page mode accesses are obtained by keeping A_{22} to A_3 constant and changing A_2 to A_0 within that page.

Standby Mode

There are two ways to implement the standby mode on the device, one using both the \overline{CE} and \overline{RESET} pins, and the other via the \overline{RESET} pin only.

When using both pins, a CMOS standby mode is achieved with \overline{CE} and \overline{RESET} input held at $V_{CC} \pm 0.3$ V. Under this condition the current consumed is less than 5 μ A Max. During Embedded Algorithm operation, V_{CC} active current (I_{CC2}) is required even if $\overline{CE} = "H"$. The device can be read with standard access time (t_{CE}) from either of these standby modes.

When using the \overline{RESET} pin only, a CMOS standby mode is achieved with \overline{RESET} input held at $V_{SS} \pm 0.3$ V ($\overline{CE} = "H"$ or "L") . Under this condition the current consumed is less than 5 μ A Max. Once the \overline{RESET} pin is set high, the device requires t_{RH} as a wake-up time for output to be valid for read access.

During standby mode, the output is in the high impedance state, regardless of \overline{OE} input.

Automatic Sleep Mode

Automatic sleep mode works to restrain power consumption during read-out of device data. It can be useful in applications such as handy terminal, which requires low power consumption.

To activate this mode, the device automatically switches itself to low power mode when the device addresses remain stable during access time of 150 ns. It is not necessary to control \overline{CE} , \overline{WE} and \overline{OE} in this mode. In this mode the current consumed is typically 1 μ A (CMOS Level) .

During simultaneous operation, V_{CC} active current (I_{CC2}) is required.

Since the data are latched during this mode, the data are continuously read out. When the addresses are changed, the mode is automatically canceled and the device reads the data for changed addresses.

Output Disable

With the \overline{OE} input at a logic high level (V_{IH}) , output from the device is disabled. This will cause the output pins to be in a high impedance state.

Autoselect

The Autoselect mode allows the reading out of a binary code and identifies its manufacturer and type. It is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional over the entire temperature range of the device.

To activate this mode, the programming equipment must force V_{ID} on address pin A_9 . Three identifier bytes may then be sequenced from the device outputs by toggling addresses. All addresses are DON'T CARES except A_7 , A_6 , A_5 , A_4 , A_3 , A_2 , A_1 and A_0 . (See "MBM29QM12DH User Bus Operations Table" and "MBM29QM12DH Command Definitions Table" in "■ DEVICE BUS OPERATION".)

The manufacturer and device codes may also be read via the command register, for instances when the device is erased or programmed in a system without access to high voltage on the A_9 pin. The command sequence is illustrated in "MBM29QM12DH Command Definitions Table" in "■ DEVICE BUS OPERATION". (Refer to Autoselect Command section.)

In the command Autoselect mode, the bank addresses $BA_i(A_{22}, A_{21}, A_{20})$ must point to a specific bank during the third write bus cycle of the Autoselect command. Then the Autoselect data will be read from that bank while array data can be read from the other bank.

In WORD mode, a read cycle from address 00h returns the manufacturer's code (Fujitsu = 04h) . A read cycle at address 01h outputs device code. When 227Eh is output, it indicates that two additional codes, called Extended Device Codes will be required. Therefore the system may continue reading out these Extended Device Codes at addresses of 0Eh and 0Fh. (Refer to "MBM29QM12DH Sector Group Protection Verify Autoselect Codes Table" and "Extended Autoselect Code Table" in "■ DEVICE BUS OPERATION")

In the case of applying V_{ID} on A_9 , since both Bank 1 and Bank 2 enter Autoselect mode, simultaneous operation cannot be executed.

Write

Device erasure and programming are accomplished via the command register. The contents of the register serve as input to the internal state machine. The state machine output dictates the function of the device.

The command register itself does not occupy any addressable memory location. The register is a latch used to store the commands, along with the address and data information needed to execute the command. The command register is written by bringing \overline{WE} to V_{IL} , while \overline{CE} is at V_{IL} and \overline{OE} is at V_{IH} . Addresses are latched on the falling edge of \overline{WE} or \overline{CE} , whichever happens later, while data is latched on the rising edge of \overline{WE} or \overline{CE} , whichever happens first. Standard microprocessor write timings are used.

Refer to AC Write Characteristics and the Erase/Programming Waveforms for specific timing parameters.

Accelerated Program Operation

The device offers accelerated program operation which enables the programming in high speed. If the system asserts V_{ACC} to the $\overline{WP/ACC}$ pin, the device automatically enters the acceleration mode and the time required

for program operation will reduce to about 60%. This function is primarily intended to allow high speed program, so caution is needed as the sector group will temporarily be unprotected.

The system would use a fast program command sequence when programming during acceleration mode. Set command to fast mode and reset command from fast mode are not necessary. When the device enters the acceleration mode, the device automatically set to fast mode. Therefore, the present sequence could be used for programming and detection of completion during acceleration mode.

Removing V_{ACC} from the \overline{WP}/ACC pin returns the device to normal operation. Do not remove V_{ACC} from \overline{WP}/ACC pin while programming. See "Accelerated Program Timing Diagram" in "■ TIMING DIAGRAM".

RESET

Hardware Reset

The device may be reset by driving the \overline{RESET} pin to V_{IL} . The \overline{RESET} pin has a pulse requirement and has to be kept low (V_{IL}) for at least " t_{RP} " in order to properly reset the internal state machine. Any operation in the process of being executed will be terminated and the internal state machine will be reset to the read mode " t_{READY} " after the \overline{RESET} pin is driven low. Furthermore, once the \overline{RESET} pin goes high the device requires an additional " t_{RH} " before it will allow read access. When the \overline{RESET} pin is low, the device will be in the standby mode for the duration of the pulse and all the data output pins will be tri-stated. If a hardware reset occurs during a program or erase operation, the data at that particular location will be corrupted. Please note that the RY/BY output signal should be ignored during the \overline{RESET} pulse. See "RESET, RY/BY Timing Diagram" in "■ TIMING DIAGRAM" for the timing diagram. Refer to Temporary Sector Group Unprotection for additional functionality.

Boot Block Sector Protection

The write protection function provides a hardware method of protecting certain boot sectors without using V_{ID} . This function is one of two provided by the \overline{WP}/ACC pin.

If the system asserts V_{IL} on the \overline{WP}/ACC pin, the device disables program and erase functions in the two outermost 8K bytes on both ends of boot sectors (SA0, SA1, SA268, SA269) independently of whether those sectors are protected or unprotected using the method described in "Sector Group Protection".

If the system asserts V_{IH} on the \overline{WP}/ACC pin, the device reverts to whether the two outermost 8K byte on both ends of boot sectors were last set to be protected or unprotected. Sector group protection or unprotection for these four sectors depends on whether they were last protected or unprotected using the method described in "Sector Group Protection".

HiddenROM Region

The HiddenROM feature provides a Flash memory region that the system may access through a new command sequence. This is primarily intended for customers who wish to use an Electronic Serial Number (ESN) in the device with the ESN protected against modification. Once the HiddenROM region is protected, any further modification of that region becomes impossible. This ensures the security of the ESN once the product is shipped to the field. ONLY Program is possible in this area until it is protected. Once it is protected, it is impossible to unprotect, so please use this with caution.

HiddenROM area is 128 words (64 words for factory and 64 words for customer) in length and is stored at the same address of the "outermost" 4 Kwords boot sector. The device occupies the address of the 000000h to 00007Fh. After the system has written the Enter HiddenROM command sequence, the system may read the HiddenROM region by using the addresses normally occupied by the boot sector (particular area of SA0). That is, the device sends all commands that would normally be sent to the boot sector to the HiddenROM region. This mode of operation continues until the system issues the Exit HiddenROM command sequence, or until power is removed from the device. On power-up, or following a hardware reset, the device reverts to sending commands to the boot sector.

HiddenROM area is divided into two regions, which are Factory Locked area and Customer Locked area. The Factory Locked area is 64 words (address: 000000h to 00003Fh) that is programmed and locked at Fujitsu. The Customer Locked area is also 64 words (address: 000040h to 00007Fh) that is programmed and locked at user. The Factory indicator Bit (DQ₇) is used to indicate whether or not the Factory Locked area is locked when shipped from the factory. The Customer Indicator Bit (DQ₆) is used to indicate whether or not the Customer Locked area is locked. The Factory Locked area can be programmed and protected at Fujitsu ONLY and is always protected

when shipped from the factory regardless of the condition whether or not this area is programmed. Therefore this area has the Factory Indicator Bit (DQ₇) permanently set to a "1". The Factory Locked area cannot be modified in any way. The Customer Locked area is shipped unprotected, allowing users to utilize that area in any manner they choose. The Customer Indicator Bit set to "0". Once the Customer Locked area is protected, the Customer Indicator Bit will be permanently set to "1".

(3) Extended Sector Group Protection [Software Protection]

In addition to normal sector group protection, the device has Extended Sector Group Protection as an extended function. This function enables protection of the sector group by forcing V_{ID} on $\overline{\text{RESET}}$ pin and writes a command sequence. Unlike conventional procedures, it is not necessary to force V_{ID} and control timing for control pins. The only $\overline{\text{RESET}}$ pin requires V_{ID} for sector group protection in this mode. The extended sector group protection requires V_{ID} on $\overline{\text{RESET}}$ pin. With this condition the operation is initiated by writing the set-up command (60h) in the command register. Then the sector group addresses pins (A₂₂, A₂₁, A₂₀, A₁₉, A₁₈, A₁₇, A₁₆, A₁₅, A₁₄, A₁₃ and A₁₂) and (A₇, A₆, A₅, A₄, A₃, A₂, A₁, A₀) = (0, 0, 0, 0, 0, 0, 1, 0) should be set to the sector group to be protected (setting V_{IL} for the other address pins is recommended), and an extended sector group protection command (60h) should be written. A sector group is typically protected in 250 μs. To verify programming of the protection circuitry, the sector group addresses pins (A₂₂, A₂₁, A₂₀, A₁₉, A₁₈, A₁₇, A₁₆, A₁₅, A₁₄, A₁₃ and A₁₂) and (A₇, A₆, A₅, A₄, A₃, A₂, A₁, A₀) = (0, 0, 0, 0, 0, 0, 1, 0) should be set a command (40h) should be written. Following the command write, a logical "1" at device output DQ₀ will produce a protected sector in the read operation. If the output is logical "0", write the extended sector group protection command (60h) again. To terminate the operation, it is necessary to set $\overline{\text{RESET}}$ pin to V_{IH}. (Refer to "Extended Sector Group Protection Timing Diagram" in "■ TIMING DIAGRAM" and "Extended Sector Group Protection Algorithm" in "■ FLOW CHART".)

If Persistent Protection Bit Lock is set to "1", this mode is disabled.

(4) New Sector Protection [Software Protection]

A command sector protection method that replaces the old V_{ID} controlled protection method in the future. However MBM29QM12DH supports both V_{ID} protection and Persistent Sector Protection. Both are supported as a shift period.

The persistent Sector Protection and the old V_{ID} controlled protection can go back and forth until Persistent Protection Lock Bit is settled.

a) Persistent Protection Bit (PPB)

A single Persistent (non-volatile) Protection Bit is assigned to a maximum of four sectors (see the sector address tables for specific sector protection groupings). All 4 K words boot-block sectors have individual sector Persistent Protection Bits (PPBs) for greater flexibility. Each PPB is individually modifiable through the PPB Write Command.

Note: If a PPB requires erasure, all of the sector PPBs must first be preprogrammed prior to PPB erasing. All PPBs erase in parallel, unlike programming where individual PPBs are programmable. It is the responsibility of the user to perform the preprogramming operation. Otherwise, an already erased sector PPB has the potential of being over-erased. There is no hardware mechanism to prevent sector PPBs over-erasure.

b) Dynamic Protection Bit (DPB)

A volatile protection bit is assigned for each sector. After power-up or hardware reset, the contents of all DPBs is "0". Each DPB is individually modifiable through the DPB Write Command.

When the parts are first shipped, the PPBs are cleared, the DPBs are cleared, and PPB Lock is defaulted to power-up in the cleared state - meaning the PPBs are changeable.

When the device is first powered on the DPBs power up cleared (sectors not protected). The Protection State for each sector is determined by the logical OR of the PPB and the DPB related to that sector. For the sectors that have the PPBs cleared, the DPBs control whether or not the sector is protected or unprotected. By issuing the DPB Write/Erase command sequences, the DPBs will be set or cleared, thus placing each sector in the protected or unprotected state. These are the so-called Dynamic Locked or Unlocked states. They are called dynamic states because it is very easy to switch back and forth between the protected and unprotected conditions. This allows software to easily protect sectors against inadvertent changes yet does not prevent the easy removal of protection when changes are needed. The DPBs may be set or cleared as often as needed.

PPB vs DPB

The PPBs allow for a more static, and difficult to change, level of protection. The PPBs retain their state across power cycles because they are Non-Volatile. Individual PPBs are set with a command but must all be cleared as a group through a complex sequence of program and erasing commands. The PPBs are also limited to 100 erase cycles.

The PPB Lock bit adds an additional level of protection. Once all PPBs are programmed to the desired settings, the PPB Lock may be set to “1”. Setting the PPB Lock disables all program and erase commands to the Non-Volatile PPBs. In effect, the PPB Lock Bit locks the PPBs into their current state. The only way to clear the PPB Lock is to go through a power cycle. System boot code can determine if any changes to the PPB are needed e.g. to allow new system code to be downloaded. If no changes are needed then the boot code can set the PPB Lock to disable any further changes to the PPBs during system operation.

The \overline{WP}/ACC write protect pin adds a final level of hardware protection to the two outermost 4 Kwords sectors. When this pin is low it is not possible to change the contents of these two sectors. These sectors generally hold system boot code. So, the \overline{WP}/ACC pin can prevent any changes to the boot code that could override the choices made while setting up sector protection during system initialization.

It is possible to have sectors that have been persistently locked, and sectors that are left in the dynamic state. The sectors in the dynamic state are all unprotected. If there is a need to protect some of them, a simple DPB Write command sequence is all that is necessary. The DPB write/erase command for the dynamic sectors switch the DPBs to signify protected and unprotected, respectively. If there is a need to change the status of the persistently locked sectors, a few more steps are required. First, the PPB Lock bit must be disabled by either putting the device through a power-cycle, or hardware reset. The PPBs can then be changed to reflect the desired settings. Setting the PPB lock bit once again will lock the PPBs, and the device operates normally again.

Note: To achieve the best protection, it's recommended to execute the PPB lock bit set command early in the boot code, and protect the boot code by holding $\overline{WP}/ACC = V_{IL}$.

DPB	PPB	PPB Lock	Sector State
0	0	0	Unprotected—PPB and DPB are changeable
1	0	0	Protected—PPB and DPB are changeable
0	1	0	Protected—PPB and DPB are changeable
1	1	0	Protected—PPB and DPB are changeable
0	0	1	Unprotected—PPB is not changeable, DPB is changeable
1	0	1	Protected—PPB is not changeable, DPB is changeable
0	1	1	Protected—PPB is not changeable, DPB is changeable
1	1	1	Protected—PPB is not changeable, DPB is changeable

The above table contains all possible combinations of the DPB, PPB, and PPB lock relating to the status of the sector.

In summary, if the PPB is set, and the PPB lock is set, the sector is protected and the protection can not be removed until the next power cycle clears the PPB lock. If the PPB is cleared, the sector can be dynamically locked or unlocked. The DPB then controls whether or not the sector is protected or unprotected.

If the user attempts to program or erase a protected sector, the device ignores the command and returns to read mode. A program command to a protected sector enables status polling for approximately 1 μ s before the device returns to read mode without having modified the contents of the protected sector. An erase command to a protected sector enables status polling for approximately 50 μ s after which the device returns to read mode without having erased the protected sector.

The programming of the DPB, PPB, and PPB lock for a given sector can be verified by writing a DPB/PPB lock verify command to the device.

–DPB Status

The programming of the DPB for a given sector can be verified by writing a DPB status verify command to the device.

–PPB Status

The programming of the PPB for a given sector can be verified by writing a PPB status verify command to the device.

–PPB Lock Bit Status

The programming of the PPB Lock Bit for a given sector can be verified by writing a PPB Lock Bit status verify command to the device.

c) Persistent Protection Bit Lock (PPB Lock)

- **PPB Locked**
- **PPB Locked with Password**

A highly sophisticated protection method that requires a password before changes to certain sectors or sector groups are permitted.

All parts default to operate in the Persistent Sector Protection mode. The customer must then choose if the Persistent or Password Protection method is most desirable. There are two one-time programmable non-volatile bits that define which sector protection method will be used. If the customer decides to continue using the Persistent Sector Protection method, they must set the Persistent Sector Protection Mode Locking Bit. This will permanently set the part to operate only using Persistent Sector Protection. If the customer decides to use the password method, they must set the Password Mode Locking Bit. This will permanently set the part to operate only using password sector protection.

It is important to remember that setting either the Persistent Sector Protection Mode Locking Bit or the Password Mode Locking Bit permanently selects the protection mode. It is not possible to switch between the two methods once a locking bit has been set. It is important that one mode is explicitly selected when the device is first programmed, rather than relying on the default mode alone. This is so that it is not possible for a system program or virus to later set the Password Mode Locking Bit, which would cause an unexpected shift from the default Persistent Sector Protection Mode into the Password Protection Mode.

The \overline{WP}/ACC Hardware Protection feature is always available, independent of the software managed protection method chosen.

A global volatile bit. When set to “1”, the PPBs cannot be changed. When cleared (“0”), the PPBs are changeable. There is only one PPB Lock bit per device. The PPB Lock is cleared after power-up or hardware reset. There is no command sequence to unlock the PPB Lock.

The Persistent Protection Bit (PPB) Lock is a volatile bit that reflects the state of the Password Mode Locking Bit after power-up reset. If the Password Mode Locking Bit is set, which indicates the device is in Password Protection Mode, the PPB Lock Bit is also set after a hardware reset (\overline{RESET} asserted) or a power-up reset. The ONLY means for clearing the PPB Lock Bit in Password Protection Mode is to issue the Password Unlock command. Successful execution of the Password Unlock command clears the PPB Lock Bit, allowing for sector PPBs modifications. Asserting \overline{RESET} , taking the device through a power-on reset, or issuing the PPB Lock Bit Set command sets the PPB Lock Bit back to a “1”.

If the Password Mode Locking Bit is not set, indicating Persistent Sector Protection Mode, the PPB Lock Bit is cleared after power-up or hardware reset. The PPB Lock Bit is set by issuing the PPB Lock Bit Set command. Once set the only means for clearing the PPB Lock Bit is by issuing a hardware or power-up reset. The Password Unlock command is ignored in Persistent Sector Protection Mode.

-Password and Password Mode Locking Bit

In order to select the Password sector protection scheme, the customer must first program the password. Fujitsu recommends that the password be somehow correlated to the unique Electronic Serial Number (ESN) of the particular flash device. Each ESN is different for every flash device; therefore each password should be different for every flash device. While programming in the password region, the customer may perform Password Verify operations.

Once the desired password is programmed in, the customer must then set the Password Mode Locking Bit. This operation achieves two objectives:

- (1) It permanently sets the device to operate using the Password Protection Mode. It is not possible to reverse this function.
- (2) It also disables all further commands to the password region. All program, and read operations are ignored.

Both of these objectives are important, and if not carefully considered, may lead to unrecoverable errors. The user must be sure that the Password Protection method is desired when setting the Password Mode Locking Bit. More importantly, the user must be sure that the password is correct when the Password Mode Locking Bit is set. Due to the fact that read operations are disabled, there is no means to verify what the password is afterwards. If the password is lost after setting the Password Mode Locking Bit, there will be no way to clear the PPB Lock bit.

The Password Mode Locking Bit, once set, prevents reading the 64-bit password on the DQ bus and further password programming. The Password Mode Locking Bit is not erasable. Once Password Mode Locking Bit is programmed, the Persistent Sector Protection Locking Bit is disabled from programming, guaranteeing that no changes to the protection scheme are allowed.

64-bit Password

The 64-bit Password is located in its own memory space and is accessible through the use of the Password Program and Verify commands (see "Password Verify Command"). The password function works in conjunction with the Password Mode Locking Bit, which when set, prevents the Password Verify command from reading the contents of the password on the pins of the device.

-Persistent Sector Protection Mode Locking Bit

Like the password mode locking bit, a Persistent Sector Protection mode locking bit exists to guarantee that the device remain in software sector protection. Once set, the Persistent Sector Protection locking bit prevents programming of the password protection mode locking bit. This guarantees that a hacker could not place the device in password protection mode.

(5) Temporary Sector Group Unprotection

This feature allows temporary unprotection of previously protected sectors of the device in order to change data. The Sector Unprotection mode is activated by setting the RESET pin to high voltage (V_{DD}). During this mode, formerly protected sector groups can be programmed or erased by selecting the sector group addresses. Once the V_{DD} is taken away from the RESET pin, all the previously protected sector groups will be protected again. While PPB Lock is set, this device cannot enter the Temporary Sector Unprotection mode.

■ COMMAND DEFINITION

Device operations are selected by writing specific address and data sequences into the command register. Some commands require Bank Address (BA) input. When command sequences are input into a bank reading, the commands have priority over the reading. "MBM29QM12DH Command Definitions Table" in "■ DEVICE BUS OPERATION" shows the valid register command sequences. Note that the Erase Suspend (B0h) and Erase Resume (30h) commands are valid only while the Sector Erase operation is in progress. Also the Program Suspend (B0h) and Program Resume (30h) commands are valid only while the Program operation is in progress. Moreover, Read/Reset commands are functionally equivalent, resetting the device to the read mode. Please note that commands are always written at DQ₇ to DQ₀ and DQ₁₅ to DQ₈ bits are ignored. Writing incorrect address and data values or writing them in the improper sequence will take the device into unknown state.

Read/Reset Command

In order to return from Autoselect mode or Exceeded Timing Limits (DQ₅ = 1) to Read/Reset mode, the Read/Reset operation is initiated by writing the Read/Reset command sequence into the command register. Microprocessor read cycles retrieve array data from the memory. The device remains enabled for reads until the command register contents are altered.

The device will automatically power-up in the Read/Reset state. In this case a command sequence is not required in order to read data. Standard microprocessor read cycles will retrieve array data. This default value ensures that no spurious alteration of the memory content occurs during the power transition. Refer to AC Read Characteristics and Timing Diagram for the specific timing parameters.

Autoselect Command

Flash memories are intended for use in applications where the local CPU alters memory contents. Therefore, manufacture and device codes must be accessible while the device resides in the target system. PROM programmers typically access the signature codes by raising A₉ to a higher voltage. However, multiplexing high voltage onto the address lines is not generally desired system design practice.

The device contains an Autoselect command operation to supplement traditional PROM programming methodology. The operation is initiated by writing the Autoselect command sequence into the command register.

The Autoselect command sequence is initiated first by writing two unlock cycles. This is followed by a third write cycle that contains the bank address (BA) and the Autoselect command. Then the manufacture and device codes can be read from the bank, and actual data from the memory cell can be read from another bank. The higher order address (A₂₂, A₂₁, A₂₀) required for reading out the manufacture and device codes demands the bank address (BA) set at the third write cycle.

Following the command write, in WORD mode, a read cycle from address (BA) 00h returns the manufacturer's code (Fujitsu = 04h). And a read cycle at address (BA) 01h outputs device code. When 227Eh was output, this indicates that two additional codes, called Extended Device Codes will be required. Therefore the system may continue reading out these Extended Device Codes at the address of (BA) 0Eh, as well as at (BA) 0Fh. Notice that the above applies to WORD mode. (Refer to "MBM29QM12DH Sector Group Protection Verify Autoselect Codes Table" and "Extended Autoselect Code Table" in "■ DEVICE BUS OPERATION")

The sector state (PPB protection or PPB unprotection) will be informed by address (BA) XX02h for $\times 16$. Scanning the sector group addresses (A₂₂, A₂₁, A₂₀, A₁₉, A₁₈, A₁₇, A₁₆, A₁₅, A₁₄, A₁₃, and A₁₂) while (A₇, A₆, A₅, A₄, A₃, A₂, A₁, A₀) = (0, 0, 0, 0, 0, 0, 1, 0) will produce a logical "1" at device output DQ₀ for a protected sector group. The programming verification should be performed by verifying sector group protection on the protected sector. (See "MBM29QM12DH User Bus Operations Table" and "MBM29QM12DH Command Definitions Table" in "■ DEVICE BUS OPERATION".)

The manufacture and device codes can be read from the selected bank. To read the manufacture and device codes and sector protection status from a non-selected bank, it is necessary to write the Read/Reset command sequence into the register. Autoselect command should then be written into the bank to be read.

If the software (program code) for Autoselect command is stored in the Flash memory, the device and manufacture codes should be read from the other bank, which does not contain the software.

To terminate the operation, it is necessary to write the Read/Reset command sequence into the register. To execute the Autoselect command during the operation, Read/Reset command sequence must be written before the Autoselect command.

Word Programming Command

The device is programmed on a word-by-word basis. Programming is a four bus cycle operation. There are two “unlock” write cycles. These are followed by the program set-up command and data write cycles. Addresses are latched on the falling edge of \overline{CE} or \overline{WE} , whichever happens later, and the data is latched on the rising edge of \overline{CE} or \overline{WE} , whichever happens first. The rising edge of \overline{CE} or \overline{WE} (whichever happens first) starts programming. Upon executing the Embedded Program Algorithm command sequence, the system is not required to provide further controls or timings. The device will automatically provide adequate internally generated program pulses and verify the programmed cell margin.

The system can determine the status of the program operation by using DQ₇ ($\overline{\text{Data}}$ Polling) , DQ₆ (Toggle Bit) or RY/ \overline{BY} . The $\overline{\text{Data}}$ Polling and Toggle Bit must be performed at the memory location which is being programmed.

The automatic programming operation is completed when the data on DQ₇ is equivalent to data written to this bit at which time the device returns to the read mode and addresses are no longer latched (see “Hardware Sequence Flags Table” in “**COMMAND DEFINITION**”). Therefore, the device requires that a valid address to the device be supplied by the system in this particular instance. Hence, $\overline{\text{Data}}$ Polling must be performed at the memory location which is being programmed.

If hardware reset occurs during the programming operation, the data being written is not guaranteed.

Programming is allowed in any sequence and across sector boundaries. Beware that a data “0” cannot be programmed back to a “1”. Attempting to do so may either hang up the device or result in an apparent success according to the data polling algorithm but a read from Read/Reset mode will show that the data is still “0”. Only erase operations can convert from “0”s to “1”s.

“Embedded Erase™ Algorithm” in “**FLOW CHART**” illustrates the Embedded Program™ Algorithm using typical command strings and bus operations.

Program Suspend/Resume Command

The Program Suspend command allows the system to interrupt a program operation so that data can be read from any address. Writing the Program Suspend command (B0h) during the Embedded Program operation immediately suspends the programming. The Program Suspend command may also be issued during a programming operation while an erase is suspended. The bank addresses of sector being programmed should be set when writing the Program Suspend command.

When the Program Suspend command is written during a programming process, the device halts the program operation within 1 μ s and updates the status bits.

After the program operation has been suspended, the system can read data from any address. The data at program-suspended address is not valid. Normal read timing and command definitions apply.

After the Program Resume command (30h) is written, the device reverts to programming. The bank addresses of sectors being suspended should be set when writing the Program Resume command. The system can determine the status of the program operation using the DQ₇ or DQ₆ status bits, just as in the standard program operation. See “Write Operation Status” for more information.

The system may also write the Autoselect command sequence when the device is in the Program Suspend mode. The device allows reading Autoselect codes at the addresses within programming sectors, since the codes are not stored in the memory. When the device exits the Autoselect mode, the device reverts to the Program Suspend mode, and is ready for another valid operation. See “Autoselect Command Sequence” for more information.

The system must write the Program Resume command (address bits are “Bank Address”) to exit from the Program Suspend mode and continue the programming operation. Further writes of the Resume command are ignored. Another Program Suspend command can be written after the device has resumed programming.

Chip Erase Command

Chip erase is a six bus cycle operation. There are two “unlock” write cycles. These are followed by writing the “set-up” command. Two more “unlock” write cycles are then followed by the chip erase command.

Chip erase does not require the user to program the device prior to erase. Upon executing the Embedded Erase Algorithm command sequence, the device will automatically program and verify the entire memory for an all-zero data pattern prior to electrical erase (Preprogram function) . The system is not required to provide any controls or timings during these operations.

The system can determine the status of the erase operation by using DQ_7 ($\overline{\text{Data}}$ Polling) , DQ_6 (Toggle Bit) or $RY/\overline{\text{BY}}$. The chip erase begins on the rising edge of the last $\overline{\text{CE}}$ or $\overline{\text{WE}}$, whichever happens first in the command sequence, and terminates when the data on DQ_7 is “1” (see Write Operation Status section), at which time the device returns to the read mode.

Chip Erase Time; Sector Erase Time \times All sectors + Chip Program Time (Preprogramming)

“Embedded Erase™ Algorithm” in “**■ FLOW CHART**” illustrates the Embedded Erase™ Algorithm using typical command strings and bus operations.

Sector Erase Command

Sector erase is a six bus cycle operation. There are two “unlock” write cycles. These are followed by writing the “set-up” command. Two more “unlock” write cycles are then followed by the Sector Erase command. The sector address (any address location within the desired sector) is latched on the falling edge of $\overline{\text{CE}}$ or $\overline{\text{WE}}$, whichever happens later, while the command (Data = 30h) is latched on the rising edge of $\overline{\text{CE}}$ or $\overline{\text{WE}}$, whichever happens first. After time-out of “ t_{row} ” from the rising edge of the last sector erase command, the sector erase operation begins.

Multiple sectors may be erased concurrently by writing the six bus cycle operations on “MBM29QM12DH Command Definitions Table” in “**■ DEVICE BUS OPERATION**”. This sequence is followed by writes of the Sector Erase command to addresses in other sectors desired to be concurrently erased. The time between writes must be less than “ t_{row} ”. Otherwise, that command will not be accepted and erasure will not start. It is recommended that processor interrupts be disabled during this time to guarantee such a condition. The interrupts can reoccur after the last Sector Erase command is written. A time-out of “ t_{row} ” from the rising edge of last $\overline{\text{CE}}$ or $\overline{\text{WE}}$, whichever happens first, will initiate the execution of the Sector Erase command (s) . If another falling edge of $\overline{\text{CE}}$ or $\overline{\text{WE}}$, whichever happens first occurs within the “ t_{row} ” time-out window, the timer is reset (monitor DQ_3 to determine if the sector erase timer window is still open, see section DQ_3 , Sector Erase Timer). Resetting the device once execution has begun will corrupt the data in the sector. In that case, restart the erase on those sectors and allow them to complete (refer to Write Operation Status section for Sector Erase Timer operation). Loading the sector erase buffer may be done in any sequence and with any number of sectors.

Sector erase does not require the user to program the device before erase. The device automatically programs all memory locations in the sector (s) to be erased prior to electrical erase (Preprogram function) . When erasing a sector, the rest remain unaffected. The system is not required to provide any controls or timings during these operations.

The system can determine the status of the erase operation by using DQ_7 ($\overline{\text{Data}}$ Polling) , DQ_6 (Toggle Bit) or $RY/\overline{\text{BY}}$.

The sector erase begins after the “ t_{row} ” time-out from the rising edge of $\overline{\text{CE}}$ or $\overline{\text{WE}}$, whichever happens first, for the last sector erase command pulse and terminates when the data on DQ_7 is “1” (see Write Operation Status section), at which time the device returns to the read mode. Data polling and Toggle Bit must be performed at an address within any of the sectors being erased.

Multiple Sector Erase Time = [Sector Erase Time + Sector Program Time (Preprogramming)] \times Number of Sector Erase

In case of multiple sector erase across bank boundaries, a read from the bank (read-while-erase) to which sectors being erased belong cannot be performed.

“Embedded Erase™ Algorithm” in “**■ FLOW CHART**” illustrates the Embedded Erase™ Algorithm using typical command strings and bus operations.

Erase Suspend/Resume Command

The Erase Suspend command allows the user to interrupt Sector Erase operation and then reads data from or programs to a sector not being erased. This command is applicable ONLY during the Sector Erase operation which includes the time-out period for sector erase. Writing the Erase Suspend command (B0h) during the Sector Erase time-out results in immediate termination of the time-out period and suspension of the erase operation.

Writing the Erase Resume command (30h) resumes the erase operation. The bank address of sector being erased or erase-suspended should be set when writing the Erase Suspend or Erase Resume command.

When the Erase Suspend command is written during the Sector Erase operation, the device takes a maximum of t_{SPD} to suspend the erase operation. When the device has entered the erase-suspended mode, the $R\bar{Y}/\bar{B}\bar{Y}$ output pin will be at High-Z and the DQ_7 bit will be at logic "1", and DQ_6 will stop toggling. The user must use the address of the erasing sector for reading DQ_6 and DQ_7 to determine if the erase operation has been suspended. Further writes of the Erase Suspend command are ignored.

When the erase operation has been suspended, the device defaults to the erase-suspend-read mode. Reading data in this mode is the same as reading from the standard read mode, except that the data must be read from sectors that have not been erase-suspended. Reading successively from the erase-suspended sector while the device is in the erase-suspend-read mode will cause DQ_2 to toggle (see the section on DQ_2).

After entering the erase-suspend-read mode, the user can program the device by writing the appropriate command sequence for Program. This program mode is known as the erase-suspend-program mode. Again, it is the same as programming in the regular Program mode, except that the data must be programmed to sectors that are not erase-suspended. Reading successively from the erase-suspended sector while the device is in the erase-suspend-program mode will cause DQ_2 to toggle. The end of the erase-suspended Program operation is detected by the $R\bar{Y}/\bar{B}\bar{Y}$ output pin, Data polling of DQ_7 or by the Toggle Bit I (DQ_6), which is the same as the regular Program operation. Note that DQ_7 must be read from the Program address while DQ_6 can be read from any address within bank being erase-suspended.

To resume the operation of Sector Erase, the Resume command (30h) should be written to the bank being erase suspended. Any further writes of the Resume command at this point will be ignored. Another Erase Suspend command can be written after the chip has resumed erasing.

Extended Command

(1) Fast Mode

The device has a Fast Mode function. It dispenses with the initial two unlock cycles required in the standard program command sequence by writing the Fast Mode command into the command register. In this mode, the required bus cycle for programming consists of two bus cycles instead of four in standard program command. During the Fast mode, do not write any commands other than the Fast program/Fast mode reset command. The read operation is also executed after exiting from the fast mode. To exit from this mode, it is necessary to write Fast Mode Reset command into the command register. The first cycle must contain the bank address (see "Embedded Program Algorithm for Fast Mode" in "■ FLOW CHART"). The V_{CC} active current is required even if $\bar{C}\bar{E} = V_{IH}$ during Fast Mode.

(2) Fast Programming

During the Fast Mode, programming can be executed with two bus cycle operation. The Embedded Program Algorithm is executed by writing program set-up command (A0h) and data write cycles (PA/PD) (see "Embedded Program Algorithm for Fast Mode" in "■ FLOW CHART").

(3) CFI (Common Flash Memory Interface)

The CFI (Common Flash Memory Interface) specification outlines device and the host system software interrogation handshake, which allows specific vendor-specified software algorithms to be used for entire families of devices. This allows device-independent, JEDEC ID-independent and forward-and backward-compatible software support for the specified flash device families. Refer to CFI specification in detail.

The operation is initiated by writing the query command (98h) into the command register. The bank address should be set when writing this command. Then the device information can be read from the bank, and data from the memory cell can be read from the another bank. The higher order address (A_{22} , A_{21} , A_{20}) required for reading out the CFI Codes requires that the bank address (BA) be set at the write cycle. Following the command write, a read cycle from specific address retrieves device information. Please note that output data of upper byte (DQ_{15} to DQ_8) is "0". Refer to CFI code table ("Common Flash Memory Interface Code Table") in "■ FLEXIBLE

SECTOR-ERASE ARCHITECTURE". To terminate operation, it is necessary to write the read/reset command sequence into the register.

HiddenROM Entry Command

The device has a HiddenROM area with One Time Protect function. This area is to enter the security code and to enable the change of the code once set. Programming is allowed in this area until it is protected. However, once it gets protected, it is impossible to unprotect. Therefore, extreme caution is required.

The HiddenROM area is 128 words (64 words for factory and 64 words for customer). This area is normally the "outermost" 4 Kwords boot block area. Therefore, write the HiddenROM entry command sequence to enter the HiddenROM area. It is called HiddenROM mode when the HiddenROM area appears.

Sectors other than the boot block area (SA0) can be read during HiddenROM mode. Read/program of the HiddenROM area is possible during HiddenROM mode. Write the HiddenROM reset command sequence to exit the HiddenROM mode. The bank address of the HiddenROM should be set on the third cycle of this reset command sequence.

In HiddenROM mode, the simultaneous operation cannot be executed multi-function mode between the HiddenROM area and the Bank A.

The following commands are unavailable when the HiddenROM is enabled. Issuing the following commands while the HiddenROM is enabled results in the command being ignored.

1. CFI
2. Set to Fast Mode
3. Fast Program
4. Reset from Fast Mode
5. Program and Sector Erase Suspend
6. Program and Sector Erase Resume

The HiddenROM Entry command is allowed when the device is in either program or erase suspend modes. If the HiddenROM is enabled, the program or erase suspend command is ignored. This prevents resuming either programming or erasure on the HiddenROM if the overlaid sector was undergoing programming or erasure. It is the responsibility of the software to resume the program or erasure of a suspended program or erase after exiting the HiddenROM.

HiddenROM Program Command

To program the data to the HiddenROM area, write the HiddenROM program command sequence during HiddenROM mode. This command is the same as the program command in usual except to write the command during HiddenROM mode. Therefore the detection of completion method is the same as in the past, using the DQ₇ data polling, and DQ₆ toggle bit. Need to pay attention to the address to be programmed. If the address other than the HiddenROM area is selected to program, data of the address will be changed.

HiddenROM Protect Command

The method to protect the HiddenROM is to apply high voltage (V_{ID}) to A₉ and \overline{OE} , set the sector address in the HiddenROM area and (A₇, A₆, A₅, A₄, A₃, A₂, A₁, A₀) = (0, 0, 0, 1, 1, 0, 1, 0), and apply the write pulse during the HiddenROM mode. To verify the protect circuit, apply high voltage (V_{ID}) to A₉, specify (A₇, A₆, A₅, A₄, A₃, A₂, A₁, A₀) = (0, 0, 0, 1, 1, 0, 1, 0) and the sector address in the HiddenROM area, and read. When "1" appears on DQ₀, the protect setting is completed. "0" will appear on DQ₀ if it is not protected. Please apply write pulse again.

And the device has also HiddenROM protect command without V_{ID}. See "MBM29QM12DH Command Definitions Table" in "■ DEVICE BUS OPERATION".

Other sector will be effected if the address other than those for HiddenROM area is selected for the sector address, so please be careful. Once it is protected, protection can not be cancelled, so please pay the closest attention.

Password Program Command

The Password Program Command permits programming the password that is used as part of the hardware protection scheme. The actual password is 64-bits long. 4 Password Program commands are required to program the password. The user must enter the unlock cycle, password program command (38h) and the program address/data for each portion of the password when programming. There are no provisions for entering the 2-cycle unlock cycle, the password program command, and all the password data. There is no special addressing order required for programming the password. Also, when the password is undergoing programming, Simultaneous Operation is disabled. Read operations to any memory location will return the programming status. Once the Password is written and verified, the Password Mode Locking Bit must be set in order to prevent verification. The Password Program Command is only capable of programming "0"s. Programming a "1" after a cell is programmed as a "0" results in a time-out by the Embedded Program Algorithm with the cell remaining as a "0". The password is all F's when shipped from the factory. All 64-bit password combinations are valid as a password. Writing the HiddenROM Exit command returns the device back to normal operation.

Password Verify Command

The Password Verify Command is used to verify the Password. The Password is verifiable only when the Password Mode Locking Bit is not programmed. If the Password Mode Locking Bit is programmed and the user attempts to verify the Password, the device will always drive all F's onto the DQ data bus.

Also, the device will not operate in Simultaneous Operation when the Password Verify command is executed. Only the password is returned regardless of the bank address. The lower two address bits ($A_1:A_0$) are valid during the Password Verify. Writing the HiddenROM Exit command returns the device back to normal operation.

Password Protection Mode Locking Bit Program Command

The Password Protection Mode Locking Bit Program Command programs the Password Protection Mode Locking Bit, which prevents further verifies or updates to the Password. Once programmed, the Password Protection Mode Locking Bit cannot be erased. Once the Password Protection Mode Locking Bit is programmed, the Persistent Sector Protection Locking Bit program circuitry is disabled, thereby forcing the device to remain in the Password Protection mode. After issuing "PL/68h" at 4th bus cycle, the device requires approximately 150 μ s time out period for programming the Password Protection Mode Locking Bit. Then by writing "PL/48h" at 5th bus cycle, the device outputs verify data at DQ_0 . If $DQ_0 = 1$ then Password Protection Mode Locking Bit is programmed. If not, then the user needs to repeat this program sequence from the 4th cycle of "PL/68h". Exiting the Password Protection Mode Locking Bit Program command is accomplished by writing the HiddenROM Exit command.

Persistent Sector Protection Mode Locking Bit Program Command

The Persistent Sector Protection Mode Locking Bit Program Command programs the Persistent Sector Protection Mode Locking Bit, which prevents the Password Mode Locking Bit from ever being programmed. By disabling the program circuitry of the Password Mode Locking Bit, the device is forced to remain in the Persistent Sector Protection mode of operation, once this bit is set. After issuing "SPML/68h" at 4th bus cycle, the device requires approximately 150 μ s time out period for programming the Persistent Protection Mode Locking Bit. Then by writing "SPML/48h" at 5th bus cycle, the device outputs verify data at DQ_0 . If $DQ_0 = 1$ then Persistent Protection Mode Locking Bit is programmed. If not, then the user needs to repeat this program sequence from the 4th cycle of "SPML/68h". Exiting the Persistent Protection Mode Locking Bit Program command is accomplished by writing the HiddenROM Exit command.

PPB Lock Bit Set Command

The PPB Lock Bit Set command is used to set the PPB Lock bit if it is cleared either at reset or if the Password Unlock command was successfully executed. There is no PPB Lock Bit Clear command. Once the PPB Lock Bit is set, it cannot be cleared unless the device is taken through a power-on clear or the Password Unlock command is executed. If the Password Mode Locking Bit is set, the PPB Lock Bit status is reflected as set, even after a power-on reset cycle. Exiting the PPB Lock Bit Set command is accomplished by writing the HiddenROM Exit command.

DPB Write(Erase) Command

The DPB Write command is used to set or clear a DPB for a given sector. The high order address bits (A_{22} to A_{12}) are issued at the same time as the code 01h or 00h on DQ_7 to DQ_0 . All other DQ data bus pins are ignored during the data write cycle. The DPBs are modifiable at any time, regardless of the state of the PPB or PPB Lock Bit. The DPBs are cleared at power-up or hardware reset. Exiting the DPB Write command is accomplished by writing the HiddenROM Exit command.

DPB verify command

DPB verify command is used to verify the status of a DPB for given sector. Scanning the sector addresses (SA) will produce a logical "1" at the device output DQ_0 for a protected sector. Otherwise the device will produce "0" at DQ_0 for the sector which is not protected. Writing the HiddenROM Exit Command returns the device back to normal operation.

PPB Lock Bit verify command

PPB Lock Bit verify command is used to verify the status of a PPB Lock Bit. A logical "1" at the device output DQ_1 indicates that the PPB Lock Bit is set. If PPB Lock Bit is not set, DQ_1 will output "0". Writing the HiddenROM Exit Command returns the device back to normal operation.

Password Unlock Command

The Password Unlock command is used to clear the PPB Lock Bit so that the PPBs can be unlocked for modification, thereby allowing the PPBs to become accessible for modification. The exact password must be entered in order for the unlocking function to occur. This command cannot be issued any faster than $2\ \mu\text{s}$ at a time to prevent a hacker from running through the all 64-bit combinations in an attempt to correctly match a password. If the command is issued before the $2\ \mu\text{s}$ execution window for each portion of the unlock, the command will be ignored.

The Password Unlock function is accomplished by writing Password Unlock command and data to the device to perform the clearing of the PPB Lock Bit. A_0 and A_1 are used to determine the 16 bit data quantity is used to match separated 16 bits. Writing the Password Unlock command is address order specific. In other words, the lowers address $A_1:A_0 = 00$, the next cycle command is to $A_1:A_0 = 01$, then to $A_1:A_0 = 10$, and finally to $A_1:A_0 = 11$. Writing out of sequence results in the Password Unlock not returning a match with the password and the PPB Lock Bit remains set.

Once the Password Unlock command is entered, the $\overline{RY/\overline{BY}}$ pin goes LOW indicating that the device is busy. Also, reading the Bank A results in the DQ_6 pin toggling, indicating that the Password Unlock function is in progress. Reading the other bank returns actual array data. Approximately $2\ \mu\text{s}$ is required for each portion of the unlock. Once the first portion of the password unlock completes ($\overline{RY/\overline{BY}}$ is not driven and DQ_6 does not toggle when read), the next cycle is issued, only this time with the next part of the password. Seven cycles Password Unlock commands are required to successfully clear the PPB Lock Bit. As with the first Password Unlock command, the $\overline{RY/\overline{BY}}$ signal goes LOW and reading the device results in the DQ_6 pin toggling on successive read operations until complete. It is the responsibility of the microprocessor to keep track of the number of Password Unlock cycles, the order, and when to read the PPB Lock bit to confirm successful password unlock. Writing the HiddenROM Exit Command returns the device back to normal operation.

PPB Program Command

The PPB Program command is used to program, or set, a given PPB. Each PPB is individually programmed (but is bulk erased with the other PPBs). The specific sector address (A_{22} to A_{12}) are written at the same time as the program command 60h. If the PPB Lock Bit is set and the corresponding PPB is set for the sector, the PPB Program command will not execute and the command will time-out without programming the PPB. After issuing "SGA + WP/68h" at 4th bus cycle, the device requires approximately $150\ \mu\text{s}$ time out period for programming the PPB. Then by writing "SGA + WP/48h" at 5th bus cycle, the device outputs verify data at DQ_0 . If $DQ_0 = 1$ then PPB is programmed. If not, then the user needs to repeat this program sequence from the 4th cycle of "SGA + WP/68h".

The PPB Program command does not follow the Embedded Program algorithm. Writing the HiddenROM Exit Command returns the device back to normal operation.

All PPB Erase Command

The All PPB Erase command is used to erase all PPBs in bulk. There is no means for individually erasing a specific PPB. Unlike the PPB program, no specific sector address is required. However, when the PPB erase command is written (60h), all Sector PPBs are erased in parallel. If the PPB Lock Bit is set the ALL PPB Erase command will not execute and the command will time-out without erasing the PPBs. After issuing "WP/60h" at 4th bus cycle, the device requires approximately 1.5 ms time out period for programming the PPB. Then by writing "SGA + WP/40h" at 5th bus cycle, the device outputs verify data at DQ₀. If DQ₀ = 0 then PPB is successfully erased. If not, then the user needs to repeat this program sequence from the 4th cycle of "WP/60h".

It is the responsibility of the user to preprogram all PPBs prior to issuing the All PPB Erase command. If the user attempts to erase a cleared PPB, over-erasure may occur making it difficult to program the PPB at a later time. Also note that the total number of PPB program/erase cycles is limited to 100 cycles. Cycling the PPBs beyond 100 cycles is not guaranteed. Writing the HiddenROM Exit Command returns the device back to normal operation.

Write Operation Status

Detailed in "Hardware Sequence Flags Table" in "■ COMMAND DEFINITION" are all the status flags which can determine the status of the bank for the current mode operation. The read operation from the bank which doesn't operate Embedded Algorithm returns data of memory cells. These bits offer a method for determining whether an Embedded Algorithm is properly completed. The information on DQ₂ is address-sensitive. This means that if an address from an erasing sector is consecutively read, the DQ₂ bit will toggle. However, DQ₂ will not toggle if an address from a non-erasing sector is consecutively read. This allows users to determine which sectors are in erase and which are not.

The status flag is not output from banks (non-busy banks) which do not execute Embedded Algorithms. For example, a bank (busy bank) is executing an Embedded Algorithm. When the read sequence is [1] < busy bank >, [2] < non-busy bank >, [3] < busy bank >, the DQ₆ toggles in the case of [1] and [3]. In case of [2], the data of memory cells are output. In the erase-suspend read mode with the same read sequence, DQ₆ will not be toggled in [1] and [3].

In the erase suspend read mode, DQ₂ is toggled in [1] and [3]. In case of [2], the data of memory cell is output.

Hardware Sequence Flags Table

Status		DQ ₇	DQ ₆	DQ ₅	DQ ₃	DQ ₂	
In Progress	Embedded Program Algorithm	\overline{DQ}_7	Toggle	0	0	1	
	Embedded Erase Algorithm	0	Toggle	0	1	Toggle* ¹	
	Program Suspended Mode	Program Suspend Read (Program Suspended Sector)	Data	Data	Data	Data	Data
		Program Suspend Read (Non-Program Suspended Sector)	Data	Data	Data	Data	Data
	Erase Suspended Mode	Erase Suspend Read (Erase Suspended Sector)	1	1	0	0	Toggle
		Erase Suspend Read (Non-Erase Suspended Sector)	Data	Data	Data	Data	Data
Erase Suspend Program (Non-Erase Suspended Sector)		\overline{DQ}_7	Toggle	0	0	1* ²	
Exceeded Time Limits	Embedded Program Algorithm	\overline{DQ}_7	Toggle	1	0	1	
	Embedded Erase Algorithm	0	Toggle	1	1	N/A	
	Erase Suspended Mode	Erase Suspend Program (Non-Erase Suspended Sector)	\overline{DQ}_7	Toggle	1	0	N/A

*1 : Successive reads from the erasing or erase-suspend sector will cause DQ₂ to toggle.

*2 : Reading from non-erase suspend sector address will indicate logic "1" at the DQ₂ bit.

DQ₇

Data Polling

The device features $\overline{\text{Data}}$ Polling as a method to indicate to the host that the Embedded Algorithms are in progress or completed. During the Embedded Program Algorithm, an attempt to read the device will produce a complement of data last written to DQ₇. Upon completion of the Embedded Program Algorithm, an attempt to read the device will produce true data last written to DQ₇. For programming, the $\overline{\text{Data}}$ Polling is valid after the rising edge of the fourth write pulse in the four write pulse sequences. During the Embedded Erase Algorithm, an attempt to read the device will produce a “0” at the DQ₇ output. Upon completion of the Embedded Erase Algorithm, an attempt to read device will produce a “1” on DQ₇. The flowchart for $\overline{\text{Data}}$ Polling (DQ₇) is shown in “Temporary Sector Group Unprotection Algorithm” in “■ FLOW CHART”.

$\overline{\text{Data}}$ polling will also flag the entry into Erase Suspend. DQ₇ will switch “0” to “1” at the start of the Erase Suspend mode. Please note that the address of an erasing sector must be applied in order to observe DQ₇ in the Erase Suspend Mode.

For chip erase and sector erase, the $\overline{\text{Data}}$ Polling is valid after the rising edge of the sixth write pulse in the six write pulse sequences. $\overline{\text{Data}}$ Polling must be performed at sector addresses of sectors being erased, not protected sectors. Otherwise the status may become invalid.

If a program address falls within a protected sector, $\overline{\text{Data}}$ Polling on DQ₇ is active for approximately 1 μs , then that bank returns to the read mode. After an erase command sequence is written, if all sectors selected for erasing are protected, $\overline{\text{Data}}$ Polling on DQ₇ is active for approximately 400 μs , then the bank returns to read mode.

Once the Embedded Algorithm operation is close to being completed, the device data pins (DQ₇) may change asynchronously while the output enable ($\overline{\text{OE}}$) is asserted low. This means that device is driving status information on DQ₇ at one instant, and then that byte’s valid data at the next instant. Depending on when the system samples the DQ₇ output, it may read the status or valid data. Even if device has completed the Embedded Algorithm operation and DQ₇ has a valid data, data outputs on DQ₀ to DQ₆ may still be invalid. The valid data on DQ₀ to DQ₇ will be read on successive read attempts.

The $\overline{\text{Data}}$ Polling feature is active only during the Embedded Programming Algorithm, Embedded Erase Algorithm or sector erase time-out. (See “Hardware Sequence Flags Table” in “■ COMMAND DEFINITION”.)

See “Data Polling during Embedded Algorithm Operation Timing Diagram” in “■ TIMING DIAGRAM” for the $\overline{\text{Data}}$ Polling timing specifications and diagrams.

DQ₆

Toggle Bit I

The device also features the “Toggle Bit I” as a method to indicate to the host system that the Embedded Algorithms are in progress or completed.

During Embedded Program or Erase Algorithm cycle, successive attempts to read ($\overline{\text{OE}}$ toggling) data from the busy bank will result in DQ₆ toggling between one and zero. Once the Embedded Program or Erase Algorithm cycle is completed, DQ₆ will stop toggling and valid data will be read on the next successive attempts. During programming, the Toggle Bit I is valid after the rising edge of the fourth write pulse in the four write pulse sequences. For chip erase and sector erase, the Toggle Bit I is valid after the rising edge of the sixth write pulse in the six write pulse sequences. The Toggle Bit I is active during the sector time out.

In programming, if the sector being written is protected, the toggle bit will toggle for about 1 μs and then stop toggling with data unchanged. In erase, the device will erase all selected sectors except for protected ones. If all selected sectors are protected, the chip will toggle the toggle bit for about 400 μs and then drop back into read mode, having data kept remained.

Either $\overline{\text{CE}}$ or $\overline{\text{OE}}$ toggling will cause DQ₆ to toggle. In addition, an Erase Suspend/Resume command will cause DQ₆ to toggle.

The system can use DQ₆ to determine whether a sector is actively erased or is erase-suspended. When a bank is actively erased (that is, the Embedded Erase Algorithm is in progress), DQ₆ toggles. When a bank enters the Erase Suspend mode, DQ₆ stops toggling. Successive read cycles during erase-suspend-program cause DQ₆ to toggle.

To operate toggle bit function properly, \overline{CE} or \overline{OE} must be high when bank address is changed.

See “ \overline{Data} Polling during Embedded Algorithm Operation Timing Diagram” in “**■ TIMING DIAGRAM**” for the Toggle Bit I timing specifications and diagrams.

DQ₅

Exceeded Timing Limits

DQ₅ will indicate if the program or erase time has exceeded the specified limits (internal pulse count) . Under these conditions DQ₅ will produce “1”. This is a failure condition indicating that the program or erase cycle was not successfully completed. \overline{Data} Polling is only operating function of the device under this condition. The \overline{CE} circuit will partially power down device under these conditions (to approximately 2 mA) . The \overline{OE} and \overline{WE} pins will control the output disable functions as described in “MBM29QM12DH User Bus Operations Table” in “**■ DEVICE BUS OPERATION**”.

The DQ₅ failure condition may also appear if a user tries to program a non-blank location without pre-erase. In this case the device locks out and never completes the Embedded Algorithm operation. Hence, the system never reads valid data on DQ₇ bit and DQ₆ never stop toggling. Once the device has exceeded timing limits, the DQ₅ bit will indicate a “1.” Please note that this is not a device failure condition since the device was incorrectly used. If this occurs, reset device with the command sequence.

DQ₃

Sector Erase Timer

After completion of the initial sector erase command sequence, sector erase time-out begins. DQ₃ will remain low until the time-out is completed. \overline{Data} Polling and Toggle Bit are valid after the initial sector erase command sequence.

If \overline{Data} Polling or the Toggle Bit I indicates that a valid erase command has been written, DQ₃ may be used to determine whether the sector erase timer window is still open. If DQ₃ is high (“1”) the internally controlled erase cycle has begun. If DQ₃ is low (“0”) , the device will accept additional sector erase commands. To insure the command has been accepted, the system software should check the status of DQ₃ prior to and following each subsequent Sector Erase command. If DQ₃ were high on the second status check, the command may not have been accepted.

See “Hardware Sequence Flags Table” in “**■ COMMAND DEFINITION**” : Hardware Sequence Flags.

DQ₂

Toggle Bit II

This toggle bit II, along with DQ₆, can be used to determine whether the device is in the Embedded Erase Algorithm or in Erase Suspend.

Successive reads from the erasing sector will cause DQ₂ to toggle during the Embedded Erase Algorithm. If the device is in the erase-suspended-read mode, successive reads from the erase-suspended sector will cause DQ₂ to toggle. When the device is in the erase-suspended-program mode, successive reads from the non-erase suspended sector will indicate a logic “1” at the DQ₂ bit.

DQ₆ is different from DQ₂ in that DQ₆ toggles only when the standard program or Erase, or Erase Suspend Program operation is in progress. The behavior of these two status bits, along with that of DQ₇, is summarized as follows :

For example, DQ₂ and DQ₆ can be used together to determine if the erase-suspend-read mode is in progress. (DQ₂ toggles while DQ₆ does not.) See also “Toggle Bit Status Table” in “**■ COMMAND DEFINITION**” and “DQ₂ vs. DQ₆” in “**■ TIMING DIAGRAM**”.

Furthermore DQ₂ can also be used to determine which sector is being erased. At the erase mode, DQ₂ toggles if this bit is read from an erasing sector.

To operate toggle bit function properly, \overline{CE} or \overline{OE} must be high when bank address is changed.

Reading Toggle Bits 3DQ₆/DQ₂

Whenever the system initially begins reading toggle bit status, it must read DQ₇ to DQ₀ at least twice in a row to determine whether a toggle bit is toggling. Typically a system would note and store the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the first. If the toggle bit is not toggling, the device has completed the program or erase operation. The system can read array data on DQ₇ to DQ₀ on the following read cycle.

However, if, after the initial two read cycles, the system determines that the toggle bit is still toggling, the system also should note whether the value of DQ₅ is high (see the section on DQ₅). If it is, the system should then determine again whether the toggle bit is toggling, since the toggle bit may have stopped toggling just as DQ₅ went high. If the toggle bit is no longer toggling, the device has successfully completed the program or erase operation. If it is still toggling, the device did not complete the operation successfully, and the system must write the reset command to return to reading array data.

The remaining scenario is that the system initially determines that the toggle bit is toggling and DQ₅ has not gone high. The system may continue to monitor the toggle bit and DQ₅ through successive read cycles, determining the status as described in the previous paragraph. Alternatively, it may choose to perform other system tasks. In this case, the system must start at the beginning of the algorithm when it returns to determine the status of the operation. (Refer to “Toggle Bit Algorithm” in “■ FLOW CHART”.)

Toggle Bit Status Table

Mode	DQ ₇	DQ ₆	DQ ₂
Program	$\overline{DQ_7}$	Toggle	1
Erase	0	Toggle	Toggle*
Erase-Suspend Read (Erase-Suspended Sector)	1	1	Toggle
Erase-Suspend Program	$\overline{DQ_7}$	Toggle	1*

* : Successive reads from the erasing or erase-suspend sector will cause DQ₂ to toggle. Reading from the non erase suspend sector address will indicate logic “1” at the DQ₂ bit.

RY/ \overline{BY}

Ready/Busy

The device provides a RY/ \overline{BY} open-drain output pin as a way to indicate to the host system that Embedded Algorithms are either in progress or have been completed. If output is low, the device is busy with either a program or erase operation. If output is high, the device is ready to accept any read/write or erase operation. If the device is placed in an Erase Suspend mode, RY/ \overline{BY} output will be high.

During programming, the RY/ \overline{BY} pin is driven low after the rising edge of the fourth write pulse. During an erase operation, the RY/ \overline{BY} pin is driven low after the rising edge of the sixth write pulse. The RY/ \overline{BY} pin will indicate a busy condition during \overline{RESET} pulse. Refer to “RY/ \overline{BY} Timing Diagram during Program/Erase Operation Timing Diagram” in “■ TIMING DIAGRAM” and “ \overline{RESET} , RY/ \overline{BY} Timing Diagram” in “■ TIMING DIAGRAM” for a detailed timing diagram. The RY/ \overline{BY} pin is pulled high in standby mode.

Since this is an open-drain output, RY/ \overline{BY} pins can be tied together in parallel with a pull-up resistor to V_{CC}.

Data Protection

The device is designed to offer protection against accidental erasure or programming caused by spurious system level signals that may exist during power transitions. During power-up, the device automatically resets the internal state machine in Read mode. Also, with its control register architecture, alteration of memory contents only occurs after successful completion of specific multi-bus cycle command sequences.

The device also incorporates several features to prevent inadvertent write cycles resulting from V_{CC} power-up and power-down transitions or system noise.

Low V_{CC} Write Inhibit

To avoid initiation of a write cycle during V_{CC} power-up and power-down, a write cycle is locked out for V_{CC} less than V_{LKO} (Min) . If $V_{CC} < V_{LKO}$, the command register is disabled and all internal program/erase circuits are disabled. Under this condition, the device will reset to the read mode. Subsequent writes will be ignored until the V_{CC} level is greater than V_{LKO} . It is the user's responsibility to ensure that the control pins are logically correct to prevent unintentional writes when V_{CC} is above V_{LKO} (Min) .

If the Embedded Erase Algorithm is interrupted, the intervened erasing sector (s) is (are) not valid.

Write Pulse “Glitch” Protection

Noise pulses of less than 3 ns (typical) on \overline{OE} , \overline{CE} or \overline{WE} will not initiate a write cycle.

Logical Inhibit

Writing is inhibited by holding any one of $\overline{OE} = V_{IL}$, $\overline{CE} = V_{IH}$ or $\overline{WE} = V_{IH}$. To initiate a write cycle \overline{CE} and \overline{WE} must be a logical zero while \overline{OE} is a logical one.

Power-Up Write Inhibit

Power-up of the device with $\overline{WE} = \overline{CE} = V_{IL}$ and $\overline{OE} = V_{IH}$ will not accept commands on the rising edge of \overline{WE} . The internal state machine is automatically reset to the read mode on power-up.

MBM29QM12DH-60

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min	Max	
Storage Temperature	T _{stg}	-55	+125	°C
Ambient Temperature with Power Applied	T _A	-40	+85	°C
Voltage with Respect to Ground All pins except A ₉ , $\overline{\text{OE}}$, and $\overline{\text{RESET}}$ *1,*2	V _{IN} , V _{OUT}	-0.5	V _{CC} +0.5	V
Power Supply Voltage *1	V _{CC}	-0.5	+4.0	V
A ₉ , $\overline{\text{OE}}$, and $\overline{\text{RESET}}$ *1,*3	V _{IN}	-0.5	+13.0	V
$\overline{\text{WP/ACC}}$ *1,*4	V _{ACC}	-0.5	+10.5	V

*1 : Voltage is defined on the basis of V_{SS} = GND = 0 V.

*2 : Minimum DC voltage on input or I/O pins is -0.5 V. During voltage transitions, input or I/O pins may undershoot V_{SS} to -2.0 V for periods of up to 20 ns. Maximum DC voltage on input or I/O pins is V_{CC}+0.5 V. During voltage transitions, input or I/O pins may overshoot to V_{CC}+2.0 V for periods of up to 20 ns.

*3 : Minimum DC input voltage on A₉, $\overline{\text{OE}}$ and $\overline{\text{RESET}}$ pins is -0.5 V. During voltage transitions, A₉, $\overline{\text{OE}}$ and $\overline{\text{RESET}}$ pins may undershoot V_{SS} to -2.0 V for periods of up to 20 ns. Voltage difference between input and supply voltage (V_{IN} - V_{CC}) does not exceed +9.0 V. Maximum DC input voltage on A₉, $\overline{\text{OE}}$ and $\overline{\text{RESET}}$ pins is +13.0 V which may overshoot to +14.0 V for periods of up to 20 ns.

*4 : Minimum DC input voltage on $\overline{\text{WP/ACC}}$ pin is -0.5 V. During voltage transitions, $\overline{\text{WP/ACC}}$ pin may undershoot V_{SS} to -2.0 V for periods of up to 20 ns. Maximum DC input voltage on $\overline{\text{WP/ACC}}$ pin is +10.5 V which may overshoot to +12.0 V for periods of up to 20 ns when V_{CC} is applied.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Part No.	Value		Unit
			Min	Max	
Ambient Temperature	T _A	MBM29QM12DH 60/70	-40	+85	°C
Power Supply Voltage	V _{CC}	MBM29QM12DH 60/70	+2.7	+3.6	V
V _{CCQ} Supply Voltage*	V _{CCQ}	MBM29QM12DH 60	+2.7	+V _{CC}	V
		MBM29QM12DH 70	+1.65	+1.95	V

* : Voltage is defined on the basis of V_{SS} = GND = 0 V.

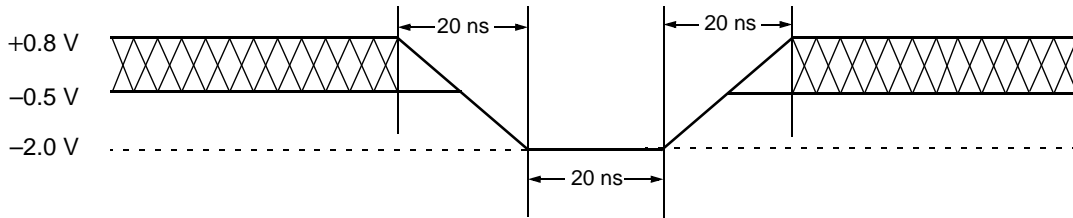
Note : Operating ranges define those limits between which the proper device function is guaranteed.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

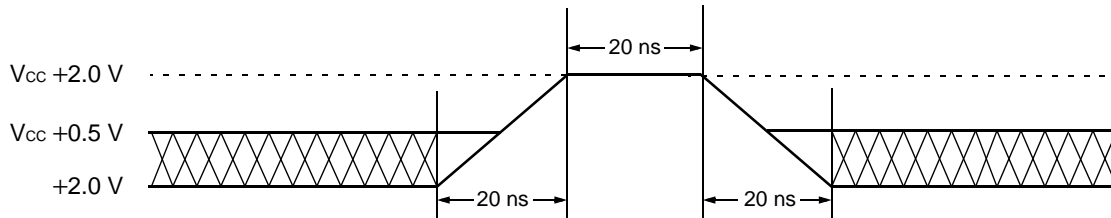
Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

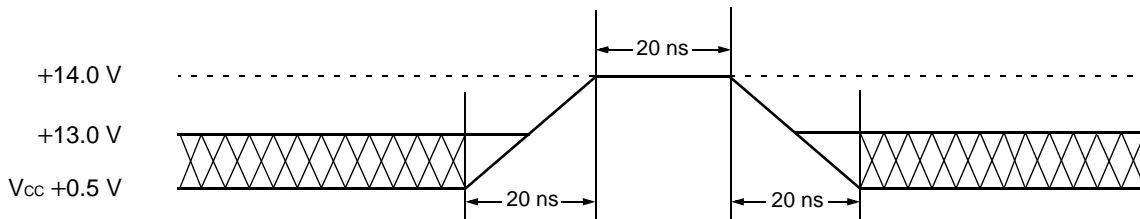
■ MAXIMUM OVERSHOOT/MAXIMUM UNDERSHOOT



Maximum Undershoot Waveform



Maximum Overshoot Waveform 1



Note: This waveform is applicable for A_9 , \overline{OE} , and \overline{RESET} .

Maximum Overshoot Waveform 2

MBM29QM12DH-60

DC CHARACTERISTICS

1. DC Characteristics ($V_{CCQ} = 2.7\text{ V to }3.6\text{ V or }1.65\text{ V to }1.95\text{ V}$)

Parameter	Symbol	Conditions	Value			Unit	
			Min	Typ	Max		
Input Leakage Current	I_{LI}	$V_{IN} = V_{SSQ} \text{ to } V_{CCQ}, V_{CC} = V_{CC} \text{ Max}$	-1.0	—	+1.0	μA	
Output Leakage Current	I_{LO}	$V_{OUT} = V_{SSQ} \text{ to } V_{CCQ}, V_{CC} = V_{CC} \text{ Max}$	-1.0	—	+1.0	μA	
$A_9, \overline{OE}, \overline{RESET}$ Inputs Leakage Current	I_{LIT}	$V_{CC} = V_{CC} \text{ Max},$ $A_9, \overline{OE}, \overline{RESET} = 12.5\text{ V}$	—	—	+35	μA	
\overline{WP}/ACC Accelerated Program Current	I_{LIA}	$V_{CC} = V_{CC} \text{ Max},$ $\overline{WP}/\text{ACC} = V_{ACC} \text{ Max}$	—	—	20	mA	
V_{CC} Active Current *1	I_{CC1}	$\overline{CE} = V_{IL}, \overline{OE} = V_{IH},$ $f = 10\text{ MHz}$	$V_{CC} = 2.7\text{ V to }3.1\text{ V}$	—	—	45	mA
			$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	—	—	60	
		$\overline{CE} = V_{IL}, \overline{OE} = V_{IH},$ $f = 5\text{ MHz}$	$V_{CC} = 2.7\text{ V to }3.1\text{ V}$	—	—	25	mA
			$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	—	—	30	
V_{CC} Active Current *2	I_{CC2}	$\overline{CE} = V_{IL}, \overline{OE} = V_{IH}$	—	—	25	mA	
V_{CC} Current (Standby)	I_{CC3}	$V_{CC} = V_{CC} \text{ Max}, \overline{CE} = V_{CCQ} \pm 0.3\text{ V},$ $\overline{RESET} = V_{CCQ} \pm 0.3\text{ V}, \overline{WP}/\text{ACC} = V_{CCQ} \pm 0.3\text{ V}$	—	1	5	μA	
V_{CC} Current (Standby, Reset)	I_{CC4}	$V_{CC} = V_{CC} \text{ Max}, \overline{RESET} = V_{SSQ} \pm 0.3\text{ V}$	—	1	5	μA	
V_{CC} Power Supply Current (Automatic Sleep Mode) *3	I_{CC5}	$V_{CC} = V_{CC} \text{ Max}, \overline{CE} = V_{SSQ} \pm 0.3\text{ V},$ $\overline{RESET} = V_{CCQ} \pm 0.3\text{ V},$ $V_{IN} = V_{CCQ} \pm 0.3\text{ V or } V_{SSQ} \pm 0.3\text{ V}$	—	1	5	μA	
V_{CC} Active Current *5 (Read-While-Program)	I_{CC6}	$\overline{CE} = V_{IL}, \overline{OE} = V_{IH}$	—	—	45	mA	
V_{CC} Active Current *5 (Read-While-Erase)	I_{CC7}	$\overline{CE} = V_{IL}, \overline{OE} = V_{IH}$	—	—	45	mA	
V_{CC} Active Current (Erase-Suspend-Program)	I_{CC8}	$\overline{CE} = V_{IL}, \overline{OE} = V_{IH}$	—	—	25	mA	
V_{CC} Active Current (Page Mode Read)	I_{CC9}	$\overline{CE} = V_{IL}, \overline{OE} = V_{IH},$ 8 Words Read	$V_{CC} = 2.7\text{ V to }3.1\text{ V}$	—	—	10	mA
			$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	—	—	15	
Input Low Level	V_{IL}	—	-0.5	—	$V_{CCQ} \times 0.3$	V	
Input High Level	V_{IH}	—	$0.7 \times V_{CCQ}$	—	$V_{CCQ} + 0.3$	V	
Voltage for Autoselect and Sector Protection ($A_9, \overline{OE}, \overline{RESET}$) *4	V_{ID}	—	11.5	12	12.5	V	
Voltage for \overline{WP}/ACC Sector Protection/Unprotection and Program Acceleration *4	V_{ACC}	—	8.5	9.0	9.5	V	
Output Low Voltage Level	V_{OL}	$I_{OL} = 100\ \mu\text{A}, V_{CC} = V_{CC} \text{ Min}$	—	—	$0.15 \times V_{CCQ}$	V	
Output High Voltage Level	V_{OH2}	$I_{OH} = -100\ \mu\text{A}$	$0.85 \times V_{CCQ}$	—	—	V	
Low V_{CC} Lock-Out Voltage	V_{LKO}	—	2.3	2.4	2.5	V	

*1: The I_{CC} current listed includes both the DC operating current and the frequency dependent component.

*2: I_{CC} active while Embedded Algorithm (program or erase) is in progress.

*3: Automatic sleep mode enables the low power mode when address remain stable for 150 ns.

*4: Applicable for only V_{CC} .

*5: Embedded Algorithm (program or erase) is in progress. (@5 MHz)

■ AC CHARACTERISTICS

• Read Only Operations Characteristics

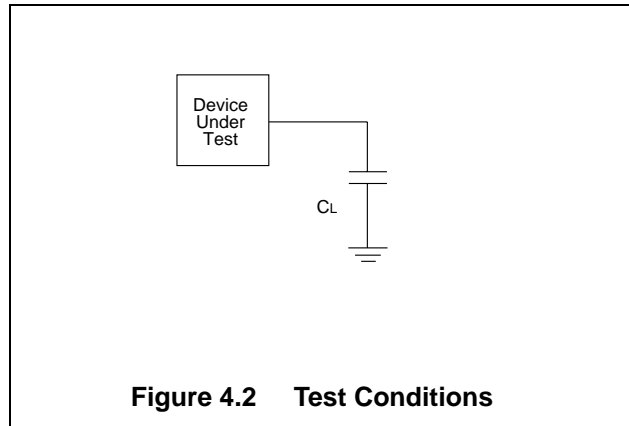
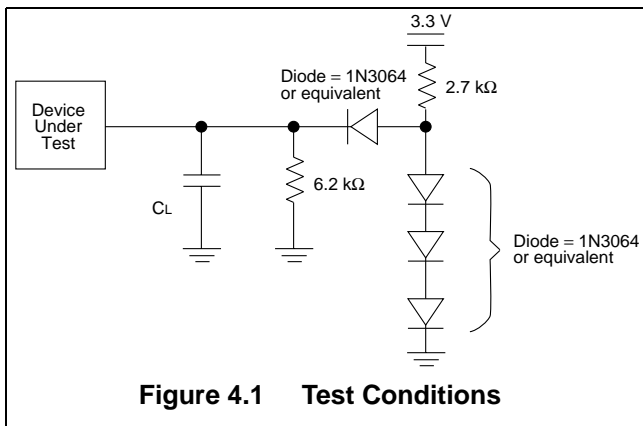
Parameter	Symbol		Test Setup	Value				Unit
	JEDEC	Standard		V _{CCQ} = 2.7 V to 3.6 V *1		V _{CCQ} = 1.65 V to 1.95 V *2		
				Min	Max	Min	Max	
Read Cycle Time	t _{AVAV}	t _{RC}	—	60	—	70	—	ns
Address to Output Delay	t _{AVQV}	t _{ACC}	$\overline{CE} = V_{IL}$ $\overline{OE} = V_{IL}$	—	60	—	70	ns
Page Read Cycle Time	—	t _{PRC}	—	20	—	30	—	ns
Page Address to Output Delay	—	t _{PACC}	$\overline{CE} = V_{IL}$ $\overline{OE} = V_{IL}$	—	20	—	30	ns
Chip Enable to Output Delay	t _{ELQV}	t _{CE}	$\overline{OE} = V_{IL}$	—	60	—	70	ns
Output Enable to Output Delay	t _{GLQV}	t _{OE}	—	—	20	—	30	ns
Chip Enable to Output High-Z	t _{EHQZ}	t _{DF}	—	—	20	—	30	ns
Output Enable to Output High-Z	t _{GHQZ}	t _{DF}	—	—	20	—	30	ns
Output Hold Time From Address, \overline{CE} or \overline{OE} , Whichever Occurs First	t _{AXQX}	t _{OH}	—	5	—	5	—	ns

*1 : Test Conditions:
Output Load:
1 TTL gate and 30 pF (Figure 4.1)

Input rise and fall times: 5 ns
Input pulse levels: 0.0 V or V_{CCQ}
Timing measurement reference level
Input: 0.5 × V_{CCQ}
Output: 0.5 × V_{CCQ}

*2 : Test Conditions:
Output Load:
C_L = 30 pF (Figure 4.2)

Input rise and fall times: 5 ns
Input pulse levels: 0.0 V or V_{CCQ}
Timing measurement reference level
Input: 0.5 × V_{CCQ}
Output: 0.5 × V_{CCQ}



MBM29QM12DH-60

• Write (Erase/Program) Operations

Parameter		Symbol		Value						Unit
				V _{CCQ} = 2.7 V to 3.6 V *1			V _{CCQ} = 1.65 V to 1.95 V *2			
				JEDEC	Standard	Min	Typ	Max	Min	
Write Cycle Time		t _{AVAV}	t _{WC}	60	—	—	70	—	—	ns
Address Setup Time		t _{AVWL}	t _{AS}	0	—	—	0	—	—	ns
Address Setup Time to \overline{OE} Low during Toggle Bit Polling		—	t _{ASO}	15	—	—	15	—	—	ns
Address Hold Time		t _{WLAX}	t _{AH}	30	—	—	35	—	—	ns
Address Hold Time from \overline{CE} or \overline{OE} High during Toggle Bit Polling		—	t _{AHT}	0	—	—	0	—	—	ns
Data Setup Time		t _{DVWH}	t _{DS}	25	—	—	30	—	—	ns
Data Hold Time		t _{WHDX}	t _{DH}	0	—	—	0	—	—	ns
Output Enable Setup Time		—	t _{OES}	0	—	—	0	—	—	ns
Output Enable Hold Time	Read	—	t _{OEH}	0	—	—	0	—	—	ns
	Toggle and Data Polling			10	—	—	10	—	—	ns
Read Recover Time Before Write		t _{GHWL}	t _{GHWL}	0	—	—	0	—	—	ns
Read Recover Time Before Write (OE High to CE Low)		t _{GHEL}	t _{GHEL}	0	—	—	0	—	—	ns
\overline{CE} Setup Time		t _{ELWL}	t _{CS}	0	—	—	0	—	—	ns
\overline{WE} Setup Time		t _{WLEL}	t _{WS}	0	—	—	0	—	—	ns
\overline{CE} Hold Time		t _{WHEH}	t _{CH}	0	—	—	0	—	—	ns
\overline{WE} Hold Time		t _{EHWH}	t _{WH}	0	—	—	0	—	—	ns
Write Pulse Width		t _{WLWH}	t _{WP}	35	—	—	40	—	—	ns
\overline{CE} Pulse Width		t _{ELEH}	t _{CP}	35	—	—	40	—	—	ns
Write Pulse Width High		t _{WHWL}	t _{WPH}	20	—	—	25	—	—	ns
\overline{CE} Pulse Width High		t _{EHEL}	t _{CPH}	20	—	—	25	—	—	ns
Word Programming Operation		t _{WHWH1}	t _{WHWH1}	—	6	—	—	6	—	μs
Sector Erase Operation*1		t _{WHWH2}	t _{WHWH2}	—	0.5	—	—	0.5	—	s
V _{CC} Setup Time		—	t _{VCS}	50	—	—	50	—	—	μs
Rise Time to V _{ID} *2		—	t _{VIDR}	500	—	—	500	—	—	ns
Rise Time to V _{ACC} *3		—	t _{VACCR}	500	—	—	500	—	—	ns
Voltage Transition Time*2		—	t _{VLHT}	4	—	—	4	—	—	μs
Write Pulse Width*2		—	t _{WPP}	100	—	—	100	—	—	μs
\overline{OE} Setup Time to \overline{WE} Active*2		—	t _{OESP}	4	—	—	4	—	—	μs
\overline{CE} Setup Time to \overline{WE} Active*2		—	t _{CSP}	4	—	—	4	—	—	μs

(Continued)

(Continued)

Parameter	Symbol		Value						Unit
			V _{CCQ} = 2.7 V to 3.6 V *1			V _{CCQ} = 1.65 V to 1.95 V *2			
	JEDEC	Standard	Min	Typ	Max	Min	Typ	Max	
Recover Time from RY/ $\overline{\text{BY}}$	—	t _{RB}	0	—	—	0	—	—	ns
$\overline{\text{RESET}}$ Pulse Width	—	t _{RP}	500	—	—	500	—	—	ns
$\overline{\text{RESET}}$ High Level Period Before Read	—	t _{RH}	50	—	—	50	—	—	ns
Program/Erase Valid to RY/ $\overline{\text{BY}}$ Delay	—	t _{BUSY}	—	—	90	—	—	90	ns
Delay Time from Embedded Output Enable	—	t _{EOE}	—	—	60	—	—	70	ns
Sector Erase Time-out Period	—	t _{TOW}	50	—	—	50	—	—	μs
Erase Suspend Transition Time	—	t _{SPD}	—	—	20	—	—	20	μs

*1: This does not include the preprogramming time.

*2: This timing is for Sector Protection operation.

*3: This timing is for Accelerated Program operation.

MBM29QM12DH-60

■ ERASE AND PROGRAMMING PERFORMANCE

Parameter	Limits			Unit	Comments
	Min	Typ	Max		
Sector Erase Time	—	0.5	2	s	Excludes programming time prior to erasure
Word Programming Time	—	6.0	100	μs	Excludes system-level overhead
Chip Programming Time	—	50.3	200	s	Excludes system-level overhead
Erase/Program Cycle	100,000	—	—	cycle	—

Note : Typical Erase conditions $T_A = +25^{\circ}\text{C}$, $V_{CC} = 2.9\text{ V}$
 Typical Program conditions $T_A = +25^{\circ}\text{C}$, $V_{CC} = 2.9\text{ V}$, Data = checker

■ TSOP(1) PIN CAPACITANCE

($T_A = +25^{\circ}\text{C}$, $f = 1.0\text{ MHz}$)






Parameter	Symbol	Test Setup	Value		Unit
			Typ	Max	
Input Pin Capacitance	C_{IN}	$V_{IN} = 0$	7	10	pF
Output Pin Capacitance	C_{OUT}	$V_{OUT} = 0$	8	12	pF
Control Pin Capacitance	C_{IN2}	$V_{IN} = 0$	8	11	pF
Control Pin Capacitance (\overline{WP}/ACC)	C_{IN3}	$V_{IN} = 0$	11	12	pF

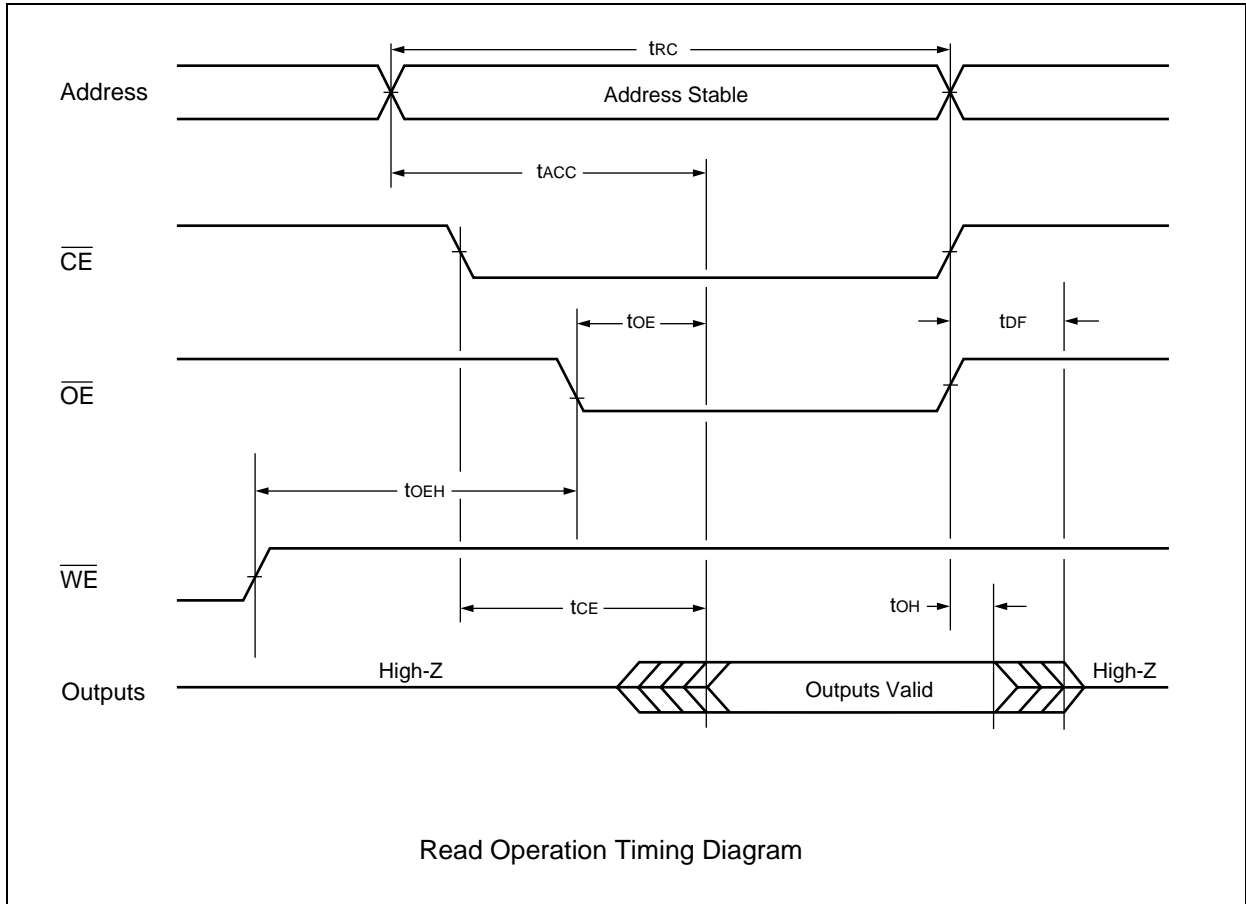
■ FBGA PIN CAPACITANCE

Parameter	Symbol	Test Setup	Value		Unit
			Typ	Max	
Input Pin Capacitance	C_{IN}	$V_{IN} = 0$	7	10	pF
Output Pin Capacitance	C_{OUT}	$V_{OUT} = 0$	8	12	pF
Control Pin Capacitance	C_{IN2}	$V_{IN} = 0$	8	11	pF
Control Pin Capacitance (\overline{WP}/ACC)	C_{IN3}	$V_{IN} = 0$	11	12	pF

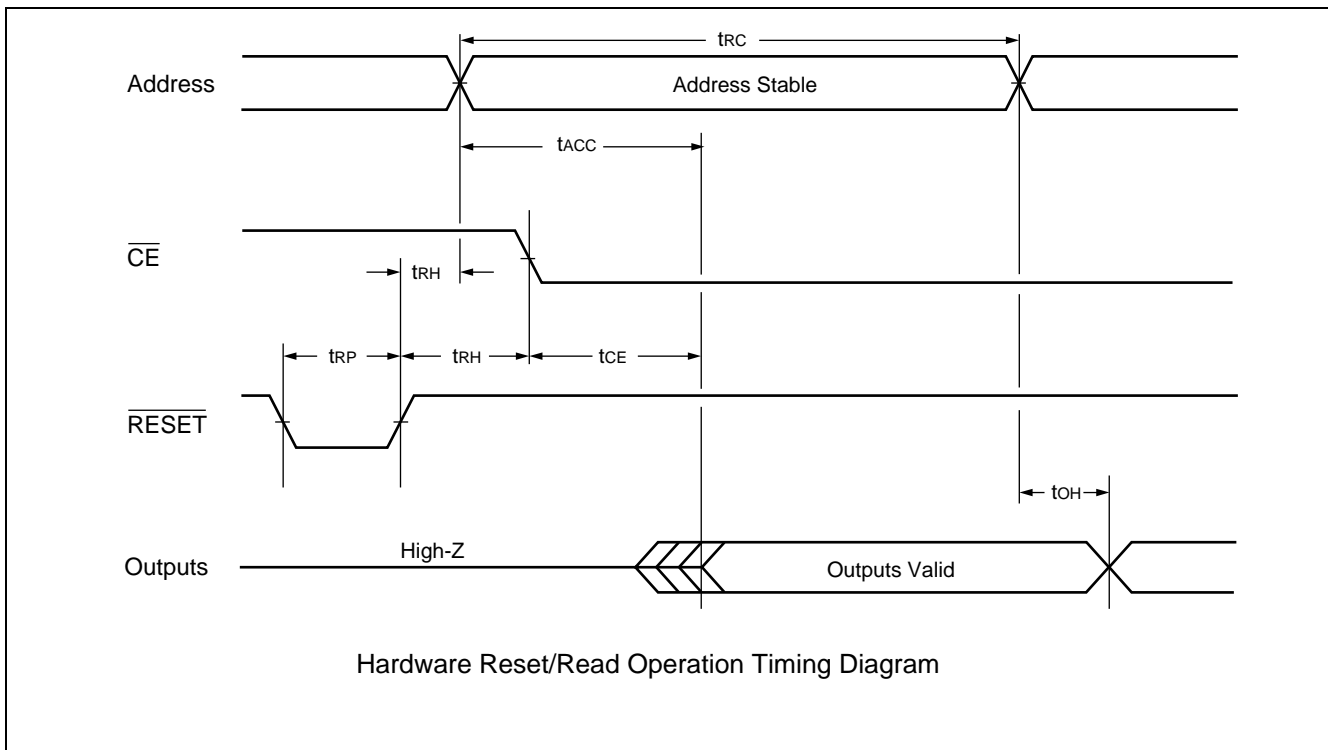
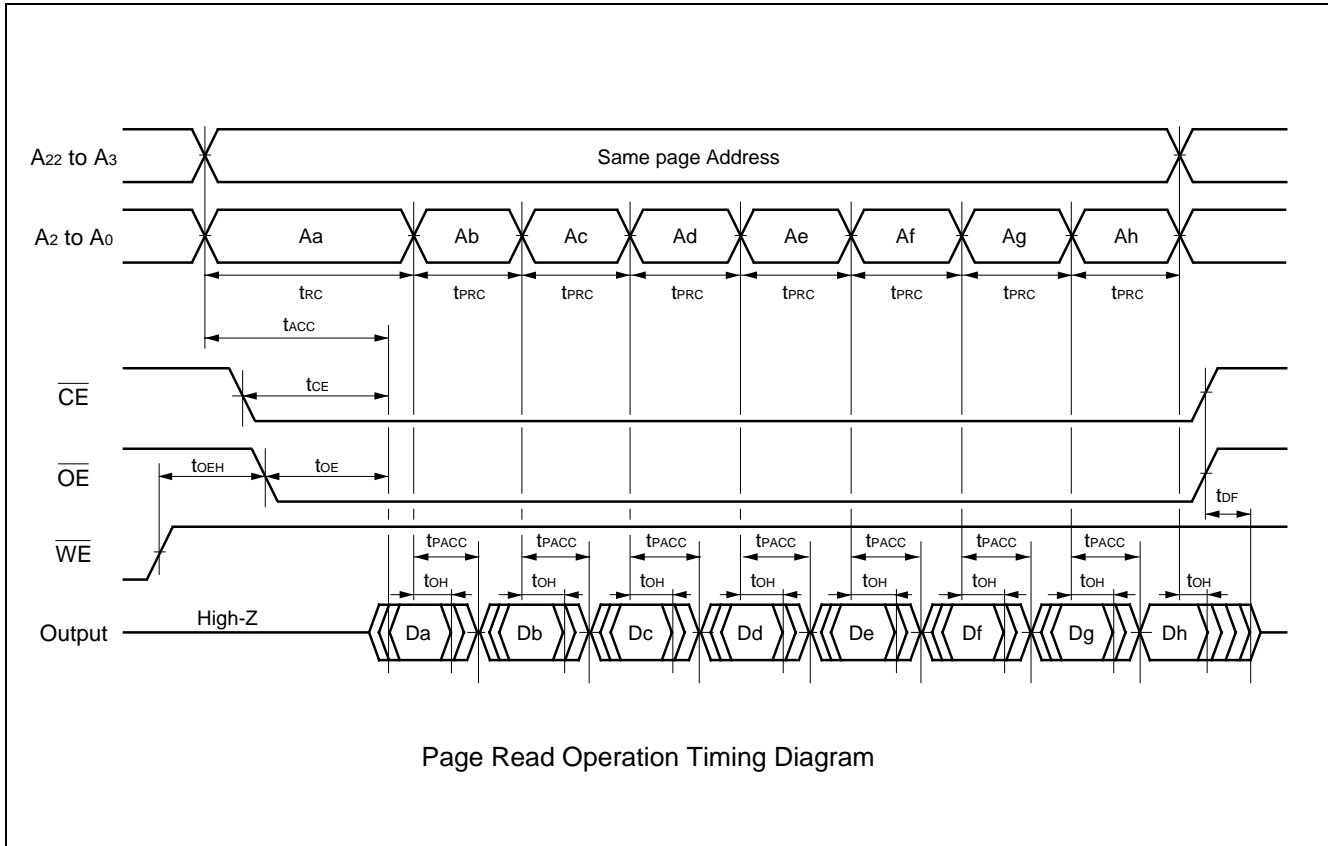
■ TIMING DIAGRAM

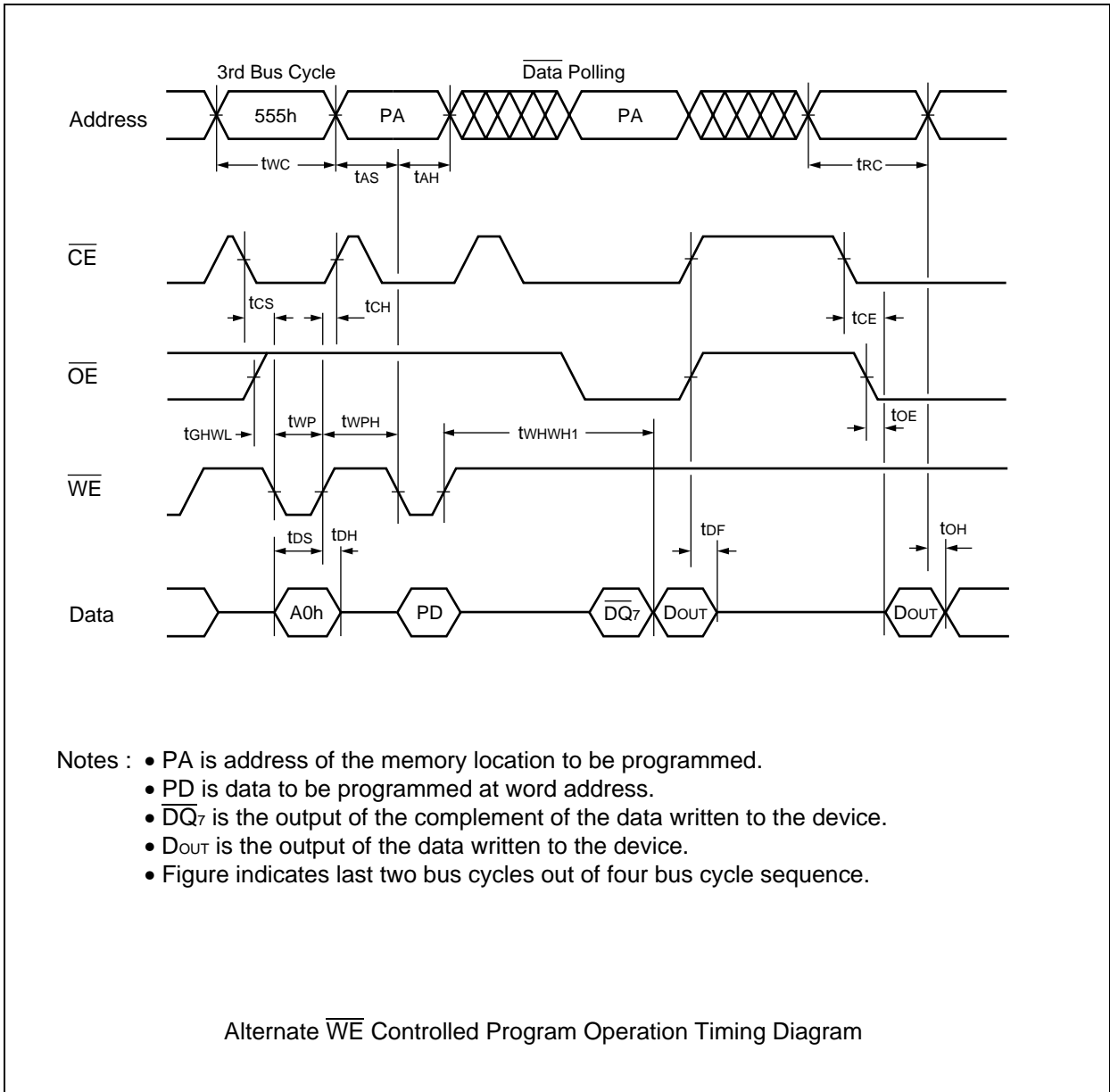
• Key to Switching Waveforms

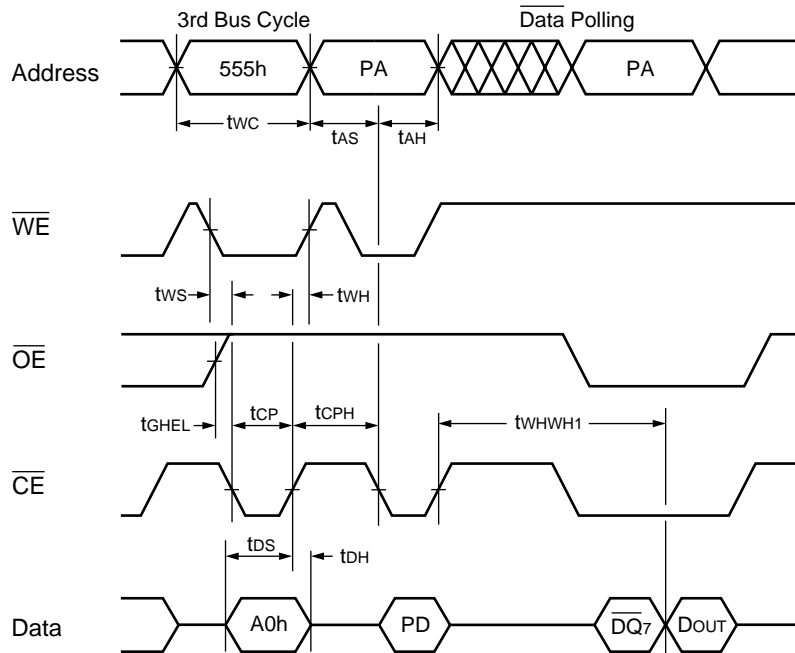
WAVEFORM	INPUTS	OUTPUTS
	Must Be Steady	Will Be Steady
	May Change from H to L	Will Change from H to L
	May Change from L to H	Will Change from L to H
	"H" or "L": Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State



MBM29QM12DH-60

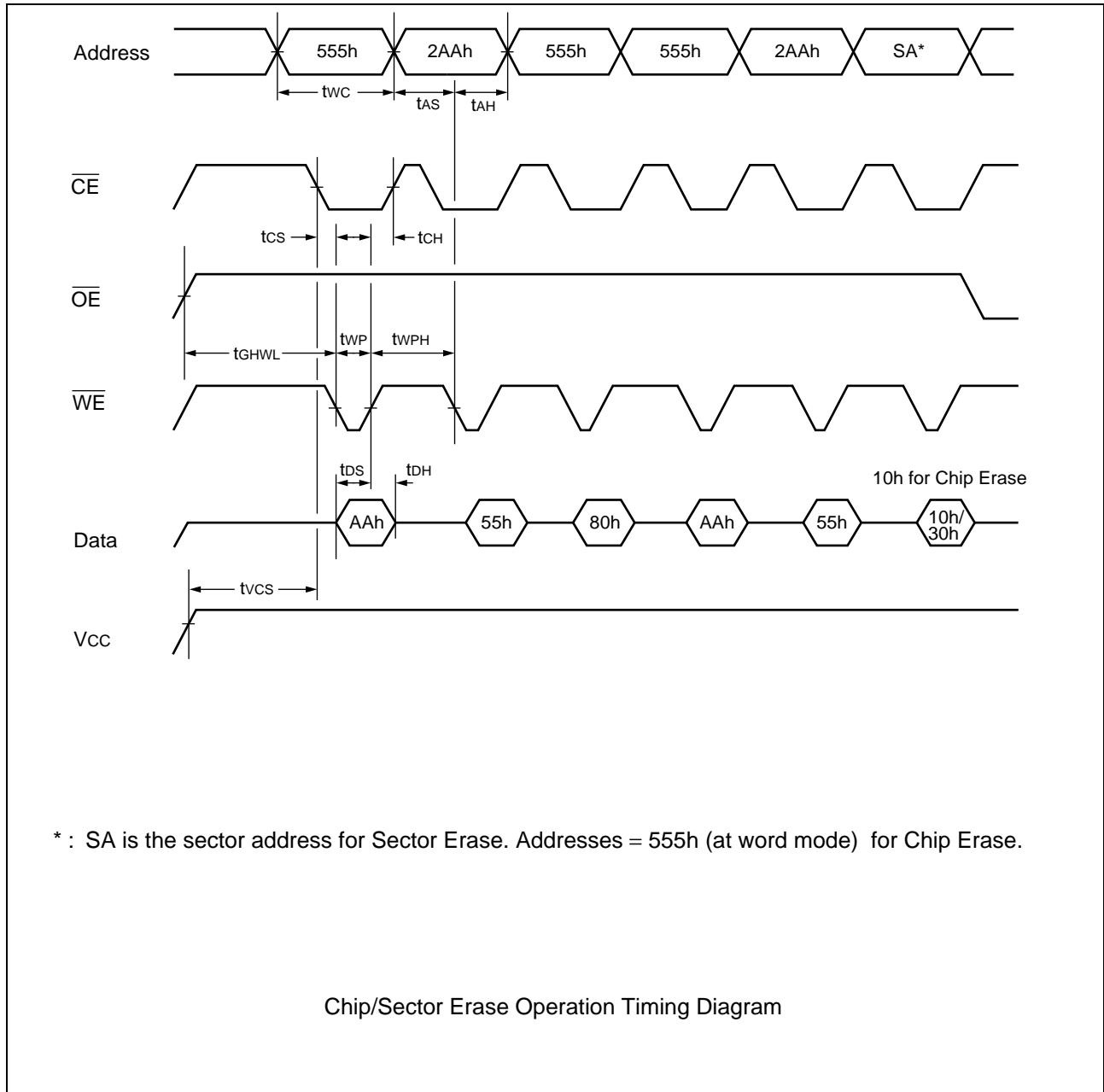


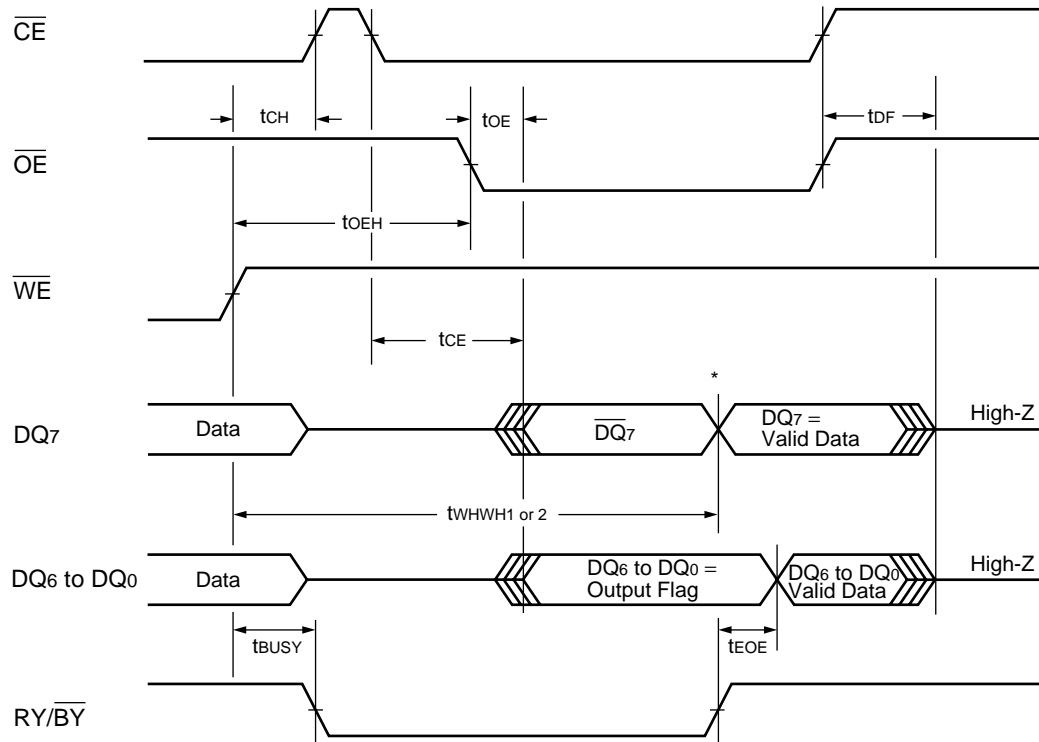




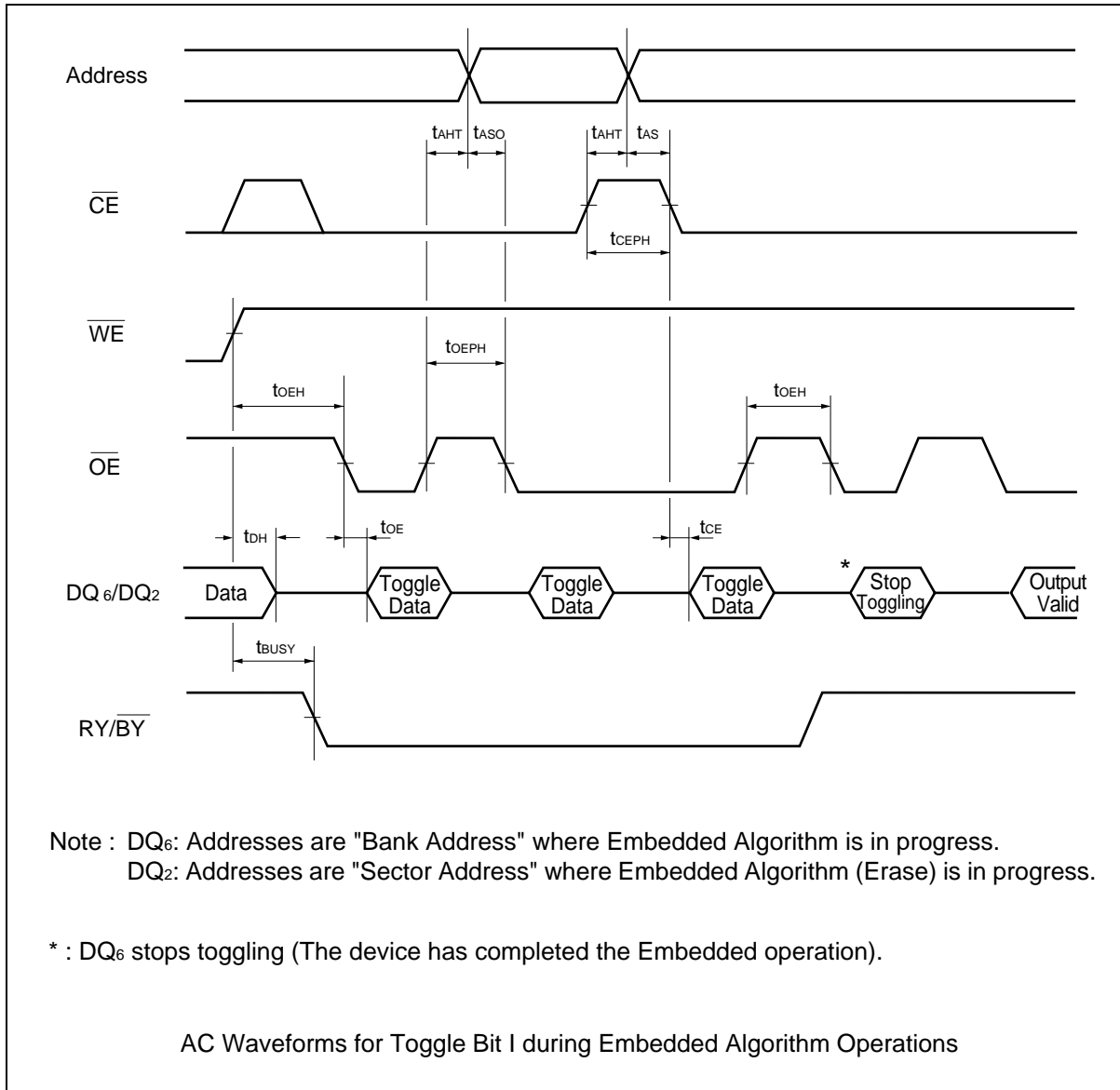
- Notes :
- PA is address of the memory location to be programmed.
 - PD is data to be programmed at word address.
 - $\overline{DQ7}$ is the output of the complement of the data written to the device.
 - D_{OUT} is the output of the data written to the device.
 - Figure indicates last two bus cycles out of four cycle sequence.

Alternate \overline{CE} Controlled Program Operation Timing Diagram

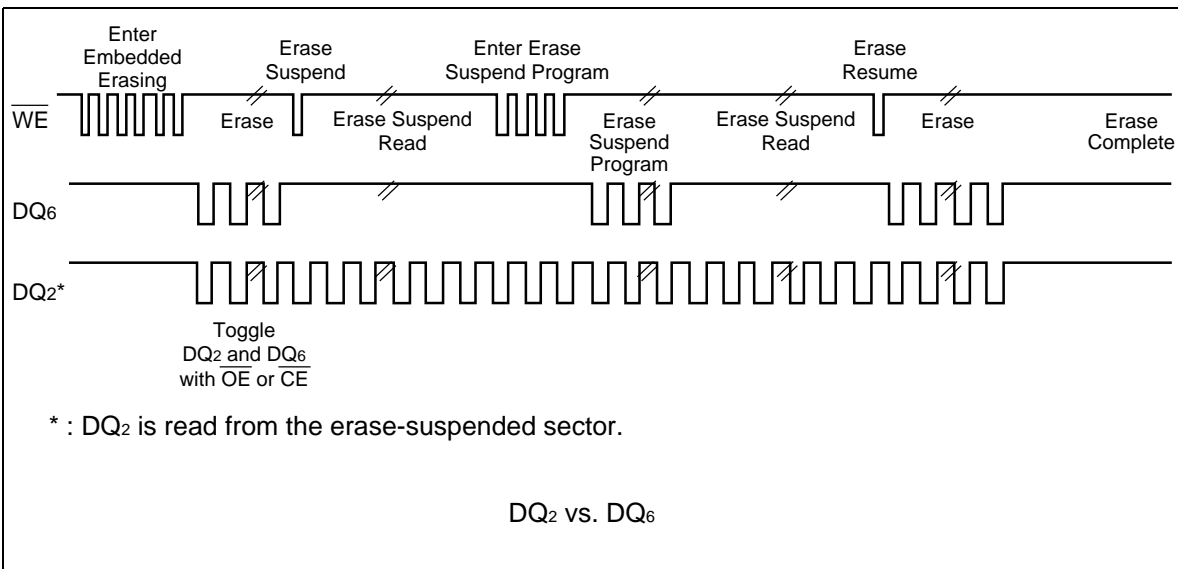
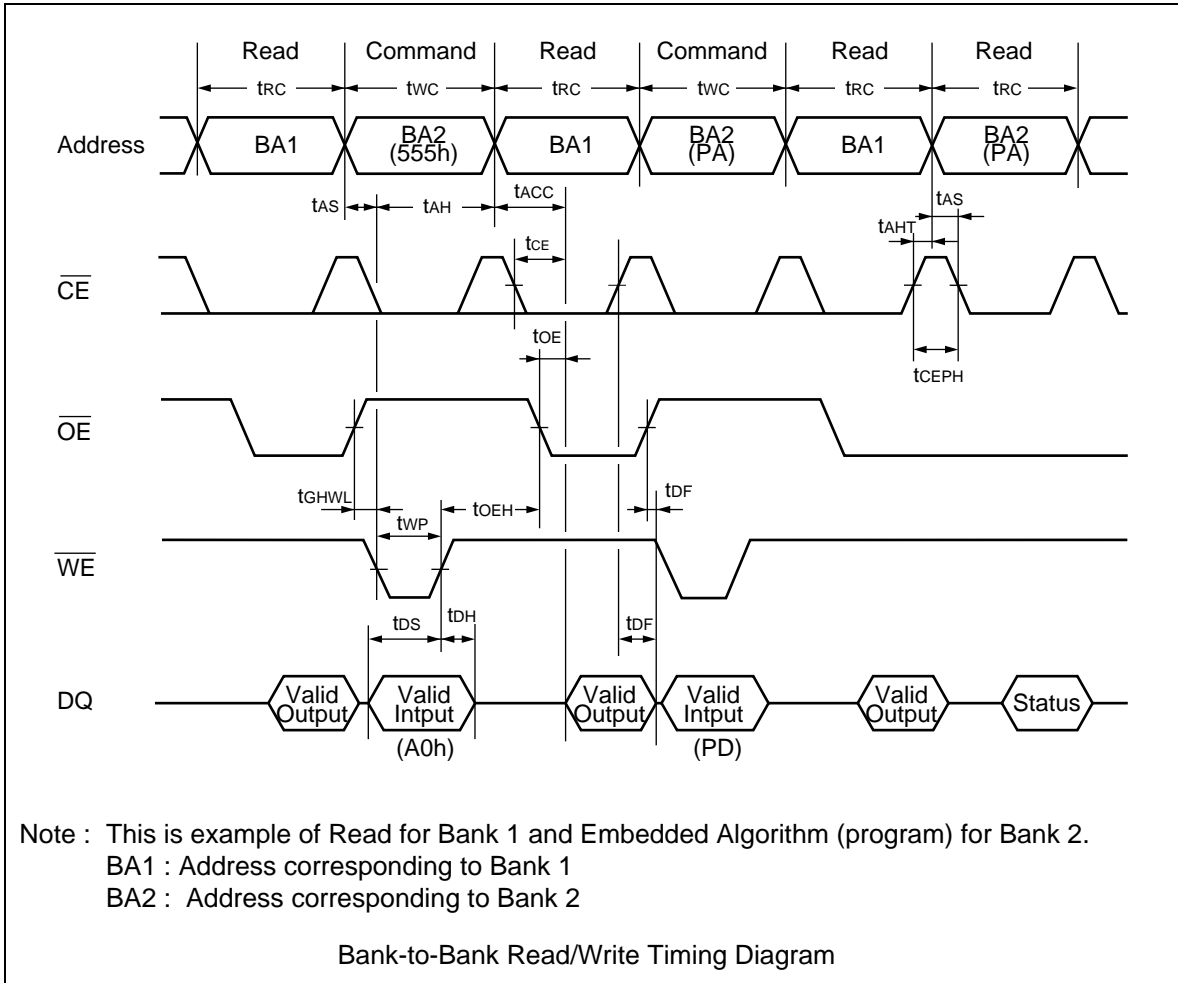


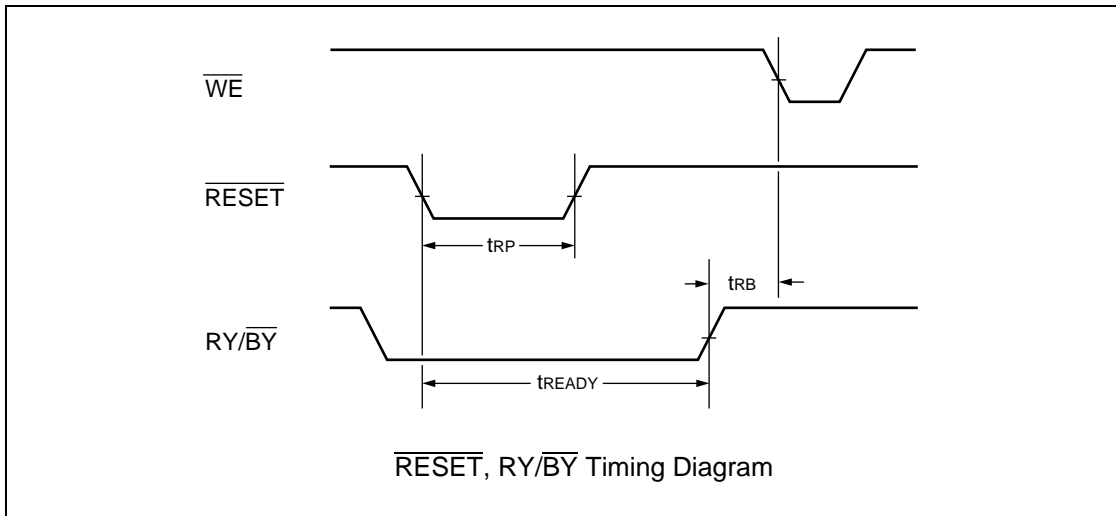
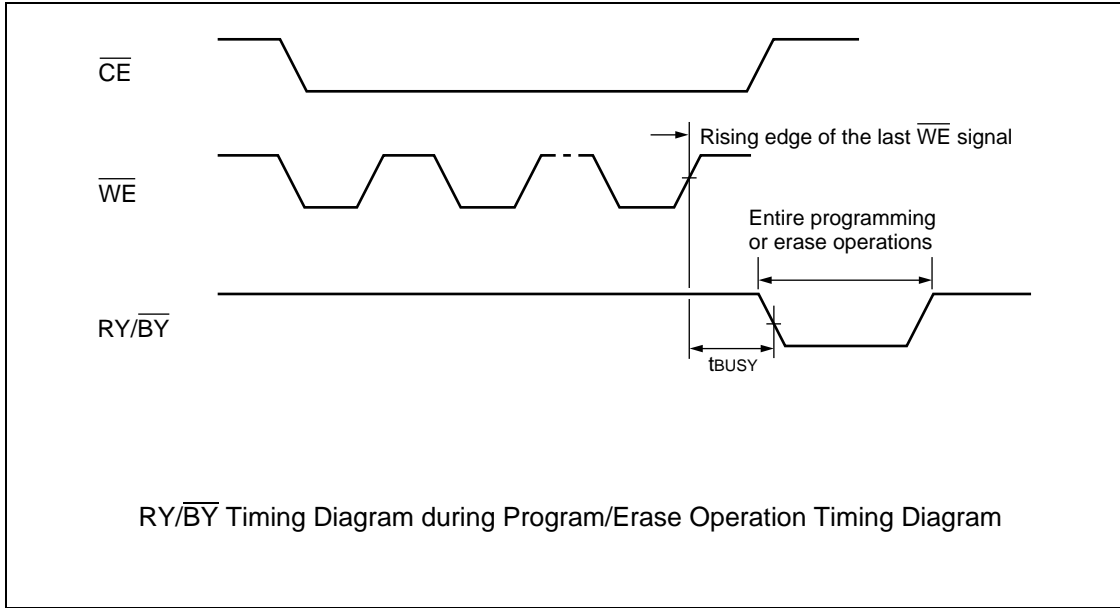


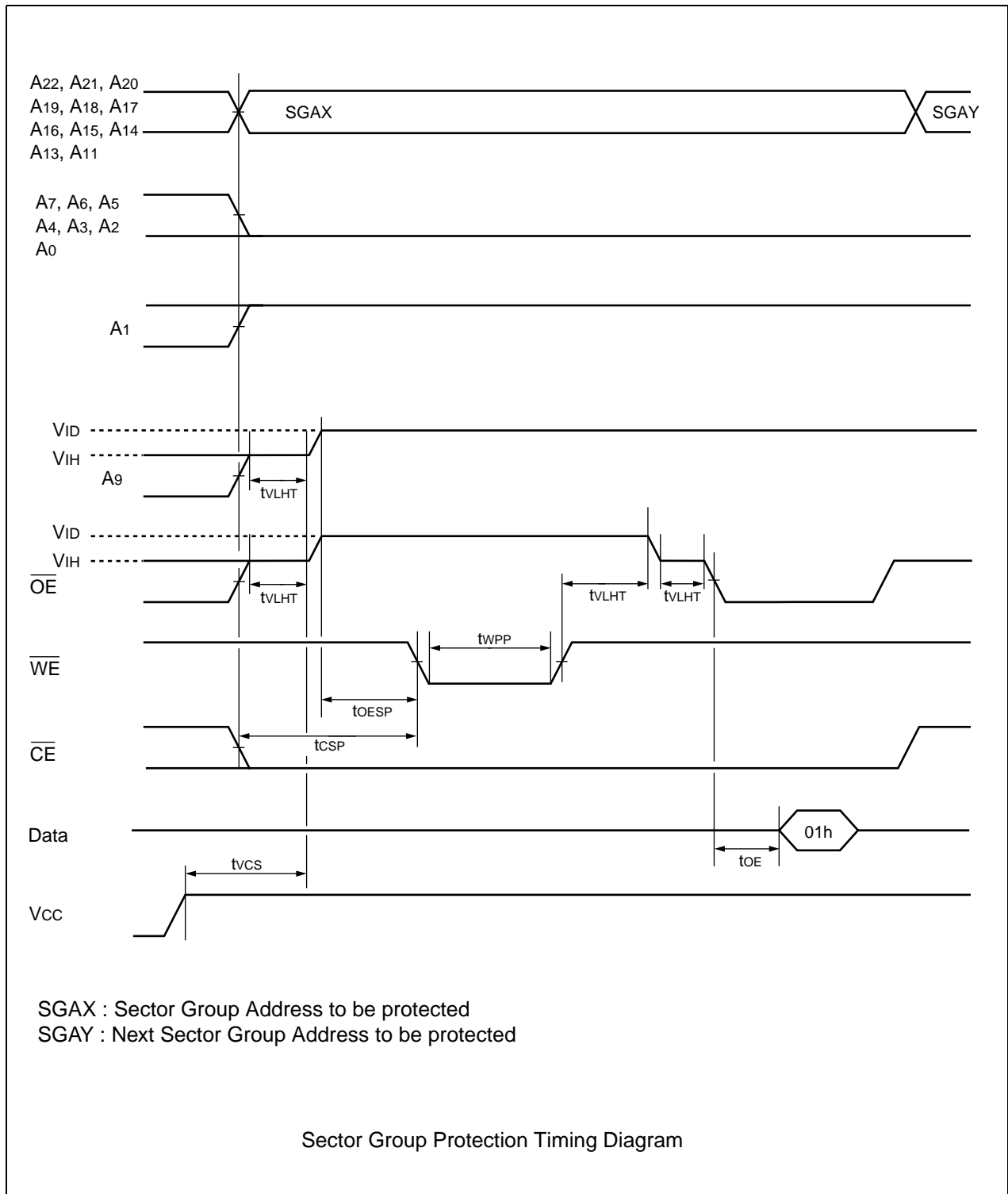
Data Polling during Embedded Algorithm Operation Timing Diagram

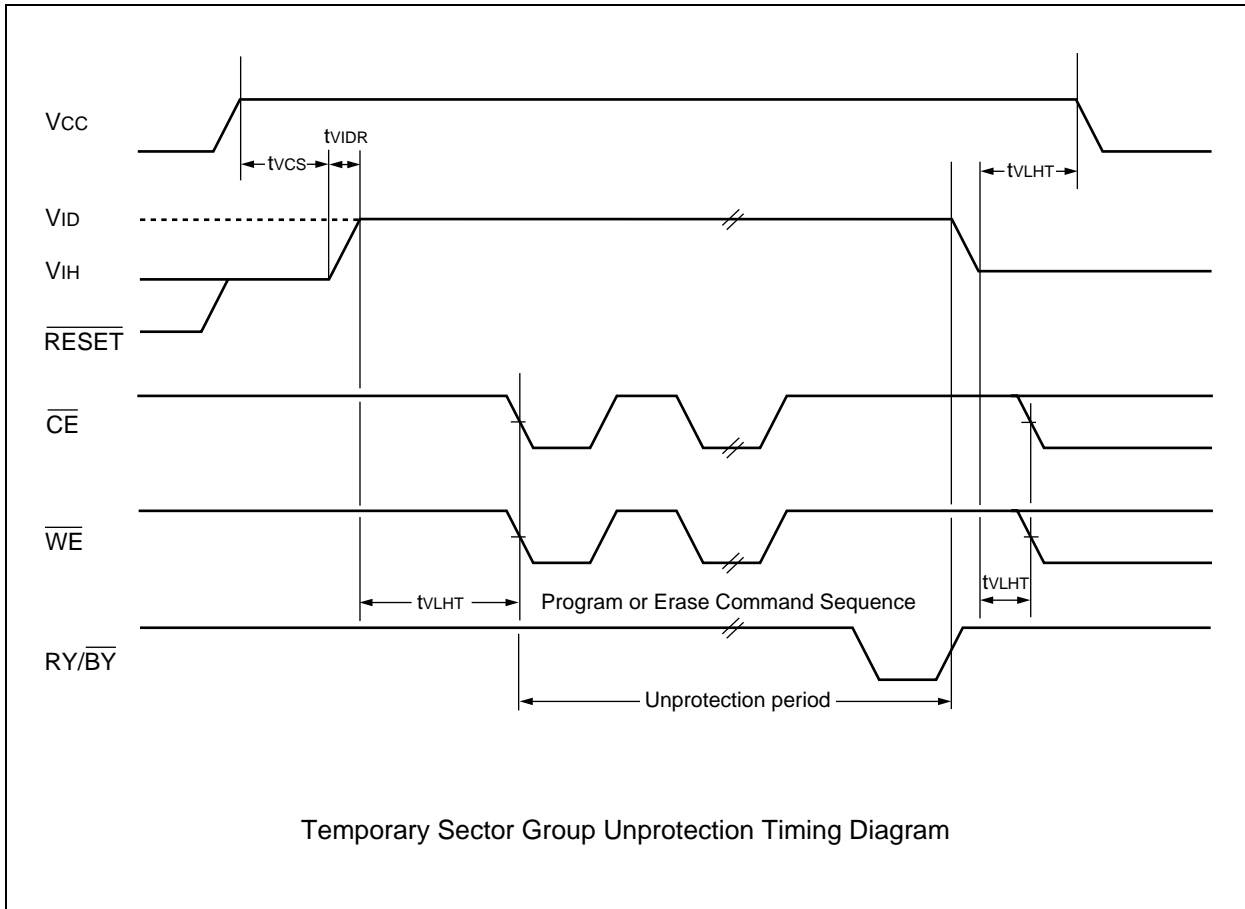


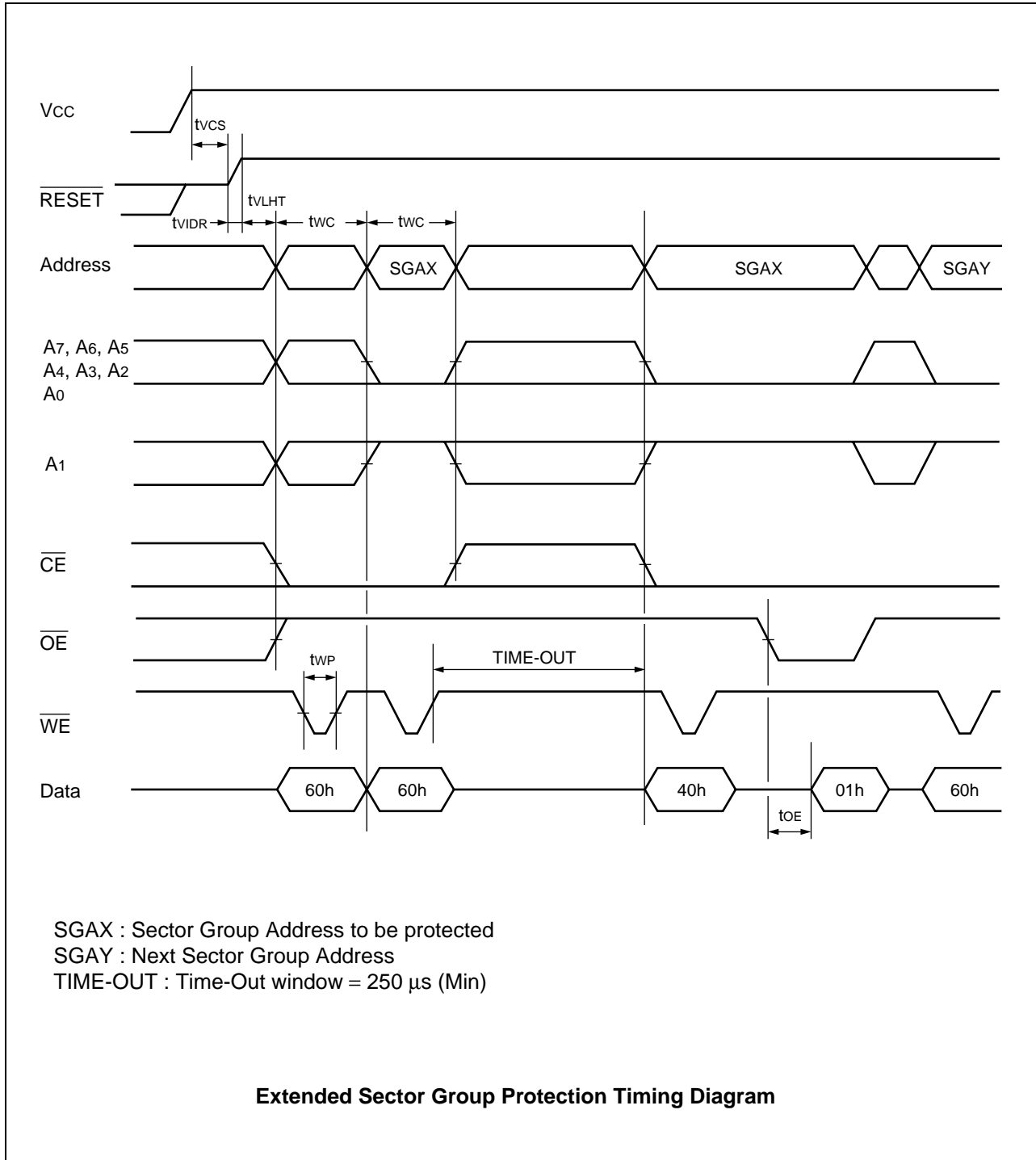
MBM29QM12DH-60



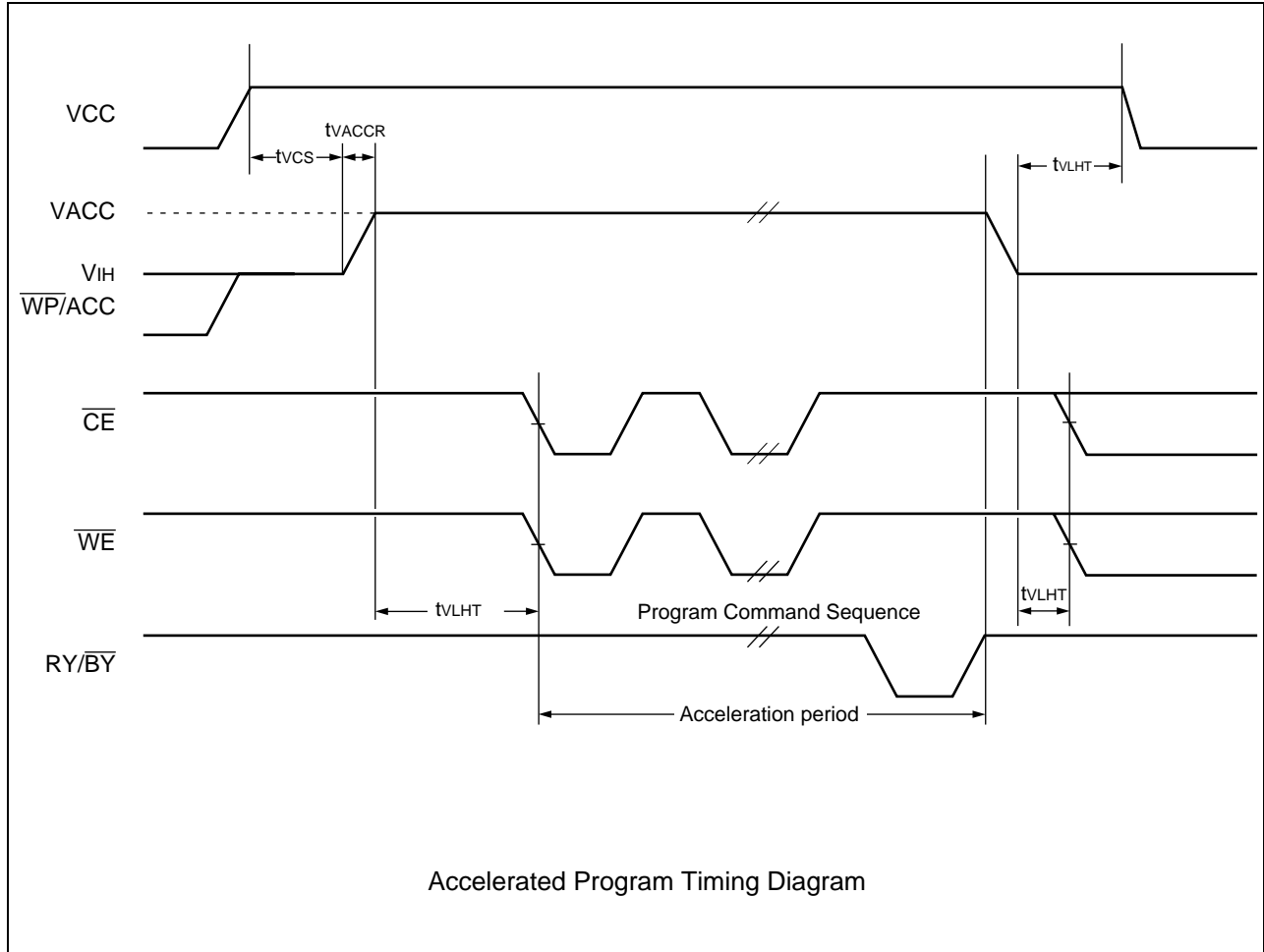






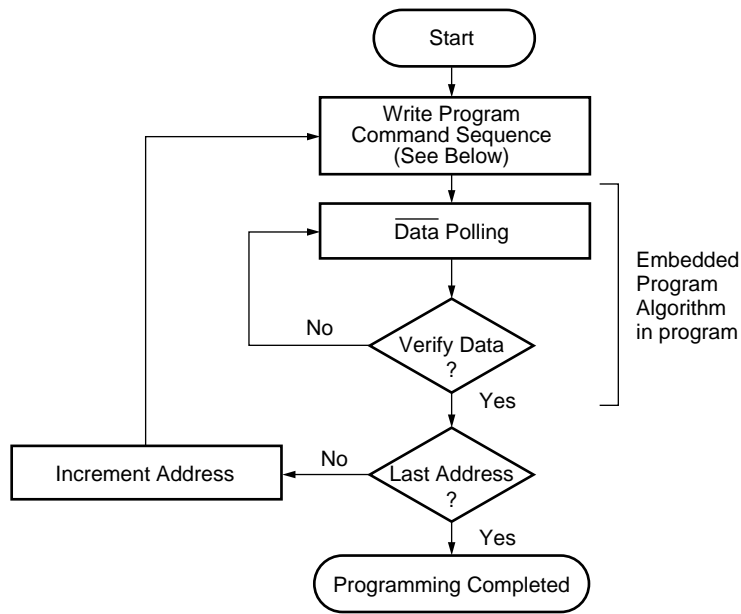


Extended Sector Group Protection Timing Diagram

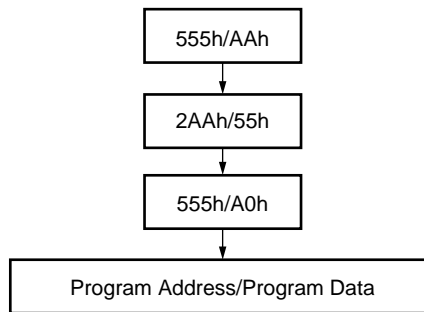


■ FLOW CHART

Embedded Algorithm™

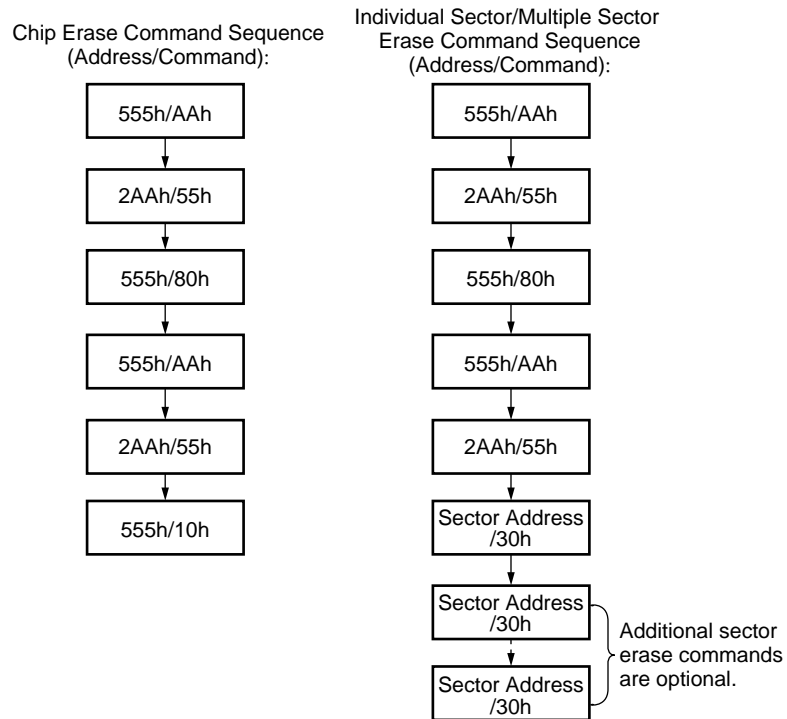
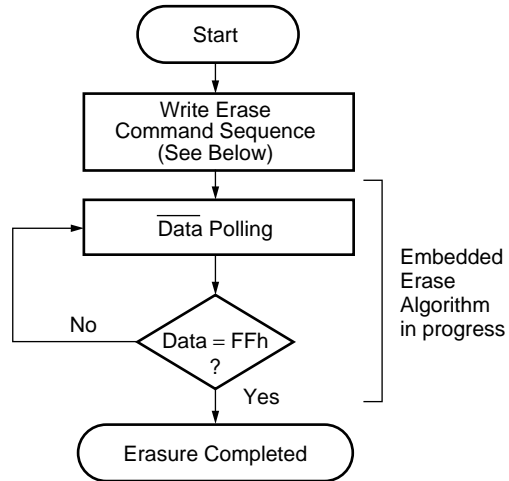


Program Command Sequence (Address/Command):

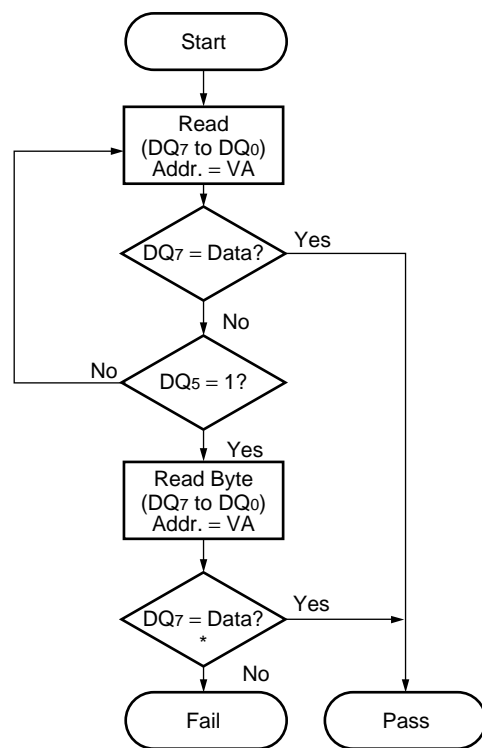


Embedded Program™ Algorithm

Embedded Algorithm™



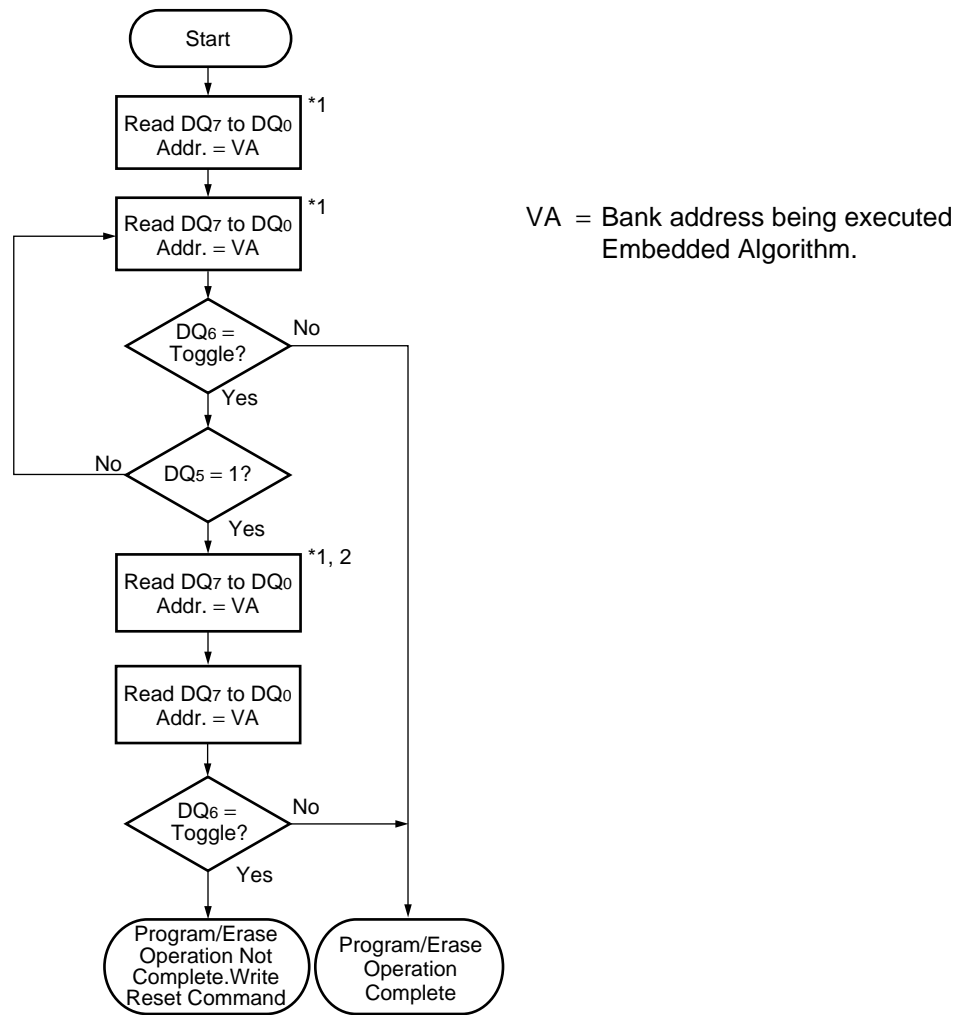
Embedded Erase™ Algorithm



VA = Address for programming
 = Any of the sector addresses within the sector being erased during sector erase or multiple erases operation.
 = Any of the sector addresses within the sector not being protected during sector erase or multiple sector erases operation.

* : DQ₇ is rechecked even if DQ₅ = "1" because DQ₇ may change simultaneously with DQ₅.

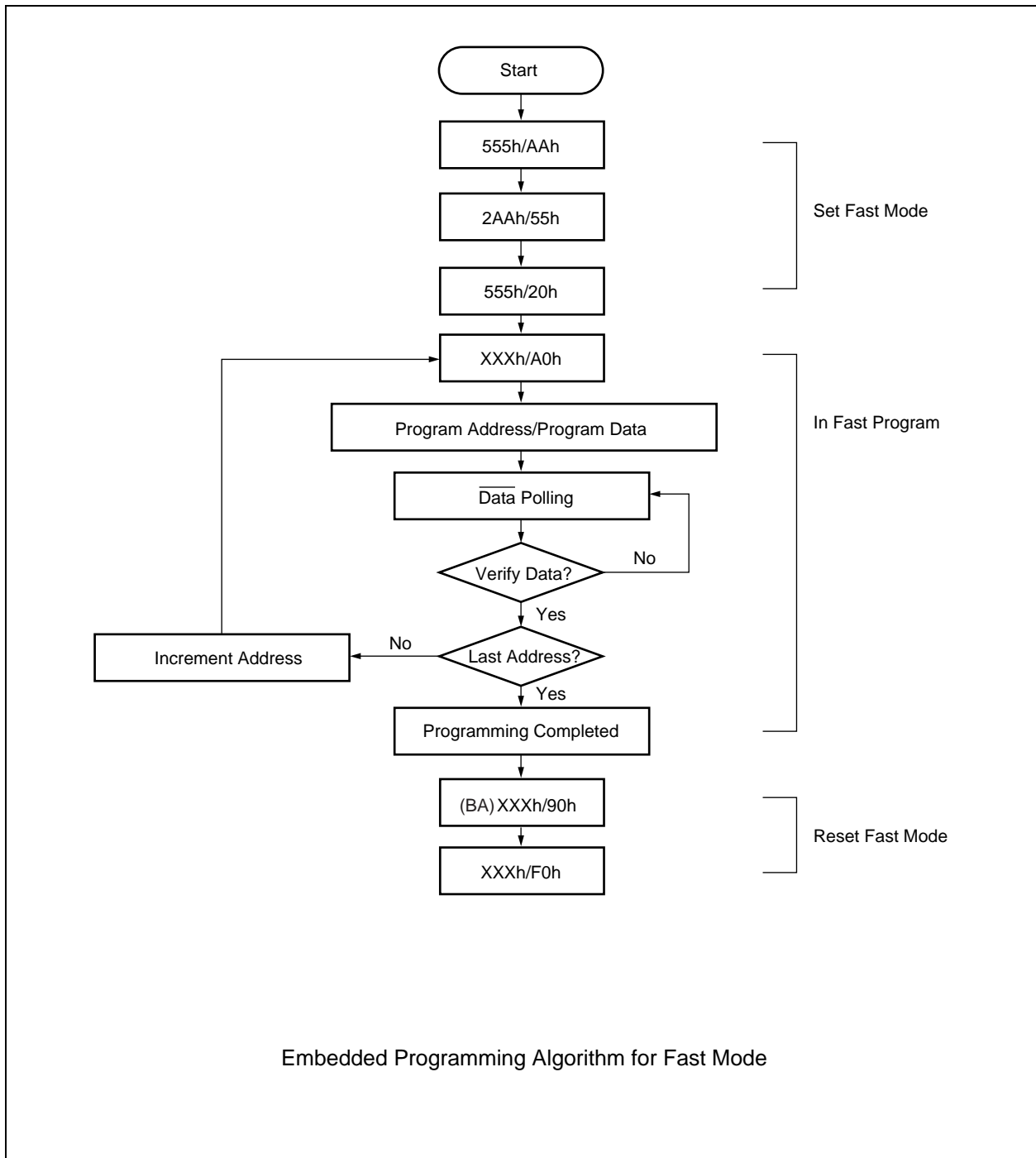
Data Polling Algorithm

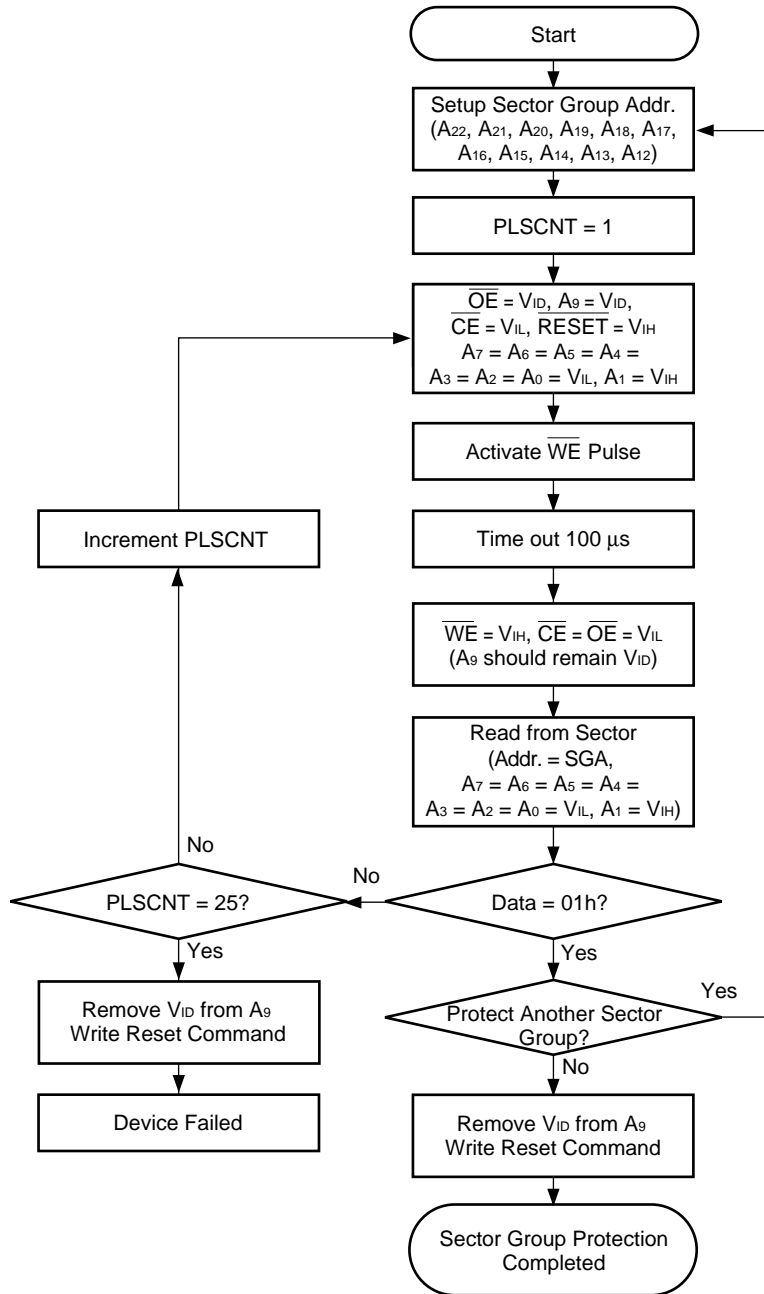


*1 : Read toggle bit twice to determine whether it is toggling.

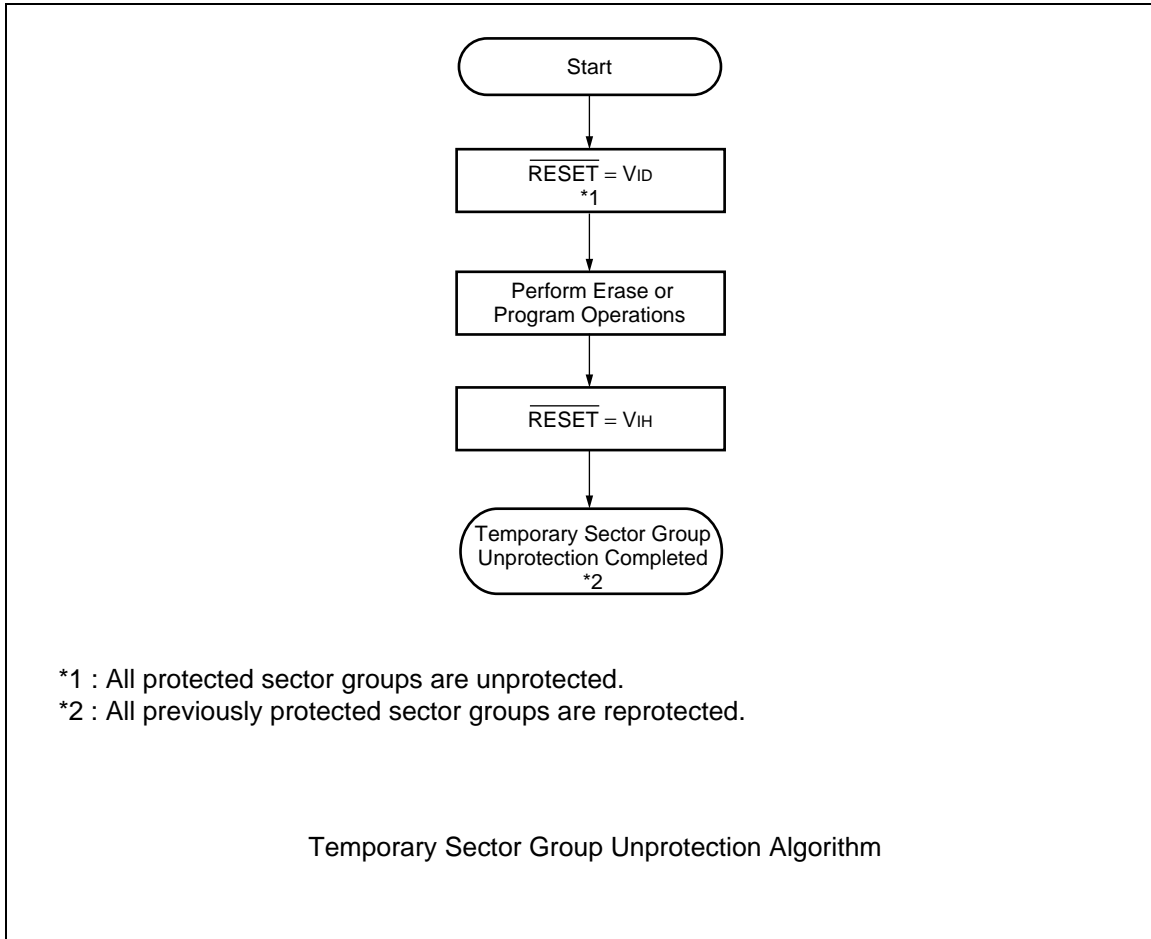
*2 : Recheck toggle bit because it may stop toggling as DQ₅ changes to "1".

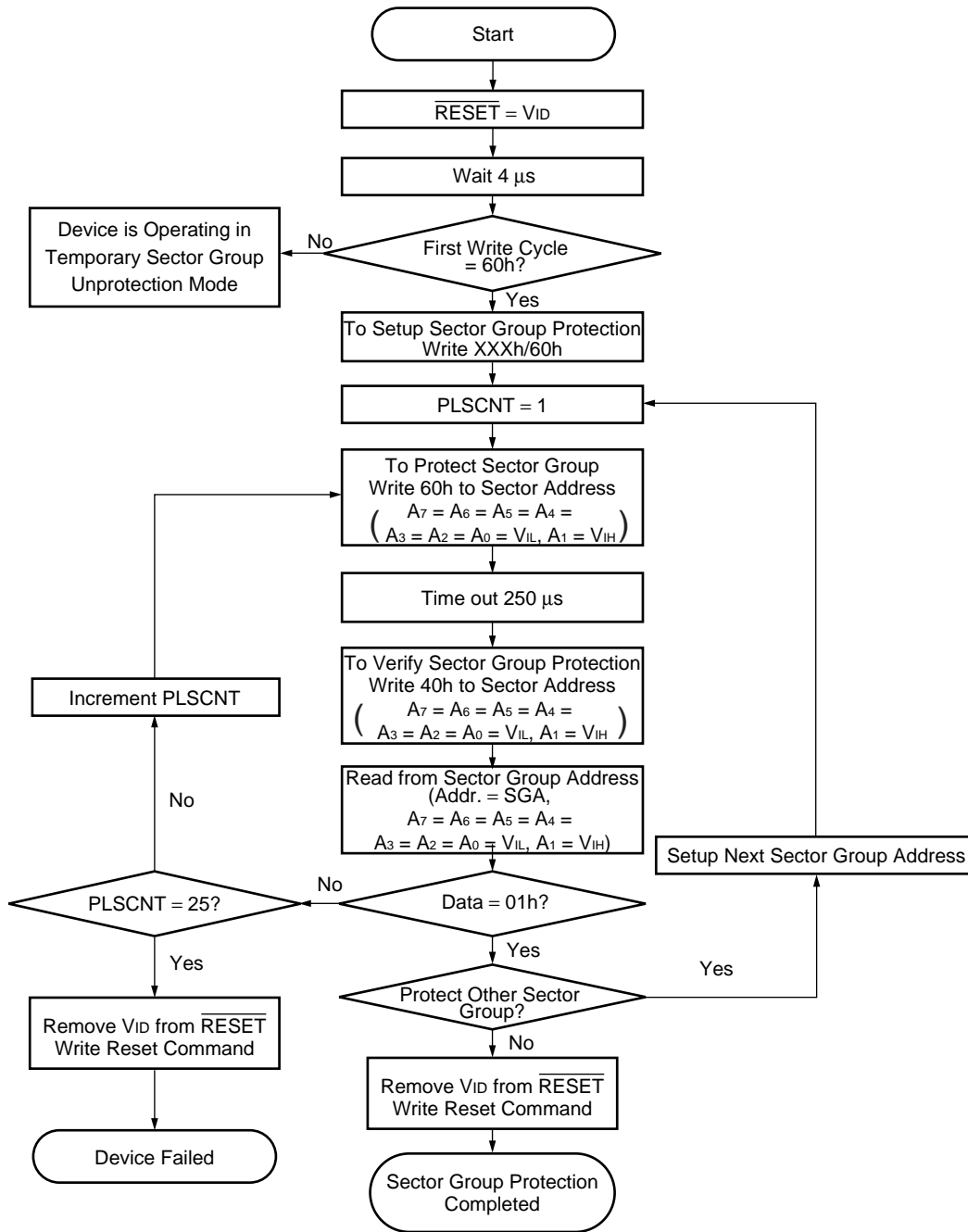
Toggle Bit Algorithm





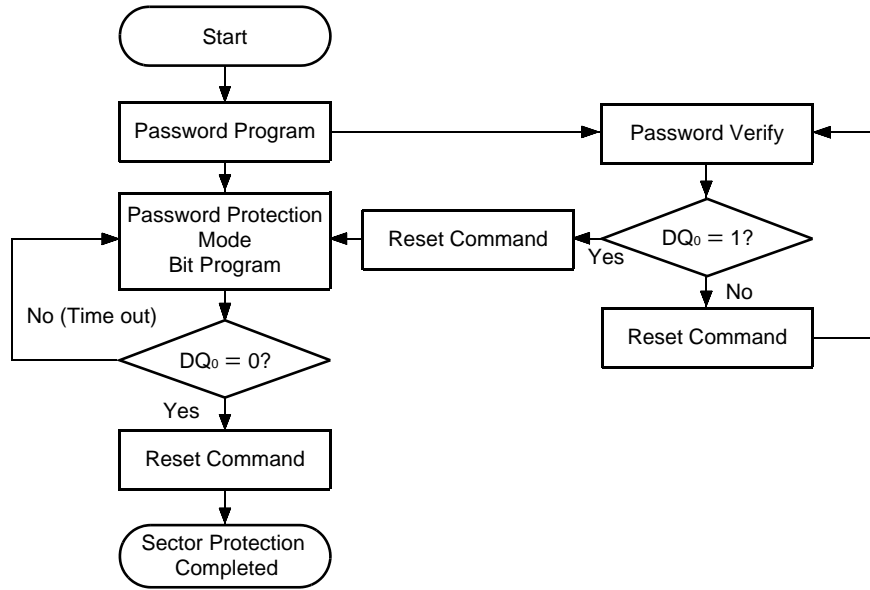
Sector Group Protection Algorithm





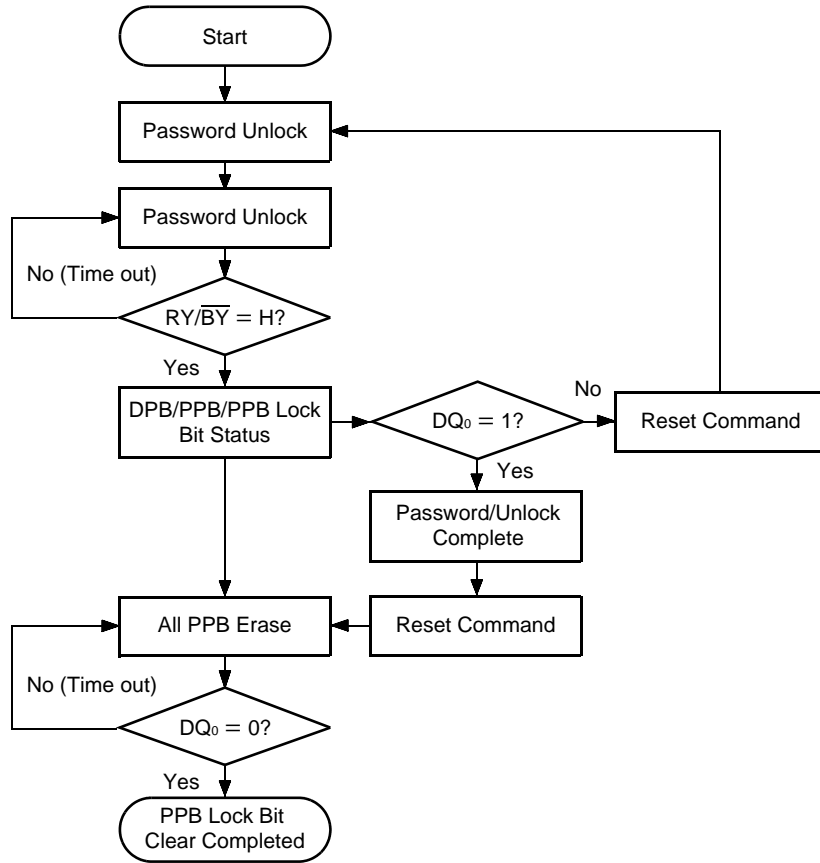
Extended Sector Group Protection Algorithm

Password Mode Choice Method



Password Sector Protect Algorithm

PPB Lock Clear in Password Mode

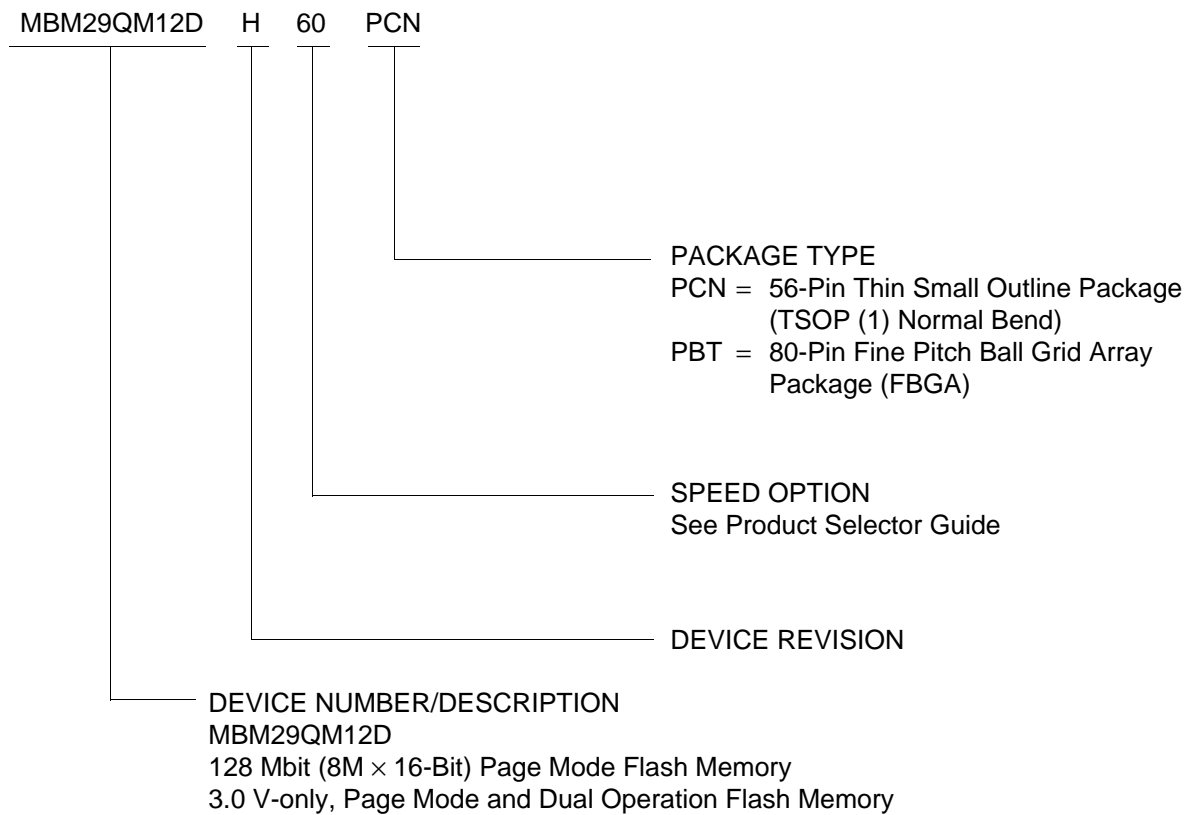


PPB Lock Bit Clear in Password Mode

MBM29QM12DH-60

■ ORDERING INFORMATION

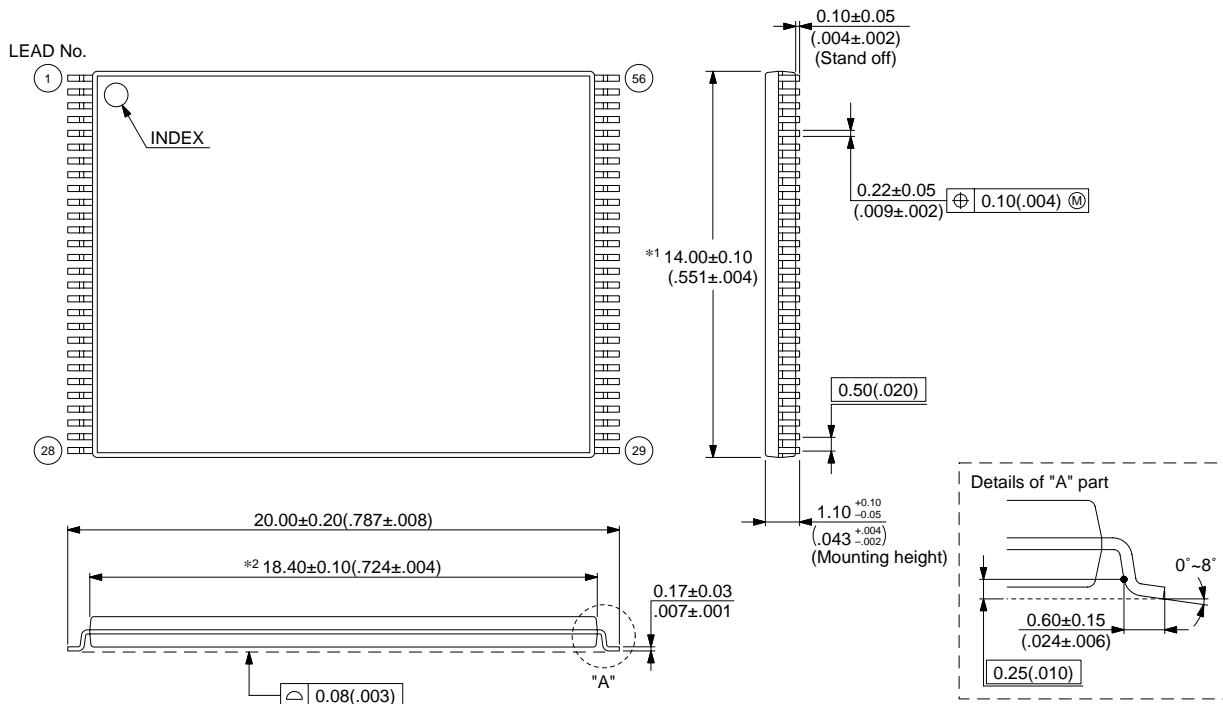
Part No.	Package	Access Time (ns)	Remarks
MBM29QM12DH60PCN	56-pin plastic TSOP (1) (FPT-56P-M01) Normal Bend	60	
MBM29QM12DH60PBT	80-pin plastic FBGA (BGA-80P-M04)	60	



PACKAGE DIMENSIONS

56-pin plastic TSOP(1)
(FPT-56P-M01)

Note 1) *1 : Resin protrusion. (Each side : +0.15 (.006) Max) .
 Note 2) *2 : These dimensions do not include resin protrusion.
 Note 3) Pins width and pins thickness include plating thickness.
 Note 4) Pins width do not include tie bar cutting remainder.



© 2002 FUJITSU LIMITED F56001S-c-4-5

Dimensions in mm (inches) .

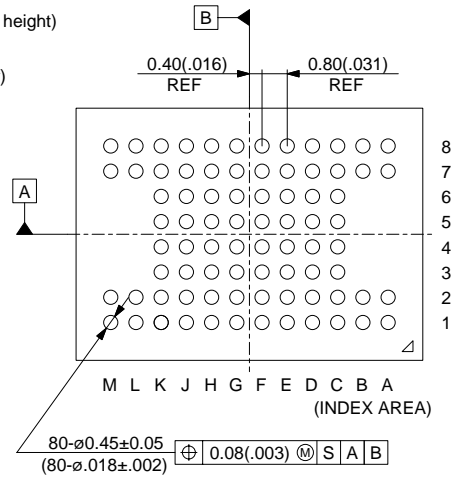
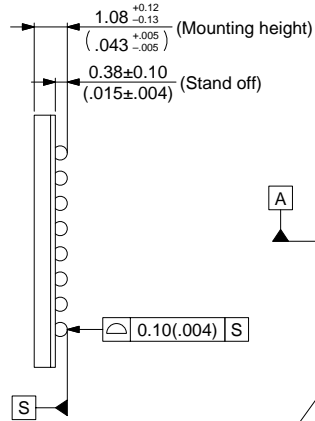
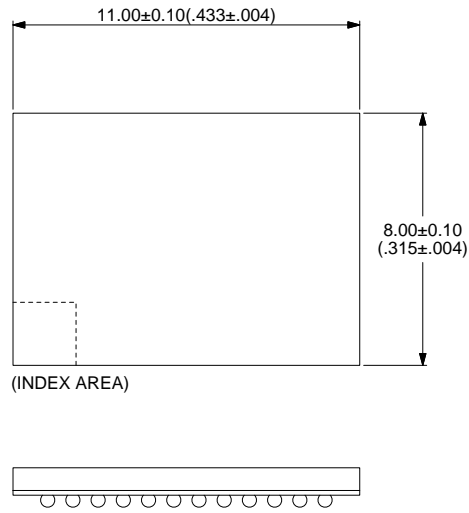
Note : The values in parentheses are reference values.

(Continued)

MBM29QM12DH-60

(Continued)

80-pin plastic FBGA
(BGA-80P-M04)



© 2003 FUJITSU LIMITED B80004S-c-1-1

Dimensions in mm (inches) .

Note : The values in parentheses are reference values.

FUJITSU LIMITED

All Rights Reserved.

The contents of this document are subject to change without notice. Customers are advised to consult with FUJITSU sales representatives before ordering.

The information, such as descriptions of function and application circuit examples, in this document are presented solely for the purpose of reference to show examples of operations and uses of Fujitsu semiconductor device; Fujitsu does not warrant proper operation of the device with respect to use based on such information. When you develop equipment incorporating the device based on such information, you must assume any responsibility arising out of such use of the information. Fujitsu assumes no liability for any damages whatsoever arising out of the use of the information.

Any information in this document, including descriptions of function and schematic diagrams, shall not be construed as license of the use or exercise of any intellectual property right, such as patent right or copyright, or any other right of Fujitsu or any third party or does Fujitsu warrant non-infringement of any third-party's intellectual property right or other right by using such information. Fujitsu assumes no liability for any infringement of the intellectual property rights or other rights of third parties which would result from the use of information contained herein.

The products described in this document are designed, developed and manufactured as contemplated for general use, including without limitation, ordinary industrial use, general office use, personal use, and household use, but are not designed, developed and manufactured as contemplated (1) for use accompanying fatal risks or dangers that, unless extremely high safety is secured, could have a serious effect to the public, and could lead directly to death, personal injury, severe physical damage or other loss (i.e., nuclear reaction control in nuclear facility, aircraft flight control, air traffic control, mass transport control, medical life support system, missile launch control in weapon system), or (2) for use requiring extremely high reliability (i.e., submersible repeater and artificial satellite).

Please note that Fujitsu will not be liable against you and/or any third party for any claims or damages arising in connection with above-mentioned uses of the products.

Any semiconductor devices have an inherent chance of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

If any products described in this document represent goods or technologies subject to certain restrictions on export under the Foreign Exchange and Foreign Trade Law of Japan, the prior authorization by Japanese government will be required for export of those products from Japan.

F0407

© FUJITSU LIMITED Printed in Japan