MM4018

CASE 79-02, STYLE 1
TO-39 (TO-205AD)

HIGH FREQUENCY TRANSISTOR

PNP SILICON

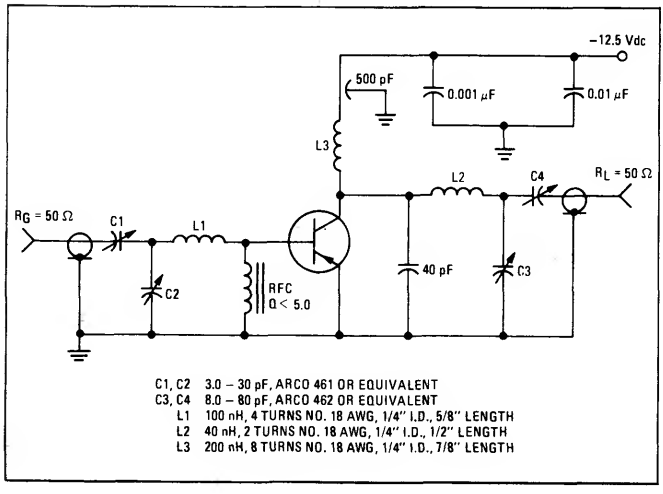
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	20	Vdc
Collector-Base Voltage	V_{CBO}	40	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector Current — Continuous	I_C	0.4	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	5.0 28.6	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 5.0 mAdc, I_B = 0)	$V_{(BR)CEO}$	20	—	—	Vdc
Collector-Base Breakdown Voltage (I_C = 5.0 mAdc, I_E = 0)	$V_{(BR)CBO}$	40	—	—	Vdc
Emitter-Base Breakdown Voltage (I_E = 1.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	—	—	Vdc
Collector Cutoff Current (V_{CE} = 15 Vdc, I_B = 0)	I_{CEO}	—	—	20	μAdc
Collector Cutoff Current (V_{CB} = 15 Vdc, I_E = 0)	I_{CBO}	—	—	10	μAdc
Collector Cutoff Current (V_{CE} = 40 Vdc, V_{BE} = 0)	I_{CES}	—	—	0.1	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 50 mAdc, V_{CE} = 5.0 Vdc)	h_{FE}	10	—	—	—
SMALL SIGNAL CHARACTERISTICS					
Current-Gain — Bandwidth Product (I_C = 50 mAdc, V_{CE} = 15 Vdc, f = 100 MHz)	f_T	—	900	—	MHz
Output Capacitance (V_{CB} = 12.5 Vdc, I_E = 0, f = 100 kHz)	C_{obo}	—	3.5	—	pF
FUNCTIONAL TEST					
Power Output (Figure 1) (P_{in} = 50 mW, V_{CC} = 12.5 Vdc, f = 175 MHz)	P_{out}	0.5	—	—	Watt
Collector Efficiency (Figure 1) (P_{in} = 50 mW, V_{CC} = 12.5 Vdc, f = 175 MHz)	η	45	55	—	%

FIGURE 1 – 175 MHz OUTPUT POWER TEST CIRCUIT



C1, C2 3.0 – 30 pF, ARCO 461 OR EQUIVALENT
C3, C4 8.0 – 80 pF, ARCO 462 OR EQUIVALENT
L1 100 nH, 4 TURNS NO. 18 AWG, 1/4" I.D., 5/8" LENGTH
L2 40 nH, 2 TURNS NO. 18 AWG, 1/4" I.D., 1/2" LENGTH
L3 200 nH, 8 TURNS NO. 18 AWG, 1/4" I.D., 7/8" LENGTH

FIGURE 2 – POWER OUTPUT versus POWER INPUT

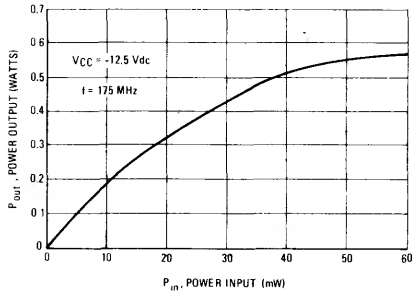


FIGURE 3 – PARALLEL EQUIVALENT OUTPUT CAPACITANCE versus FREQUENCY

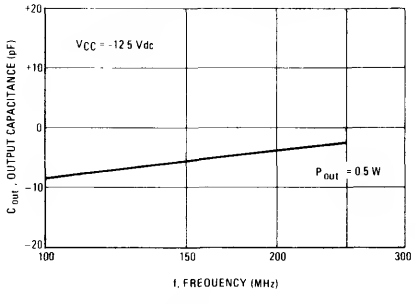


FIGURE 4 – PARALLEL EQUIVALENT INPUT RESISTANCE versus FREQUENCY

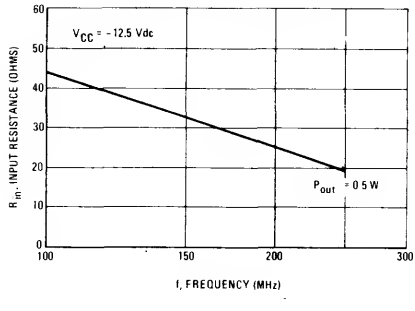
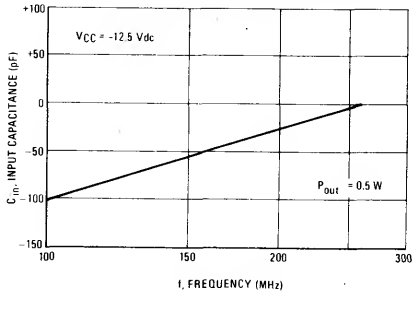


FIGURE 5 – PARALLEL EQUIVALENT INPUT CAPACITANCE versus FREQUENCY



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