Shenzhen LIZE Electronic Technology Co., Ltd

SPECIFICATION

L2264

Current Mode PWM Controller

REV 1.0

General Description

L2264 is a current mode PWM power switch IC. It combines a current mode PWM controller and a power MOSFET. It is optimized for high performance off-line flyback converter application in sub 18 W range. For lower the standby power and higher RoHS compliant, the IC offers a Burst Mode control feature and ultra-low start-up current and operating current, that is, at the condition of no load or light load,L2264 can reduce the switch frequency linearly which minimize the switching power loss; the ultra-low startup current and operating current make a reliable power for startup design, and also large resistor can be used in the startup circuit to improve switching efficiency.

The internal synchronous slope compensation circuit reduces the possible subharmonic oscillation at high PWM duty cycle output. Leading-edge blanking on current sense(CS) input removes the signal glitch due to snubber diode circuit reverse recovery and thus greatly reduces the external component count and system cos t in the design. L2264 offers comprehensive protection coverage with automatic self-recovery feature, including cycle by cycle over current protection (OCP), over load protection (OLP), under voltage lockout (UVLO). The gate-driven output is clamped to maximum 18V to protect the internal MOSFET.

Excellent EMI performance is achieved by using the soft-switching and frequency jittering at the totem-pole-gate-drive output. The tone energy at below 20KHZ is minimized in the design and audio noise is eliminated during operation. The L2264 is the ideal substitute of the linear power supply or the RCC-mode power, for a better performance of the whole switch power system and a lower cost.

L2264 is available in DIP-8 package.

Features

- Burst Mode control
- 4uA ultra-low startup current
- 1.4mA Low operating current
- Built-in Leading-edge blanking
- Built-in synchronous slope compensation circuit
- Current Mode operates
- External programmable PWM switching frequency
- Cycle by cycle over current protection (OCP)
- VDD over voltage clamp & under voltage lockout(UVLO)
- Maximum Gate-driven output voltage clamped at 18V
- Frequency jittering
- Constant limited output power
- Over load protection (OLP)
- Free audio noise operation
- Build in high voltage power MOSFET

Applications

Universal switch power supply equipment and offline AC/DC flyback power converter

Power Adapter
STB Power Supplies
Open-frame SMPS
Battery Charger

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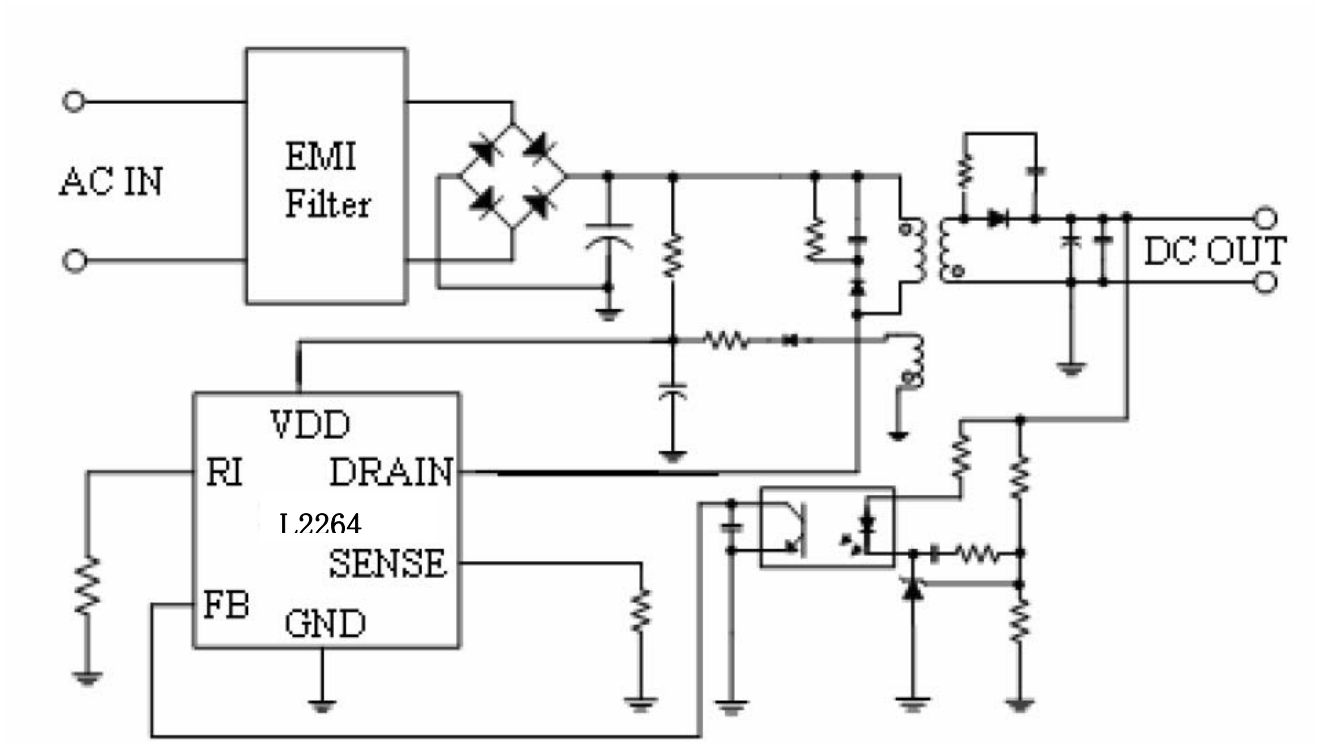
Typical Application Circuit

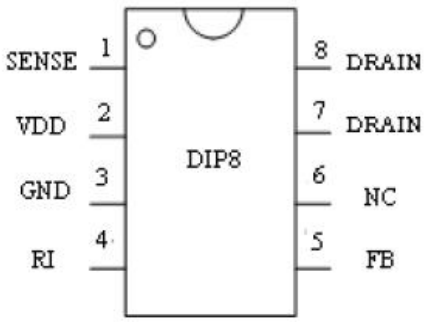


Output Power Table

Product	230VAC±15%	85-265VAC
	Open Frame1	Open Frame1
L2264	18W	13W

Note1:Maximum practical continuous power in an open frame design with sufficient drain pattern as a heat sink,at 50℃

Pin Definition and Device Marking



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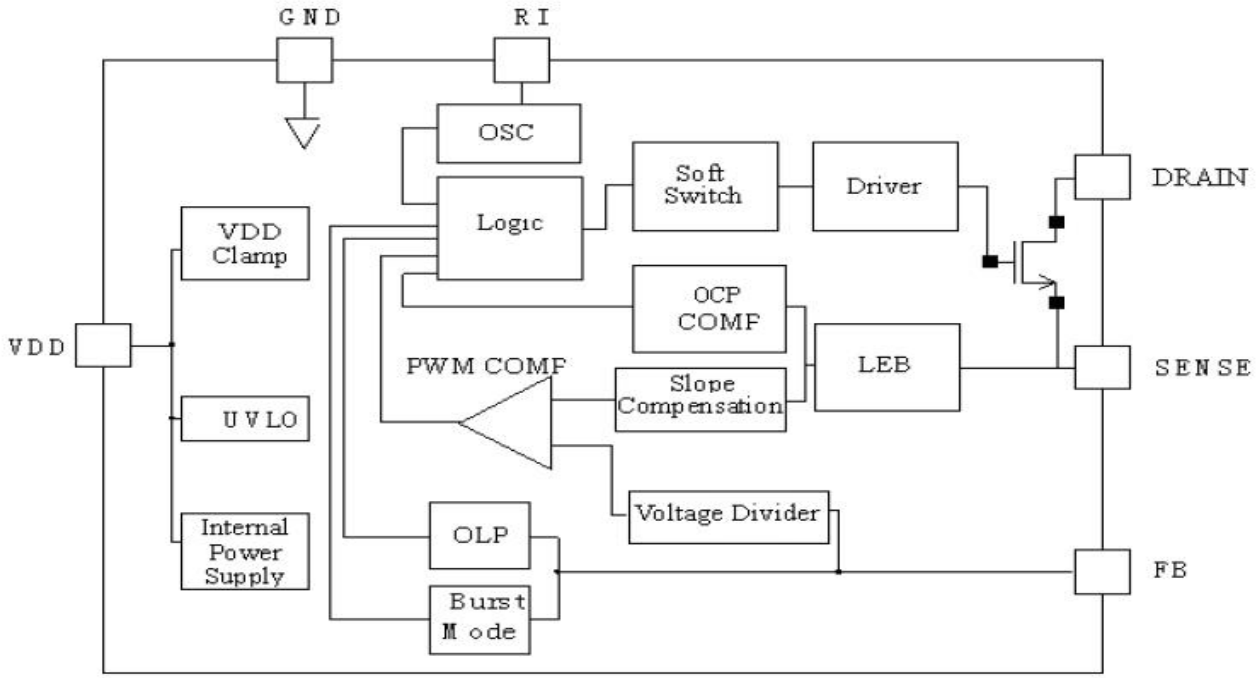
Pin Function Description

Pin Name	Pin Number	Pin Type	Function Description
SENSE	1	Current Monitoring	Current sense input
VDD	2	Power	Power supply
GND	3	GND	Ground
RI	4	Frequency Setting	Internal oscillator frequency setting pin. A resistor which is connected between RI and GND sets the PWM frequency.
FB	5	Feedback Input	Feedback input pin. The PWM duty cycle is determined by voltage level into this pin and the current-sense signal at Pin 1. The internal protection circuit will automatically shutdown when the FB voltage level exceeds a preset threshold voltage.
NC	6	Floating	Floating
DRIAN	7/8	Internal MOSFET Drain	Internal HV MOSFET Drain, connected to the primary lead of the transformer.

Block Diagram



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Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
Drain voltage(off-state)	Internal HV MOSFET Drain voltage	-0.3~650	V
VDD	DC supply voltage	30	V
V_{FB}	FB input voltage	-0.3~7	V
V_{SENSE}	SENSE input voltage	-0.3~7	V
V_{RI}	RI input voltage	-0.3~7	V
T_J	Operating junction temperature	-20~150	℃
T_{STG}	Storage temperature	-40~150	℃
V_{CV}	VDD clamp voltage	34	V
I_{CC}	VDD DC clamp current	10	mA

Note: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, functional operation of the device at these or any other conditions beyond those indicated in the Recommended Operating Conditions section are not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.

Recommended Operating Condition

Symbol	Parameter	Value	Unit
VDD	VDD supply voltage	10~30	V
RI	RI resistor value	100	Kohm
T_A	Operating temperature	-20~85	℃

ESD Information

Symbol	Parameter	Value	Unit
$V_{ESD-HBM}$	Human model	3	KV
V_{ESD-MM}	Machine model	150	V

Electrical Characteristics

Supply Voltage (VDD)						
symbol	**parameter**	**Test condition**	**Min**	**Typ**	**Max**	**Unit**
VDD_OP	Operation voltage				30	V
UVLO_ON	Turn on threshold Voltage		7.7	8.8	9.8	V
UVLO_OFF	Turn-off threshold Voltage		13	14	15	V
I_VDD_ST	Start up current	VDD=13V,RI=100K		3	10	uA
I_VDD_OP	Operation Current	VDD=16V,RI=100K,V_{FB}=3V		2.3		mA
VDD Clamp	VDD Zener Clamp Voltage	IVDD=10mA	27	29	31	V
Feedback Input Section						

VFB_Open	VFB Open Loop Voltage			5.7		V
IFB_Short	FB Pin Short Current	FB Shorted to GND	0.75	0.865	0.98	mA
VTH_PL	Power limiting FB Threshold			3.7		V
TD_PL	Power limiting Debounce			32		ms
ZFB_IN	Input Impedance			6		kΩ
Max_Duty	Maximum duty cycle			75		%
Current Sense Section						
TLEB	Leading edge Blanking Time			250		ns
Zsense	Input impedance			40		kΩ
TD_OC	OCP control delay			120		ns
VTH_OC	OCP threshold			0.9		V
Oscillator Section						
Fosc	Frequency	Oscillation @RI=100K,CS=0,FB=3V	60	65	70	khz
Fosc_BM	Burst mode frequency	Oscillation @RI=100K,CS=0,FB=1.1V		25		khz
Δf_temp	Frequency variation versus temp. Deviation	TEMP = -20 to 85℃		5		%
Δf_VDD	Frequency variation versus VDD	VDD = 12 to 25V		5		%
V_RI_Open	RI open Load Voltage			2		V
RI_range			50	100	150	kΩ
Mosfet Section						
BVdss	MOSFET Drain-Source breakdown voltage		650			V
Ron	Static Drain to Source on resistance				5	Ω

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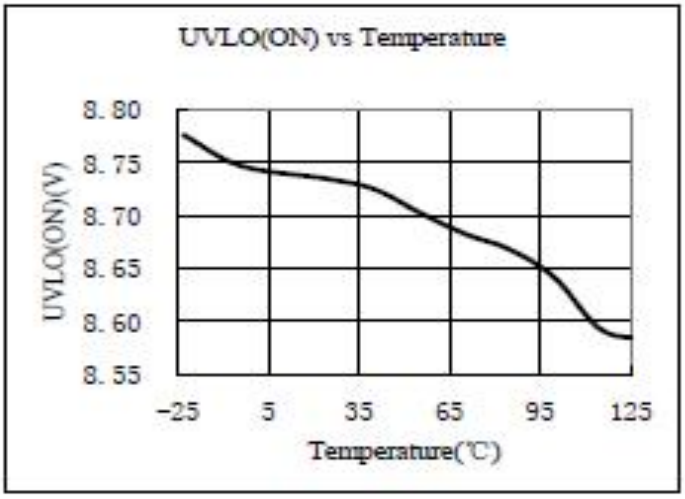
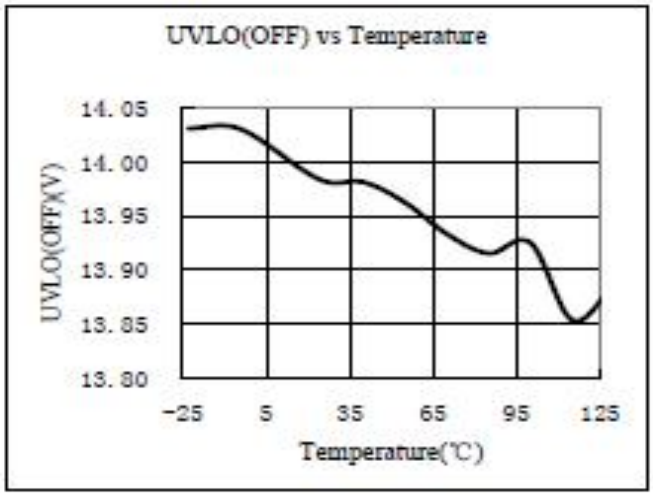
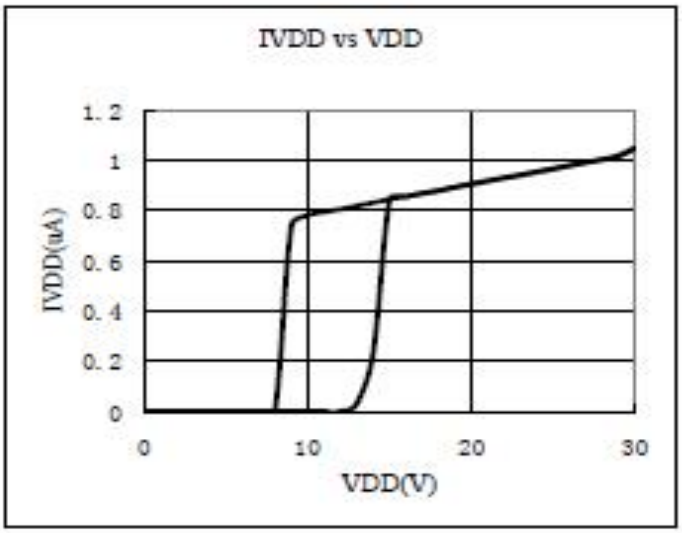
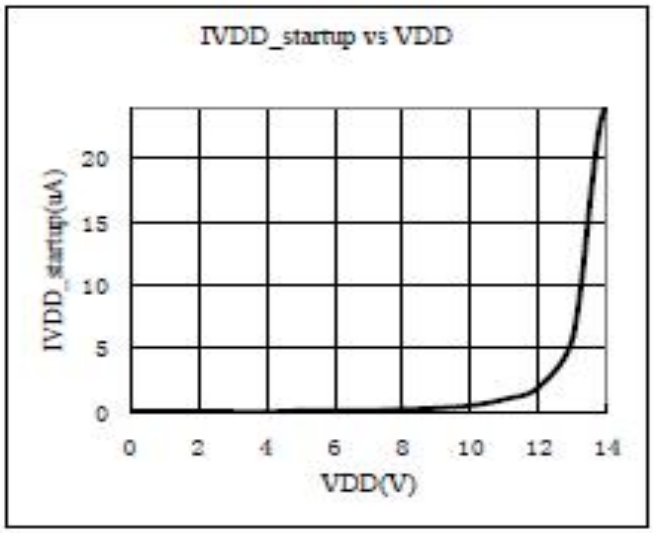
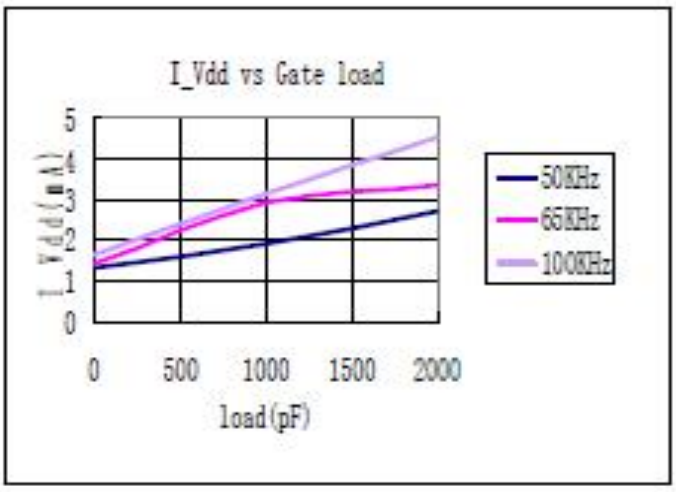
Typical Operating Characteristics

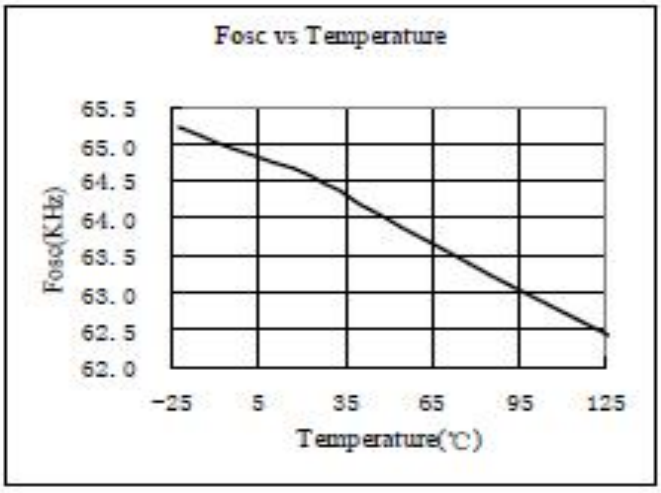












Function Description

L2264 combines a dedicated current mode PWM controller with a high voltage power MOSFET. It is optimized for high performance off-line flyback converter application in sub 18W range. Ultra low startup current and operating current together with burst mode feature minimize the standby power consumption and improve the switching efficiency. In addition to reduce the external component count, the internal synchronous slope compensation combines with the leading-edge blanking improves system large stability and reduces the possible subharmonic oscillation. L2264 also have multiform general recovery protection mode. The main function is described as below:

Startup Current and Startup Control

Startup current of L2264 is designed to be extremely low at 3uA, so that VDD could be charged up above UVLO threshold level and device starts up quickly. A large value startup resistor can therefore be used to minimize the power loss, predigest the design of startup circuit and provides reliable startup in application. For the design of AC/DC adaptor with universal input range, a startup resistor of 2 MΩ, 1/8 W could be used together with a VDD capacitor to provide a fast startup and low power dissipation solution.

Operating Current

The operating current of L2264 is low at 2.3mA. Excellent efficiency is achieved with low operating current together and extended burst mode control circuit.

Extended Burst Mode Operation

At zero load or light load, most of the power dissipation of the switching power supply comes from the MOSFET switching loss, the core loss of the transformer and the loss on the snubber circuit. The magnitude of power loss is in proportion to thenumber of witching events within a period of time. Therefore reducing the switch event leads to reduction on the power loss and thus saving the energy.For the burst mode control circuit, L2264 self adjusts the switching mode according to the loading condition. At the condition of no load or light/medium load, the FB input voltage drops below burst mode threshold level. Device enters Burst Mode control on the basis of the judgment. The gate drive output switches only when VDD voltage drops below a preset level and FB input is active. Otherwise the gate drive remains at off to minimize the switching loss and power consumption to the greatest extend. The frequency control also eliminates the audio noise at any loading conditions.

Oscillator Operation

A resistor connected between RI and GND sets the charge/discharge time of the constant current source to the internal cap and thus the PWM scillator frequency is determined. The relationship between RI and switching frequency follows the below equation within the specified RI in Kohm range at nominal loading operational condition:

$$FOSC = \frac{6500}{RI(Kohm)} (Khz)$$

Current Sensing and Leading Edge Blanking

Cycle-by-Cycle current limiting is offered in L2264.The switch current is detected by a sense resistor into the sense pin. An internal leading edge blanking circuit chops off the sense voltage spike at initial MOSFET on state due to snubber diode reverse recovery so that the external RC filtering on sense input is no longer required. The current limit comparator is disabled and thus cannot turn off the internal MOSFET during the blanking period. PWM duty cycle is determined by the current sense input voltage and the FB input voltage

Internal Synchronized Slope Compensation

Built-in slope compensation circuit adds slope voltage onto the current sense input voltage for PWM generation. This greatly enhances the close loop stability at CCM and prevents possible subharmonic oscillation and thus reduces the output ripple voltage.

Gate Drive

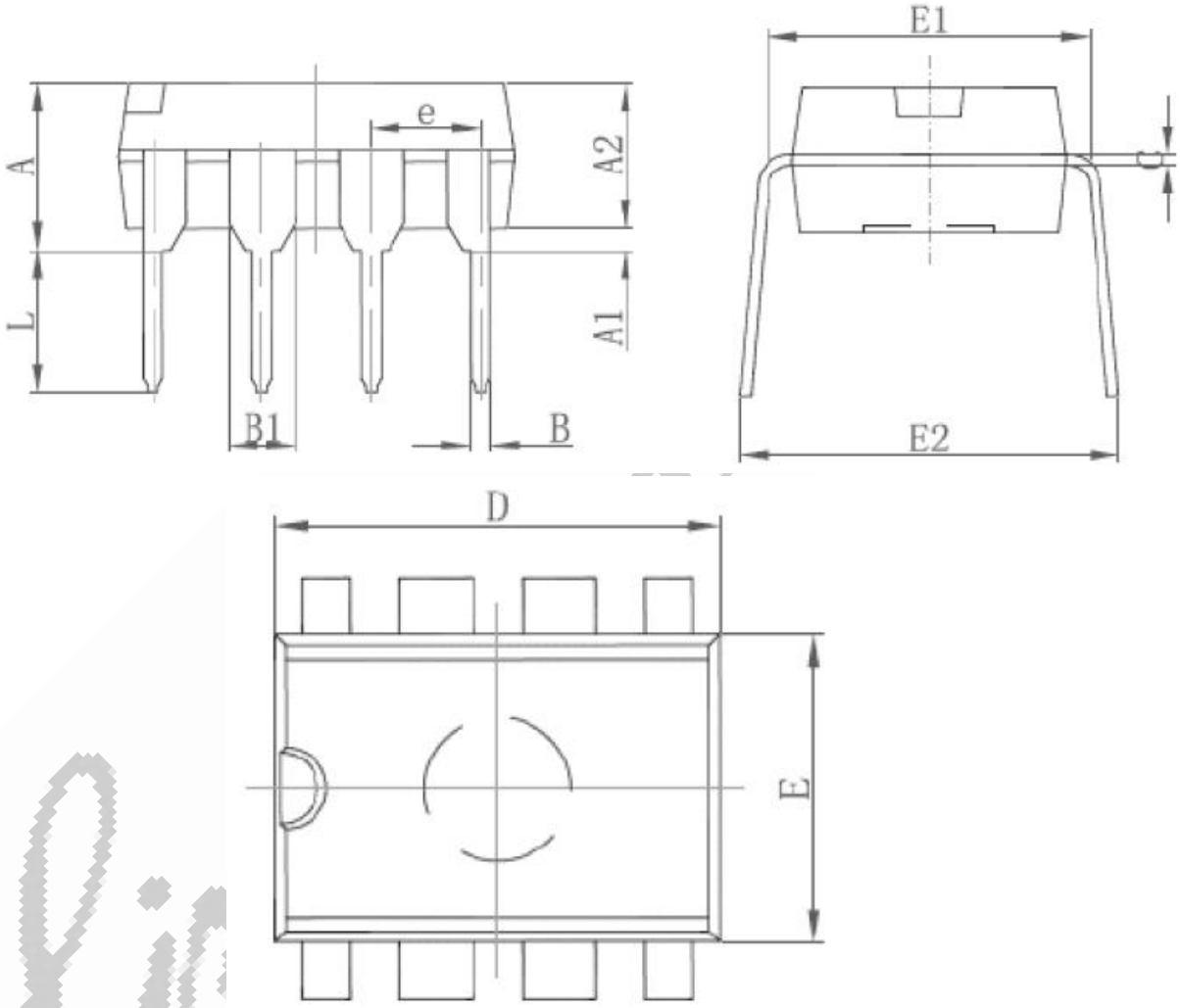
The gate drive strength which is too weak leads to over switch loss of MOSFET while too strong gate drive output compromises in the over EMI. A good tradeoff between output strength and dead time control is achieved through the design of the built-in totem pole gate. The low standby dissipation and good EMI system design is easier to achieve through this dedicated devise. For MOSFET gate protection, an internal 18V clamp is added at higher than expectedVDD input.

Protection Controls

Excellent system stability is achieved by the comprehensive protection of L2264. Including Cycle-by-Cycle current limiting (OCP), Over Load Protection (OLP) and over voltage clamp, Under Voltage Lockout on VDD (UVLO). The average of the PWM signal is detected by the built-in OCP protection circuit effectively. At overload condition when FB input voltage exceeds power limit threshold value for more than TD_PL, control circuit reacts to shut down the output power MOSFET. Device restarts when VDD voltage drops below UVLO limit. It is clamped when VDD is higher than threshold value. The power MOSFET is shut down when VDD drops below UVLO limit and device enters power on start-up sequence thereafter.

Package Information

8 PIN Plastic DIP



Symbol	Dimensions In Milimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	3.710	4.310	0.146	0.170
A1	0.500		0.020	
A2	3.200	3.600	0.126	0.142
B	0.350	0.650	0.014	0.026
B1	1.524(BSC)		0.060(BSC)	
C	0.204	0.360	0.008	0.014
D	9.000	9.500	0.354	0.374
E	6.200	6.600	0.244	0.260
E1	7.320	7.920	0.288	0.312
e	2.540(BSC)		0.100(BSC)	
L	3.000	3.600	0.118	0.142
E2	8.200	9.000	0.323	0.354

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