AK4951A

24bit Stereo CODEC with MIC/HP/SPK-AMP

1. General Description

The AK4951A is a low power 24-bit stereo CODEC with a microphone, headphone and speaker amplifiers.

The AK4951A supports sampling frequency from 8kHz to 48kHz. It is suitable for a wide range of application from speech signal processing for narrowband, wideband and super wideband to sound signal processing for audio band.

The input circuits include a microphone amplifier, an automatic wind noise reduction filter of the proprietary algorithms and a high performance digital ALC (automatic level control) circuit, therefore the AK4951A can record with high-quality sound regardless of whether indoors or outdoors. In addition, the output circuits include a cap-less headphone amplifier with a negative voltage generated by charge pump circuit and a speaker amplifier with 1W output power. It is suitable for various products as well as portable applications with recording/playback function.

The AK4951A are available in a small 32-pin QFN (4mm x 4mm, 0.4mm pitch) package saving mounting area on the board.

Application:

- **IP Camera**
- **Digital Camera**
- **IC Recorder**
- **Tablet**
- **Wireless Headphone**
- **Headset**

2. Features

1. Recording Functions

- **Analog Input: 3 Stereo Single-ended inputs with Selectors**
- **Microphone Amplifier: +30dB ~ 0dB, 3dB Step**
- **Microphone Power Supply: 2.0V or 2.4V, Noise Level= –108dBV**
- **Digital ALC (Automatic Level Control)**
  - Setting Range: +36dB ~ –52.5dB, 0.375dB Step & Mute
- **ADC Performance: S/(N+D): 83dB, DR, S/N: 88dB (MIC-Amp=+18dB)**
  S/(N+D): 85dB, DR, S/N: 96dB (MIC-Amp=0dB)
- **Microphone Sensitivity Correction**
- **Automatic Wind Noise Reduction Filter**
  Selectable voice peak detection mode
- **5-Band Notch Filter: Include Dynamic Gain Control**
- **Stereo Separation Emphasis Circuit**
- **Digital Microphone Interface**

2. **Playback Functions**
   - **Digital ALC (Automatic Level Control)**
     - **Setting Range: +36dB ~ –52.5dB, 0.375dB Step & Mute**
   - **Sidetone Mixer & Volume Control (0dB ~ –18dB, 6dB Step)**
   - **Digital Volume Control**
     - **+12dB ~ –89.5dB, 0.5dB Step & Mute**
   - **Capacitor-less Stereo Headphone Amplifier**
     - **HP-Amplifier Performance: S/(N+D): 75dB@20mW, S/N: 97dB**
     - **Output Power: 20mW@16Ω**
     - **Pop Noise Free at Power-ON/OFF**
   - **Mono Speaker Amplifier (with Stereo Line Output Switch)**
     - **Speaker Amplifier Porformance: S/(N+D): 75dB@250mW, S/N: 99dB**
     - **BTL Output**
     - **Output Power: 400mW@8Ω (SVDD=3.3V), 1W@8Ω (SVDD=5V)**
   - **Analog Mixing: BEEP Input**
3. **Power Management**
4. **Master Clock:**
   (1) PLL Mode
   Frequencies: 11.2896MHz, 12MHz, 12.288MHz, 13.5MHz, 16MH, 24MHz, 27MHz (MCKI pin), 32fs or 64fs (BICK pin)
   (2) External Clock Mode
   Frequencies: 256fs, 384fs, 512fs or 1024fs (MCKI pin)
5. **Sampling Frequencies**
   - **PLL Master Mode:**
     8kHz, 11.025kHz, 12kHz, 16kHz, 22.05kHz, 24kHz, 32kHz, 44.1kHz, 48kHz
   - **PLL Slave Mode (BICK pin): 8kHz ~ 48kHz**
   - **EXT Master/Slave Mode:**
     8kHz ~ 48kHz (256fs, 384fs, 512fs), 8kHz ~ 24kHz (1024fs)
6. **Master/Slave Mode**
7. **Audio Interface Format: MSB First, 2's complement**
   - **ADC: 16/24bit MSB justified, 16/24bit I^2S**
   - **DAC: 16/24bit MSB justified, 16bit LSB justified, 24bit LSB justified, 16/24bit I^2S**
8. **µP I/F: I^2C Bus (Ver 1.0, 400kHz Fast-Mode)**
9. **Ambient Operating Temperature: Ta = –40 ~ 85°C**
10. **Power Supply**
    - **Analog Power Supply (AVDD): 2.8 ~ 3.5V**
    - **Speaker Power Supply (SVDD): 1.8 ~ 5.5V**
    - **Digital & Headphone Power Supply (DVDD): 1.6 ~ 1.98V**
    - **Digital I/O Power Supply (TVDD): 1.6 or (DVDD – 0.2) ~ 3.5V**
11. **Package: 32-pin QFN (4 x 4 mm, 0.4mm pitch)**

3. Table of Contents

4. Block Diagram and Functions

■ Block Diagram

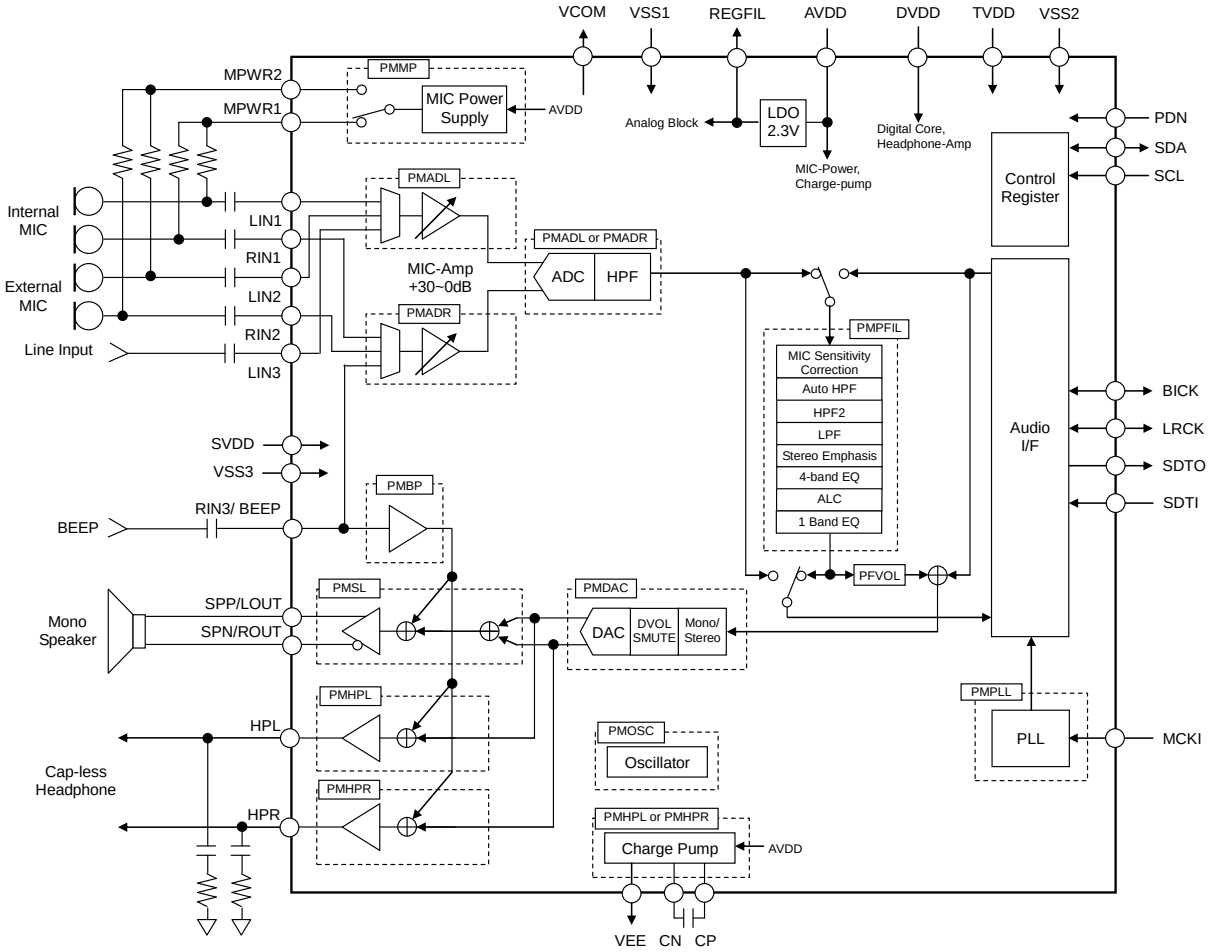


Figure 1. Block Diagram

■ Comparison Table to AK4951

1. Function

Function	AK4951	AK4951A
PLL Mode (MCKI Frequency)	11.2896MHz, 12MHz, 12.288MHz, 13.5MHz, 24MHz, 27MHz	11.2896MHz, 12MHz, 12.288MHz, 13.5MHz, **16MHz**, 24MHz, 27MHz
Automatic Wind Noise Reduction Filter	Voice peak detection mode: **Auto**	Voice peak detection mode: **Selectable**

2. Register Setting

1) PLL Reference Clock Setting

Mode 0 of the PLL mode setting was added from AK4951.

Mode	PLL3 bit	PLL2 bit	PLL1 bit	PLL0 bit	PLL Reference Clock Input Pin	Input Frequency	PLL Lock Time (max)
0	**0**	**0**	**0**	**0**	**MCKI pin**	**16MHz**	**5ms**
2	0	0	1	0	BICK pin	32fs	2ms
3	0	0	1	1	BICK pin	64fs	2ms
4	0	1	0	0	MCKI pin	11.2896MHz	5ms
5	0	1	0	1	MCKI pin	12.288MHz	5ms
6	0	1	1	0	MCKI pin	12MHz	5ms
7	0	1	1	1	MCKI pin	24MHz	5ms
12	1	1	0	0	MCKI pin	13.5MHz	5ms
13	1	1	0	1	MCKI pin	27MHz	5ms
Others	Others				N/A		

2) Automatic Wind Noise Reduction Filter

VODETN bit was added from AK4951.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
03H	Signal Select 2	SPKG1	SPKG0	**VODETN**	MICL	INL1	INL0	INR1	INR0

VODETN: Voice Peak Detection Disable
0: Enable (default)
1: Disable
When AHPF and VODETN bits = “1”, voice peak detection is disable. VODETN bit must be set when PMPFIL bit = “0”.

3) Device Information

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
31H	Device Information	REV3	REV2	REV1	REV0	DVN3	DVN2	DVN1	DVN0

REV3-0: Device Revision ID (Read operation only.)
1100: AK4951
1101: AK4951A

5. Pin Configurations and Functions

■ Pin Layout

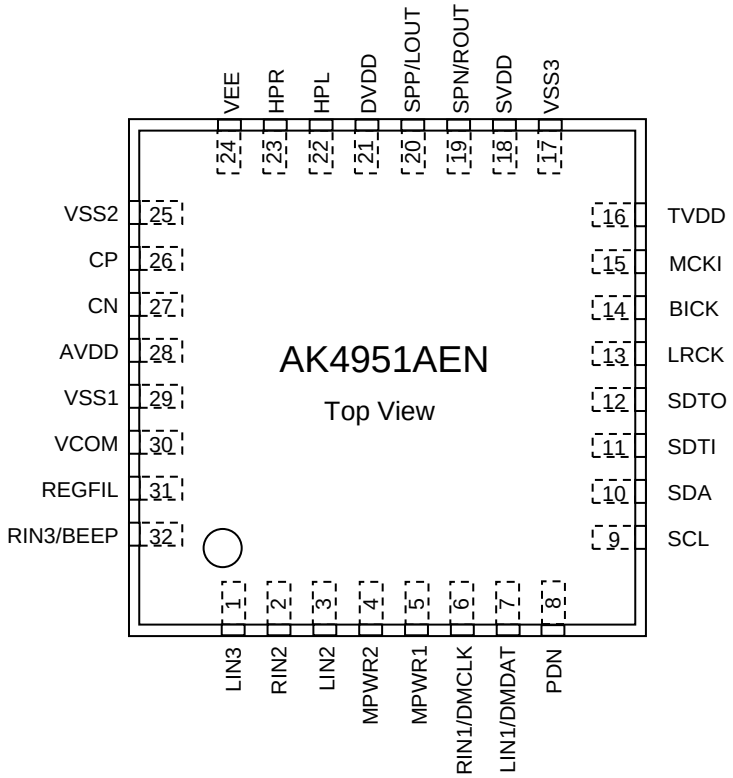


Figure 2. Pin Layout

■ PIN/FUNCTION

No.	Pin Name	I/O	Function	
1	LIN3	I	Lch Analog Input 3 pin	
2	RIN2	I	Rch Analog Input 2 Pin	
3	LIN2	I	Lch Analog Input 2 pin	
4	MPWR2	O	MIC Power Supply 2 Pin	
5	MPWR1	O	MIC Power Supply 1 Pin	
6	RIN1	I	Rch Analog Input 1 Pin	(DMIC bit = “0”: default)
	DMCLK	O	Digital Microphone Clock pin	(DMIC bit = “1”)
7	LIN1	I	Lch Analog Input 1 Pin	(DMIC bit = “0”: default)
	DMDAT	I	Digital Microphone Data Input Pin	(DMIC bit = “1”)
8	PDN	I	Reset & Power-down Pin “L”: Reset & Power-down, “H”: Normal Operation	
9	SCL	I	Control Data Clock Pin	
10	SDA	I/O	Control Data Input/Output Pin	
11	SDTI	I	Audio Serial Data Input Pin	
12	SDTO	O	Audio Serial Data Output Pin	
13	LRCK	I/O	Input/Output Channel Clock Pin	
14	BICK	I/O	Audio Serial Data Clock Pin	
15	MCKI	I	External Master Clock Input Pin	
16	TVDD	-	Digital I/O Power Supply Pin, 1.6 or (DVDD-0.2) ~ 3.5V	
17	VSS3	-	Ground 3 Pin	
18	SVDD	-	Speaker-Amp Power Supply Pin, 1.8 ~ 5.5V	
19	SPN	O	Speaker-Amp Negative Output Pin	(LOSEL bit = “0”: default)
	ROUT	O	Rch Stereo Line Output Pin	(LOSEL bit = “1”)
20	SPP	O	Speaker-Amp Positive Output Pin	(LOSEL bit = “0”: default)
	LOUT	O	Lch Stereo Line Output Pin	(LOSEL bit = “1”)
21	DVDD	-	Digital Power Supply Pin, 1.6 ~ 1.98V	
22	HPL	O	Lch Headphone-Amp Output Pin	
23	HPR	O	Rch Headphone-Amp Output Pin	
24	VEE	O	Charge-Pump Circuit Negative Voltage Output Pin This pin must be connected to VSS2 with 2.2μF±20% capacitor in series.	
25	VSS2	-	Ground 2 Pin	
26	CP	O	Positive Charge-Pump Capacitor Terminal Pin This pin must be connected to CN pin with 2.2μF±20% capacitor in series.	
27	CN	I	Negative Charge-Pump Capacitor Terminal Pin This pin must be connected to CP pin with 2.2μF±20% capacitor in series.	
28	AVDD	-	Analog Power Supply Pin, 2.8 ~ 3.5V	
29	VSS1	-	Ground 1 Pin	
30	VCOM	O	Common Voltage Output Pin Bias voltage of ADC inputs and DAC outputs. This pin must be connected to VSS1 with 2.2F±20% capacitor in series.	
31	REGFIL	O	LDO Voltage Output pin for Analog Block (typ 2.3V) This pin must be connected to VSS1 with 2.2μF±20% capacitor in series.	
32	RIN3	I	Rch Analog Input 3 Pin	(PMBP bit = “0”: default)
	BEEP	I	Beep Signal Input Pin	(PMBP bit = “1”)

Note 1. All input pins except analog input pins (LIN1, RIN1, LIN2, RIN2, LIN3, RIN3/BEEP) must not be allowed to float.

■ Handling of Unused Pin

Unused I/O pins must be processed appropriately as below.

Classification	Pin Name	Setting
Analog	MPWR, SPN, SPP, HPL, HPR, CP, CN, VEE, LIN1/DMDAT, RIN1/DMCLK, LIN2, RIN2, LIN3, RIN3/BEEP	Open
Digital	MCKI, SDTI	Connect to VSS2
	SDTO	Open

6. Absolute Maximum Ratings

(VSS1=VSS2=VSS3=0V; Note 2)

Parameter		Symbol	Min.	Max.	Unit
Power Supplies	Analog	AVDDam	–0.3	6.0	V
	Digital	DVDDam	–0.3	2.5	V
	Digital I/O	TVDDam	–0.3	6.0	V
	Speaker-Amp	SVDDam	–0.3	6.0	V
Input Current, Any Pin Except Supplies		IIN	-	±10	mA
Analog Input Voltage (Note 3)		VINA	–0.3	AVDD+0.3	V
Digital Input Voltage (Note 4)		VIND	–0.3	TVDD+0.3	V
Ambient Operating Temperature (powered applied)		Ta	–40	85	°C
Storage Temperature		Tstg	–65	150	°C
Maximum Power Dissipation (Note 5)		Pd	-	840	mW

Note 2. All voltages are with respect to ground. VSS1, VSS2 and VSS3 must be connected to the same analog ground plane.

Note 3. LIN1, RIN1, LIN2, RIN2, LIN3 and RIN3/BEEP pins

Note 4. PDN, CCLK/SCL, CSN/SDA, CDTIO/CAD0, SDTI, LRCK, BICK and MCKI pins
Pull-up resistors at the SDA and SCL pins must be connected to a voltage in the range from TVDD or more to 6V or less.

Note 5. This power is the AK4951A internal dissipation that does not include power dissipation of externally connected speakers. The maximum junction temperature is 125°C and θja (Junction to Ambient) is 42°C/W at JESD51-9 (2p2s). When Pd =840mW and the θja is 42°C/W, the junction temperature does not exceed 125°C. In this case, the AK4951A will not be damaged by its internal power dissipation. Therefore, the AK4951A should be used in the condition of θja ≤ 42°C/W.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

7. Recommended Operating Conditions

(VSS1=VSS2=VSS3 =0V; Note 2)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Power Supplies (Note 6)	Analog	AVDD	2.8	3.3	3.5	V
	Digital	DVDD	1.6	1.8	1.98	V
	Digital I/O (Note 7)	TVDD	1.6 or (DVDD-0.2)	1.8	3.5	V
	Speaker-Amp	SVDD	1.8	3.3	5.5	V

Note 2. All voltages are with respect to ground.

Note 6. The power-up sequence between AVDD, DVDD, TVDD and SVDD is not critical. The PDN pin must be "L" upon power up, and should be changed to "H" after all power supplies are supplied to avoid an internal circuit error.

Note 7. The minimum value is higher voltage between DVDD-0.2 and 1.6V.

*** When SVDD is powered ON and the PDN pin is "L", AVDD, DVDD and TVDD can be powered ON/OFF. When TVDD is powered ON and the PDN pin is "L", AVDD, DVDD and SVDD can be powered ON/OFF. The PDN pin must be set to "H" after all power supplies are ON, when the AK4951A is powered-up from power-down state.**

* AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

8. Electrical Characteristics

■ Analog Characteristics

(Ta=25°C; AVDD=SVDD=3.3V, TVDD=DVDD=1.8V; VSS1=VSS2=VSS3=0V; fs=48kHz, BICK=64fs; Signal Frequency=1kHz; 24bit Data; Measurement Bandwidth=20Hz ~ 20kHz; unless otherwise specified)

Parameter			Min.	Typ.	Max.	Unit
MIC Amplifier: LIN1, RIN1, LIN2, RIN2, LIN3, RIN3 pins						
Input Resistance			20	30	40	kΩ
Gain	Gain Setting		0	-	+30	dB
	Step Width		-	3	-	dB
MIC Power Supply: MPWR1, MPWR2 pins						
Output Voltage		MICL bit = "0"	2.2	2.4	2.6	V
		MICL bit = "1"	1.8	2.0	2.2	V
Output Noise Level (A-weighted)			-	-108	-	dBV
Load Resistance			1.0	-	-	kΩ
Load Capacitance			-	-	30	pF
PSRR (f = 1kHz) (Note 8)			-	100	-	dB
ADC Analog Input Characteristics: LIN1, RIN1, LIN2, RIN2, LIN3, RIN3 pins → ADC(Programmable Filter = OFF) → SDTO						
Resolution			-	-	24	Bits
Input Voltage (Note 9)		(Note 10)	-	0.261	-	Vpp
		(Note 11)	1.86	2.07	2.28	Vpp
S/(N+D) (-1dBFS)		(Note 10)	73	83	-	dBFS
		(Note 11)	-	85	-	dBFS
D-Range (–60dBFS, A-weighted)		(Note 10)	78	88	-	dB
		(Note 11)	-	96	-	dB
S/N (A-weighted)		(Note 10)	78	88	-	dB
		(Note 11)	-	96	-	dB
Interchannel Isolation		(Note 10)	75	100	-	dB
		(Note 11)	-	110	-	dB
Interchannel Gain Mismatch		(Note 10)	-	0	0.5	dB
		(Note 11)	-	0	0.5	dB
PSRR (f = 1kHz) (Note 8)			-	80	-	dB

Note 8. PSRR applied to AVDD with 500mVpp sine wave.
Note 9. Vin = 0.9 x 2.3Vpp (typ) @MGAIN3-0 bits = "0000" (0dB)
Note 10. MGAIN3-0 bits = "0110" (+18dB)
Note 11. MGAIN3-0 bits = "0000" (0dB)

Parameter			Min.	Typ.	Max.	Unit
DAC Characteristics:						
Resolution			-	-	24	Bits
Headphone-Amp Characteristics: DAC → HPL, HPR pins, ALC=OFF, IVOL=DVOL= 0dB, R_L=16Ω						
Output Voltage (0dBFS)			1.44	1.60	1.76	Vpp
S/(N+D)	R_L=16Ω		50	75	-	dB
	R_L=10kΩ		-	80	-	dB
S/N (A-weighted)			87	97	-	dB
Interchannel Isolation			65	80	-	dB
Interchannel Gain Mismatch			-	0	0.8	dB
Output Offset Voltage			-1	0	+1	mV
Load Resistance			16	-	-	Ω
Load Capacitance			-	-	300	pF
PSRR (f = 1kHz) (Note 12)	AVDD		-	74	-	dB
	DVDD		-	90	-	dB
Speaker-Amp Characteristics: DAC → SPP/SPN pins, ALC=OFF, IVOL=DVOL= 0dB, R_L=8Ω, BTL						
Output Voltage						
SPKG1-0 bits = "00", –0.5dBFS (Po=150mW)			-	3.18	-	Vpp
SPKG1-0 bits = "01", –0.5dBFS (Po=250mW)			3.20	4.00	4.80	Vpp
SPKG1-0 bits = "10", –0.5dBFS (Po=400mW)			-	1.79	-	Vrms
SPKG1-0 bits = "11", –0.5dBFS (Po=1000mW) (SVDD=5V)			-	2.83	-	Vrms
S/(N+D)						
SPKG1-0 bits = "00", –0.5dBFS (Po=150mW)			-	80	-	dB
SPKG1-0 bits = "01", –0.5dBFS (Po=250mW)			40	75	-	dB
SPKG1-0 bits = "10", –0.5dBFS (Po=400mW)			-	20	-	dB
SPKG1-0 bits = "11", –0.5dBFS (Po=1000mW) (SVDD=5V)			-	20	-	dB
S/N (A-weighted)	SPKG1-0 bits = "01"		80	99	-	dB
Output Offset Voltage	SPKG1-0 bits = "01"		-30	0	+30	mV
Load Resistance			8	-	-	Ω
Load Capacitance			-	-	100	pF
PSRR (f = 1kHz) (Note 13)	AVDD		-	80	-	dB
	SVDD		-	60	-	dB
Stereo Line Output Characteristics: DAC → LOUT, ROUT pins, ALC=OFF, IVOL=DVOL = 0dB, R_L=10kΩ, LVCM1-0 bits = "01"						
Output Voltage	(0dBFS)	LVCM0 bit = "0", SVDD=2.8V	-	2.26	-	Vpp
		LVCM0 bit = "1"	-	1.0	-	Vrms
	(-3dBFS)	LVCM0 bit = "0", SVDD=2.8V	1.44	1.6	1.76	Vpp
		LVCM0 bit = "1"	1.82	2.0	2.22	Vpp
S/(N+D)	(0dBFS)	LVCM0 bit = "0", SVDD=2.8V	-	80	-	dB
		LVCM0 bit = "1"	-	80	-	dB
	(-3dBFS)		75	85	-	dB
S/N (A-weighted)			82	94	-	dB
Interchannel Isolation			-	100	-	dB
Interchannel Gain Mismatch			-	0	0.8	dB
Load Resistance			10	-	-	kΩ
Load Capacitance			-	-	30	pF

Note 12. PSRR applied with 500mVpp sine wave.
Note 13. PSRR applied to AVDD or SVDD with 500mVpp sine wave.

Parameter			Min.	Typ.	Max.	Unit
Mono Input: BEEP pin (PMBP bit =“1”, BPVCM bit = “0”, BPLVL3-0 bits = “0000”)						
Input Resistance			46	66	86	kΩ
Maximum Input Voltage (Note 14)			-	-	1.54	Vpp
Gain						
	BEEP pin → HPL, HPR pins		–1	0	+1	dB
	BEEP pin → SPP/SPN pins (Note 15)					
		SPKG1-0 bits = “00”	+4.4	+6.4	+8.4	dB
		SPKG1-0 bits = “01”	-	+8.4	-	dB
		SPKG1-0 bits = “10”	-	+11.1	-	dB
		SPKG1-0 bits = “11”	-	+14.9	-	dB
	BEEP pin → LOUT, ROUT pins					
		LVCM1-0 bits = “00”	-1	0	+1	dB
		LVCM 1-0 bits = “01”	-	+2	-	dB
		LVCM 1-0 bits = “10”	-	+2	-	dB
		LVCM 1-0 bits = “11”	-	+4	-	dB
Power Supplies:						
Power Up (PDN pin = “H”)						
	MIC + ADC + DAC + Headphone out					
		AVDD+DVDD+TVDD (Note 16)	-	6.5	9.8	mA
		AVDD+DVDD+TVDD (Note 17)	-	5.7	-	mA
		SVDD (No Load)	-	36	54	μA
	MIC + ADC + DAC + Speaker out					
		AVDD+DVDD+TVDD (Note 18)	-	5.6	8.4	mA
		AVDD+DVDD+TVDD (Note 19)	-	4.7	-	mA
		SVDD (No Load)	-	1.8	2.7	mA
Power Down (PDN pin = “L”) (Note 20)						
	AVDD+DVDD+TVDD+SVDD		-	0	10	μA
	SVDD (Note 21)		-	0	10	μA

Note 14. The maximum value is AVDD Vpp when BPVCM bit = “1”. However, a click noise may occur when the amplitude after BEEP-Amp is 0.5Vpp or more. (set by BPLVL3-0 bits)

Note 15. The gain is in inverse proportion to external input resistance.

Note 16. When PLL Master Mode (MCKI=12MHz), and PMADL=PMADR=PMDAC=PMPFIL=PMHPL= PMHPR= PMVCM=PMPLL =PMBP=PMMP=M/S bits = “1”. In this case, the MPWR1 (MPWR2) pin outputs 0mA. AVDD= 4.4mA (typ), DVDD= 2.0mA (typ), TVDD= 0.08mA (typ).

Note 17. When EXT Slave Mode (PMPLL=M/S bits =“0”), PMADL=PMADR=PMDAC=PMHPL=PMHPR= PMVCM=PMBP=PMMP bits = “1”, and PMPFIL bit = “0”. In this case, the MPWR1 (MPWR2) pin outputs 0mA. AVDD= 4.2mA (typ), DVDD= 1.5mA (typ), TVDD= 0.02mA (typ).

Note 18. When PLL Master Mode (MCKI=12MHz), and PMADL=PMADR=PMDAC=PMPFIL=PMSL= PMVCM= PMPLL =PMBP=PMMP=SLPSN=DACS=M/S bits = “1”. In this case, the MPWR1 (MPWR2) pin outputs 0mA. AVDD= 3.8mA, DVDD= 1.7mA (typ), TVDD= 0.08mA (typ).

Note 19. When EXT Slave Mode (PMPLL=M/S bits =“0”), PMADL=PMADR=PMDAC=PMSL=PMVCM= PMBP=PMMP=SLPSN=DACS bits = “1”, and PMPFIL bit = “0”. In this case, the MPWR1 (MPWR2) pin outputs 0mA. AVDD= 3.5mA, DVDD= 1.2mA (typ), TVDD= 0.02mA (typ).

Note 20. All digital input pins are fixed to TVDD or VSS2.

Note 21. When AVDD, DVDD and TVDD are powered OFF.

■ Power Consumption on Each Operation Mode

Conditions: Ta=25°C; AVDD=SVDD=3.3V, TVDD=DVDD=1.8V; VSS1=VSS2=VSS3=0V; fs=48kHz, Programmable Filter=OFF, External Slave Mode, BICK=64fs; LIN1/RIN1 input = No signal; SDTI input = No data; Headphone & Speaker outputs = No load.

Table 1. Power Consumption on Each Operation Mode (typ)

Mode	Power Management Bit									AVDD [mA]	DVDD [mA]	TVDD [mA]	SVDD [mA]	Total Power [mW]
	PMVCM	PMSL	PMDAC	PMADL	PMADR	PMHPL	PMHPR	PMPFIL	LOSEL					
All Power-down	0	0	0	0	0	0	0	0	0	0	0	0	0	0
LIN1/RIN1 → ADC	1	0	0	1	1	0	0	0	0	2.40	0.75	0.02	0	9.3
LIN1 (Mono) → ADC	1	0	0	1	0	0	0	0	0	1.62	0.75	0.02	0	6.7
DAC → HP	1	0	1	0	0	1	1	0	0	2.15	0.80	0.02	0	8.6
DAC → SPK	1	1	1	0	0	0	0	0	0	1.50	0.50	0.02	1.80	11.8
DAC → Line out	1	1	1	0	0	0	0	0	1	1.68	0.50	0.02	0.34	7.6
LIN1/RIN1 → ADC & DAC → HP	1	0	1	1	1	1	1	0	0	3.75	1.55	0.02	0	15.2
LIN1/RIN1 → ADC & DAC → SPK	1	1	1	1	1	0	0	0	0	3.10	1.25	0.02	1.80	18.5
LIN1/RIN1 → ADC & DAC → Line out	1	1	1	1	1	0	0	0	1	3.30	1.25	0.02	0.34	14.3

■ Filter Characteristics

(Ta =25°C; fs=48kHz; AVDD=2.8 ~ 3.5V, SVDD=1.8 ~ 5.5V, DVDD = 1.6 ~ 1.98V, TVDD = 1.6 or (DVDD-0.2)~ 3.5V)

Parameter		Symbol	Min.	Typ.	Max.	Unit
ADC Digital Filter (Decimation LPF):						
Passband (Note 22)	±0.16dB	PB	0	-	18.8	kHz
	−0.66dB		-	21.1	-	kHz
	−1.1dB		-	21.7	-	kHz
	−6.9dB		-	24.1	-	kHz
Stopband (Note 22)		SB	28.4	-	-	kHz
Passband Ripple		PR	-	-	±0.16	dB
Stopband Attenuation		SA	73	-	-	dB
Group Delay (Note 23)		GD	-	17	-	1/fs
Group Delay Distortion		ΔGD	-	0	-	μs
ADC Digital Filter (HPF): HPFC1-0 bits = "00"						
Frequency Response	−3.0dB	FR	-	3.7	-	Hz
(Note 22)	−0.5dB		-	10.9	-	Hz
	−0.1dB		-	23.9	-	Hz
DAC Digital Filter (LPF):						
Passband (Note 22)	±0.05dB	PB	0	-	21.8	kHz
	−6.0dB		-	24	-	kHz
Stopband (Note 22)		SB	27.0	-	-	kHz
Passband Ripple		PR	-	-	±0.05	dB
Stopband Attenuation		SA	70	-	-	dB
Group Delay (Note 23)		GD	-	29	-	1/fs
DAC Digital Filter (LPF) + SCF:						
Frequency Response: 0 ~ 20.0kHz		FR	-	±1.0	-	dB

Note 22. The passband and stopband frequencies scale with fs (sampling frequency).

Note 23. A calculating delay time which is induced by digital filtering. This time is from the input of an analog signal to the setting of 24-bit data of both channels to the ADC output register. For the DAC, this time is from setting the 24-bit data of a channel from the input register to the output of analog signal. For the signal through the programmable filters (Microphone Sensitivity Correction + Automatic Wind Noise Reduction Filter + 1st order HPF + 1st order LPF + Stereo Separation Emphasis + 4-band Equalizer + ALC + 1-band Equalizer), the group delay is increased by 4/fs from the value above in both recording and playback modes if there is no phase change by the IIR filter.

■ DC Characteristics

(Ta =25°C; fs=48kHz; AVDD=2.8 ~ 3.5V, SVDD= 1.8 ~ 5.5V, DVDD = 1.6 ~ 1.98V, TVDD = 1.6 or (DVDD-0.2) ~ 3.5V)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Audio Interface & Serial µP Interface (CDTIO/CAD0, CSN/SDA, CCLK/SCL, I2C, PDN, BICK, LRCK, SDTI, MCKI pins)						
High-Level Input Voltage	(TVDD ≥ 2.2V)	VIH	70%TVDD	-	-	V
	(TVDD < 2.2V)	VIH	80%TVDD	-	-	V
Low-Level Input Voltage	(TVDD ≥ 2.2V)	VIL	-	-	30%TVDD	V
	(TVDD < 2.2V)	VIL	-	-	20%TVDD	V
Input Leakage Current		Iin1	-	-	±10	µA
Audio Interface & Serial µP Interface (CDTIO, SDA, BICK, LRCK, SDTO pins Output)						
High-Level Output Voltage	(Iout = −80µA)	VOH	TVDD−0.2	-	-	V
Low-Level Output Voltage						
(Except SDA pin : Iout = 80µA)		VOL1	-	-	0.2	V
(SDA pin, 2.0V ≤ TVDD ≤ 3.5V: Iout = 3mA)		VOL2	-	-	0.4	V
(SDA pin, 1.6V ≤ TVDD < 2.0V: Iout = 3mA)		VOL2	-	-	20%TVDD	V
Digital Microphone Interface (DMDAT pin Input; DMIC bit = "1")						
High-Level Input Voltage		VIH2	65%AVDD	-	-	V
Low-Level Input Voltage		VIL2	-	-	35%AVDD	V
Input Leakage Current		Iin2	-	-	±10	µA
Digital Microphone Interface (DMCLK pin Output; DMIC bit = "1")						
High-Level Output Voltage	(Iout=−80µA)	VOH3	AVDD-0.4	-	-	V
Low-Level Output Voltage	(Iout= 80µA)	VOL3	-	-	0.4	V

■ Switching Characteristics

(Ta=25°C; fs=48kHz; C_L=20pF; AVDD=2.8~3.5V, SVDD=1.8~5.5V, DVDD=1.6~1.98V, TVDD=1.6 or (DVDD-0.2)~3.5V)

Parameter		Symbol	Min.	Typ.	Max.	Unit
PLL Master Mode (PLL Reference Clock = MCKI pin)						
MCKI Input Timing						
Frequency	PLL3-0 bits = "0100"	fCLK	-	11.2896	-	MHz
	PLL3-0 bits = "0101"	fCLK	-	12.288	-	MHz
	PLL3-0 bits = "0110"	fCLK	-	12	-	MHz
	PLL3-0 bits = "0111"	fCLK	-	24	-	MHz
	PLL3-0 bits = "1100"	fCLK	-	13.5	-	MHz
	PLL3-0 bits = "1101"	fCLK	-	27	-	MHz
Pulse Width Low		tCLKL	0.4/fCLK	-	-	s
Pulse Width High		tCLKH	0.4/fCLK	-	-	s
LRCK Output Timing						
Frequency		fs	-	Table 7	-	Hz
Duty Cycle		Duty	-	50	-	%
BICK Output Timing						
Frequency	BCKO bit = "0"	fBCK	-	32fs	-	Hz
	BCKO bit = "1"	fBCK	-	64fs	-	Hz
Duty Cycle		dBCK	-	50	-	%
PLL Slave Mode (PLL Reference Clock = BICK pin)						
LRCK Input Timing						
Frequency	PLL3-0 bits = "0010"	fs	-	fBCK/32	-	Hz
	PLL3-0 bits = "0011"	fs	-	fBCK/64	-	Hz
Duty		Duty	45	-	55	%
BICK Input Timing						
Frequency	PLL3-0 bits = "0010"	fBCK	0.256	-	1.536	MHz
	PLL3-0 bits = "0011"	fBCK	0.512	-	3.072	MHz
Pulse Width Low		tBCKL	0.4/fBCK	-	-	s
Pulse Width High		tBCKH	0.4/fBCK	-	-	s
External Slave Mode						
MCKI Input Timing						
Frequency	CM1-0 bits = "00"	fCLK	-	256fs	-	Hz
	CM1-0 bits = "01"	fCLK	-	384fs	-	Hz
	CM1-0 bits = "10"	fCLK	-	512fs	-	Hz
	CM1-0 bits = "11"	fCLK	-	1024fs	-	Hz
Pulse Width Low		tCLKL	0.4/fCLK	-	-	s
Pulse Width High		tCLKH	0.4/fCLK	-	-	s
LRCK Input Timing						
Frequency	CM1-0 bits = "00"	fs	8	-	48	kHz
	CM1-0 bits = "01"	fs	8	-	48	kHz
	CM1-0 bits = "10"	fs	8	-	48	kHz
	CM1-0 bits = "11"	fs	8	-	24	kHz
Duty		Duty	45	-	55	%
BICK Input Timing						
Frequency		fBCK	32fs	-	64fs	Hz
Pulse Width Low		tBCKL	130	-	-	ns
Pulse Width High		tBCKH	130	-	-	ns

Parameter		Symbol	Min.	Typ.	Max.	Unit
External Master Mode						
MCKI Input Timing						
Frequency	256fs	fCLK	2.048	-	12.288	MHz
	384fs	fCLK	3.072	-	18.432	MHz
	512fs	fCLK	4.096	-	24.576	MHz
	1024fs	fCLK	8.192	-	24.576	MHz
Pulse Width Low		tCLKL	0.4/fCLK	-	-	s
Pulse Width High		tCLKH	0.4/fCLK	-	-	s
LRCK Output Timing						
Frequency	CM1-0 bits = "00"	fs	-	fCLK/256	-	Hz
	CM1-0 bits = "01"	fs	-	fCLK/384	-	Hz
	CM1-0 bits = "10"	fs	-	fCLK/512	-	Hz
	CM1-0 bits = "11"	fs	-	fCLK/1024	-	Hz
Duty Cycle		Duty	-	50	-	%
BICK Output Timing						
Frequency	BCKO bit = "0"	fBCK	-	32fs	-	Hz
	BCKO bit = "1"	fBCK	-	64fs	-	Hz
Duty Cycle		dBCK	-	50	-	%
Audio Interface Timing						
Master Mode						
BICK "↓" to LRCK Edge (Note 24)		tBLR	−40	-	40	ns
LRCK Edge to SDTO (MSB) (Except I^{2}S mode)		tLRD	−70	-	70	ns
BICK "↓" to SDTO		tBSD	−70	-	70	ns
SDTI Hold Time		tSDH	50	-	-	ns
SDTI Setup Time		tSDS	50	-	-	ns
Slave Mode						
LRCK Edge to BICK "↑" (Note 24)		tLRB	50	-	-	ns
BICK "↑" to LRCK Edge (Note 24)		tBLR	50	-	-	ns
LRCK Edge to SDTO (MSB) (Except I^{2}S mode)		tLRD	-	-	80	ns
BICK "↓" to SDTO		tBSD	-	-	80	ns
SDTI Hold Time		tSDH	50	-	-	ns
SDTI Setup Time		tSDS	50	-	-	ns
Digital Audio Interface Timing; C_L=100pF						
DMCLK Output Timing						
Period		tSCK	-	1/(64fs)	-	s
Rising Time		tSRise	-	-	10	ns
Falling Time		tSFall	-	-	10	ns
Duty Cycle		dSCK	40	50	60	%
Audio Interface Timing						
DMDAT Setup Time		tDSDS	50	-	-	ns
DMDAT Hold Time		tDSDH	0	-	-	ns

Note 24. BICK rising edge must not occur at the same time as LRCK edge.

Parameter	Symbol	Min.	Typ.	Max.	Unit
Control Interface Timing (I^2C Bus)					
SCL Clock Frequency	fSCL	-	-	400	kHz
Bus Free Time Between Transmissions	tBUF	1.3	-	-	μs
Start Condition Hold Time (prior to first clock pulse)	tHD:STA	0.6	-	-	μs
Clock Low Time	tLOW	1.3	-	-	μs
Clock High Time	tHIGH	0.6	-	-	μs
Setup Time for Repeated Start Condition	tSU:STA	0.6	-	-	μs
SDA Hold Time from SCL Falling (Note 26)	tHD:DAT	0	-	-	μs
SDA Setup Time from SCL Rising	tSU:DAT	0.1	-	-	μs
Rise Time of Both SDA and SCL Lines	tR	-	-	0.3	μs
Fall Time of Both SDA and SCL Lines	tF	-	-	0.3	μs
Setup Time for Stop Condition	tSU:STO	0.6	-	-	μs
Capacitive Load on Bus	Cb	-	-	400	pF
Pulse Width of Spike Noise Suppressed by Input Filter	tSP	0	-	50	ns
Power-down & Reset Timing					
PDN Accept Pulse Width (Note 29)	tAPD	200	-	-	ns
PDN Reject Pulse Width (Note 29)	tRPD	-	-	50	ns
PMADL or PMADR "↑" to SDTO valid (Note 30)					
ADRST1-0 bits ="00"	tPDV	-	1059	-	1/fs
ADRST1-0 bits ="01"	tPDV	-	267	-	1/fs
ADRST1-0 bits ="10"	tPDV	-	531	-	1/fs
ADRST1-0 bits ="11"	tPDV	-	135	-	1/fs
VCOM Voltage					
Rising Time (Note 31)	tRVCM	-	0.6	2.0	ms

Note 25. I^2C Bus is a trademark of NXP B.V.
Note 26. Data must be held for sufficient time to bridge the 300ns transition time of SCL.
Note 27. CCLK rising edge must not occur at the same time as CSN edge.
Note 28. It is the time of 10% potential change of the CDTIO pin when R_L = 1kΩ (pull-up or TVDD).
Note 29. The AK4951A can be reset by the PDN pin = "L". The PDN pin must be held "L" for more than 200ns for a certain reset. The AK4951A is not reset by the "L" pulse less than 50ns.
Note 30. This is the count of LRCK "↑" from the PMADL or PMADR bit = "1".
Note 31. All analog blocks including PLL block are powered up after the VCOM voltage (VCOM pin) rises up. An external capacitor of the VCOM pin is 2.2μF and the REGFIL pin is 2.2μF. The capacitance variation should be ±50%.

■ Timing Diagram

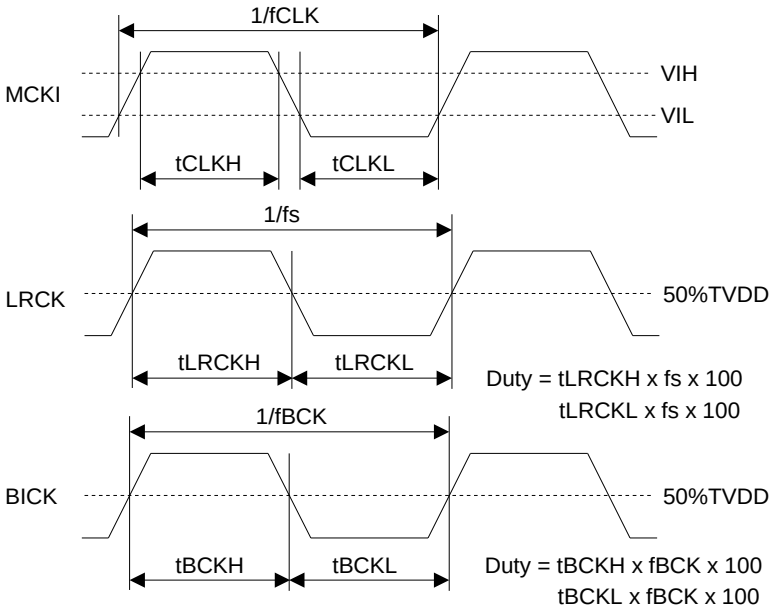


Figure 3. Clock Timing (PLL/EXT Master mode)

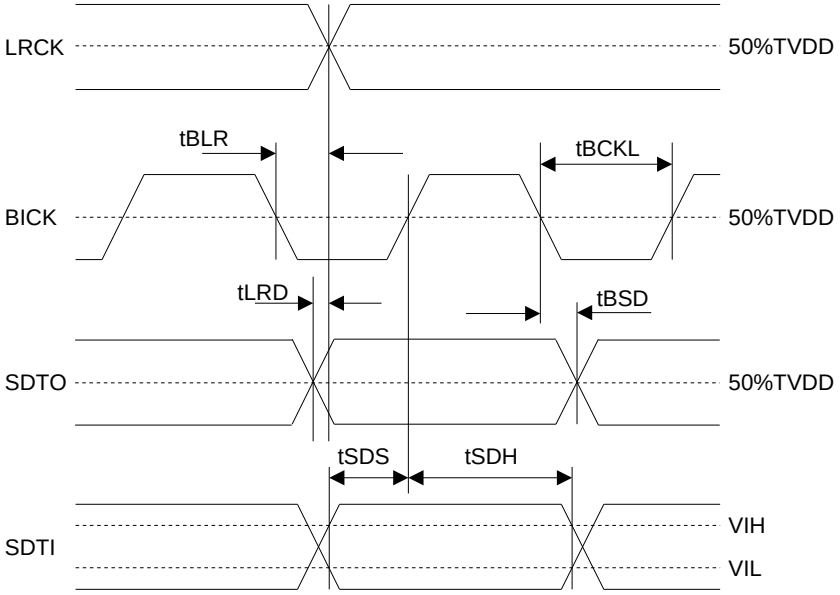


Figure 4. Audio Interface Timing (PLL/EXT Master mode)

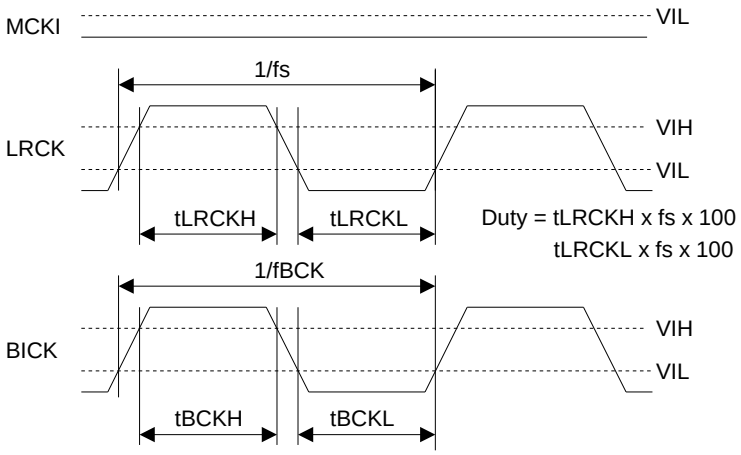


Figure 5. Clock Timing (PLL Slave mode)

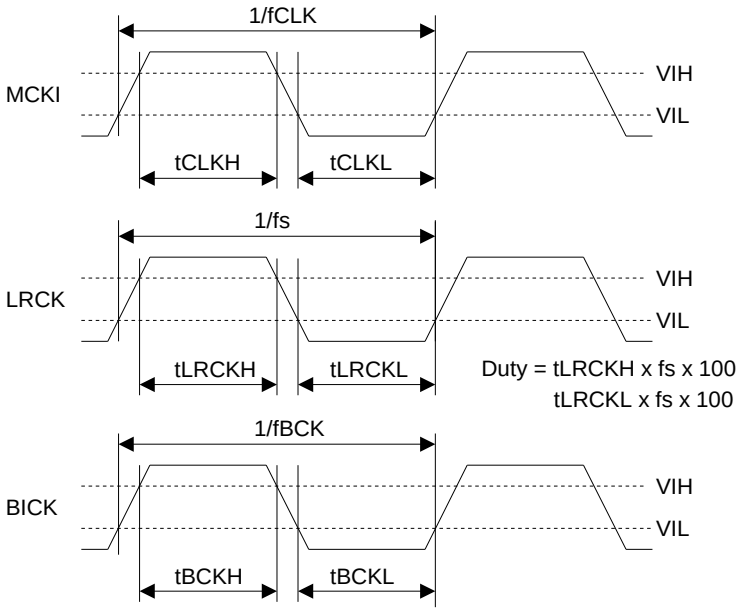


Figure 6. Clock Timing (EXT Slave mode)

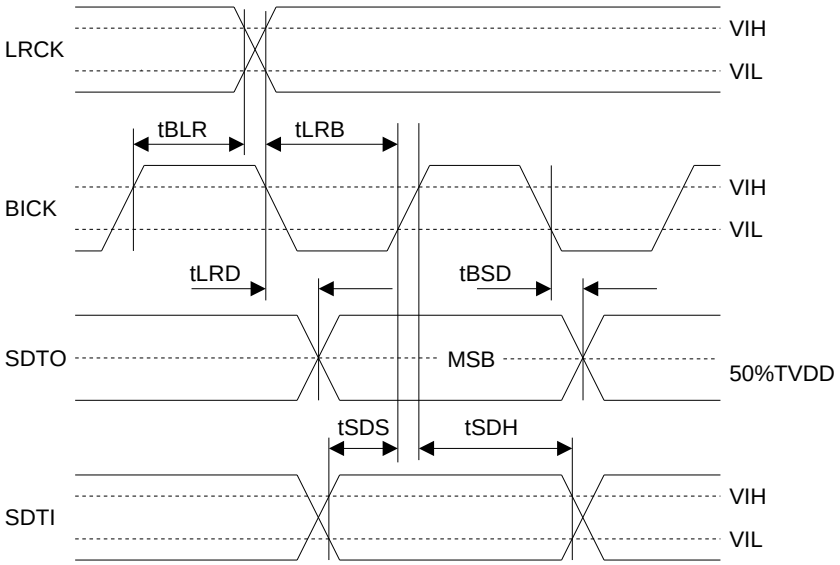
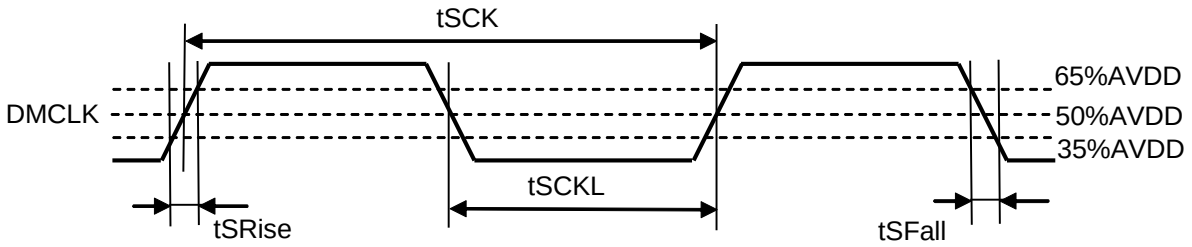


Figure 7. Audio Interface Timing (PLL/EXT Slave mode)



dSCK = 100 x tSCKL / tSCK

Figure 8. DMCLK Clock Timing

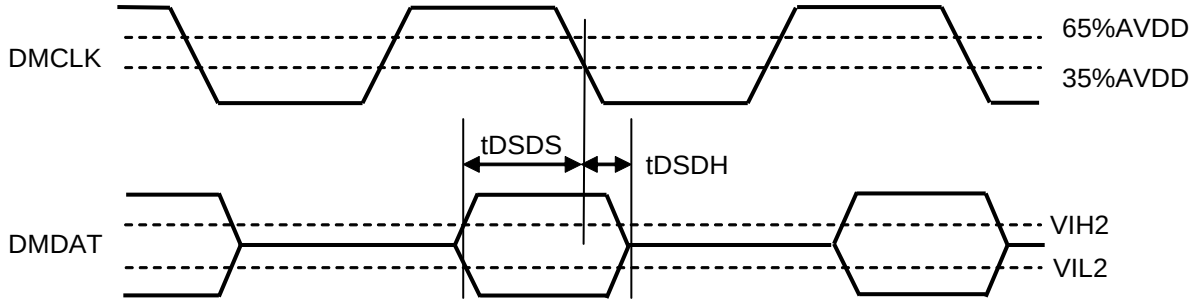


Figure 9. Audio Interface Timing (DCLKP bit = "1")

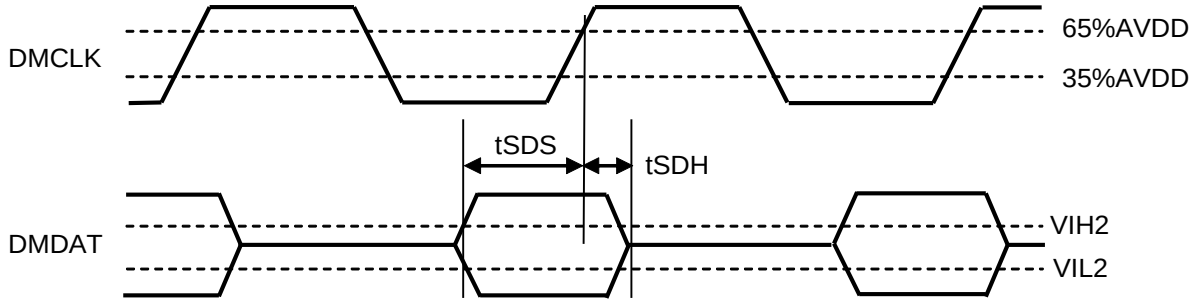


Figure 10. Audio Interface Timing (DCLKP bit = "0")

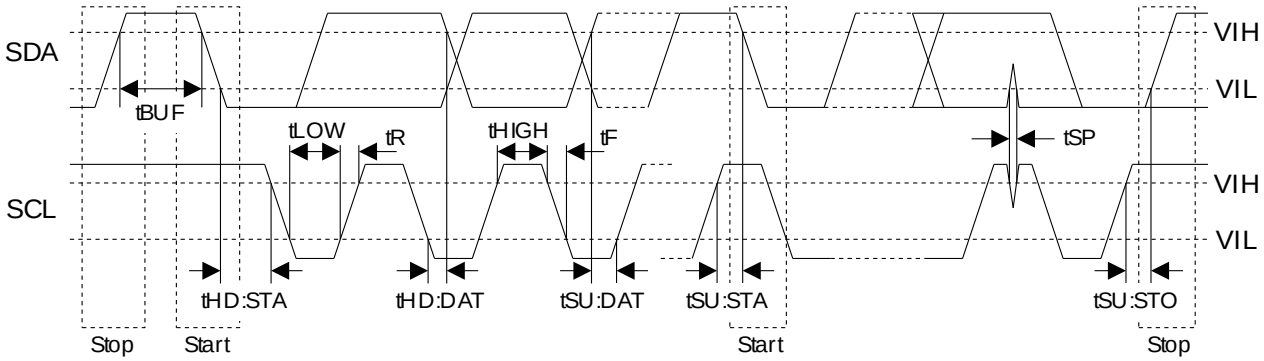


Figure 11. I^2C Bus Mode Timing

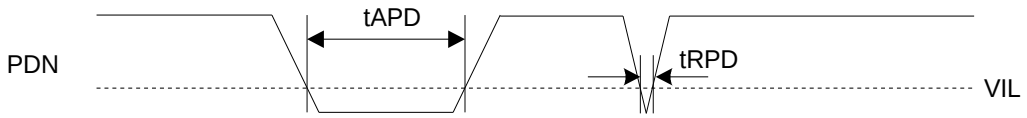


Figure 12. Power Down & Reset Timing 1

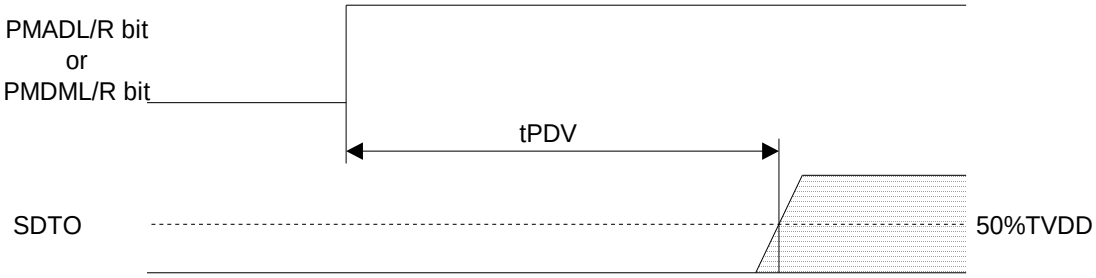


Figure 13. Power Down & Reset Timing 2

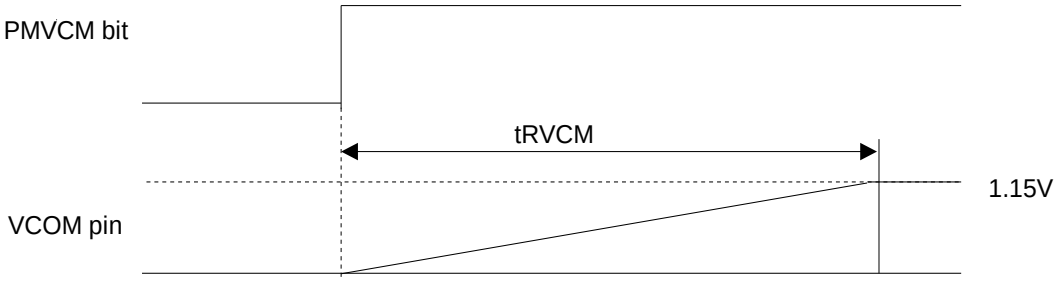


Figure 14. VCOM Rising Timing

9. Functional Descriptions

■ System Clock

There are the following four clock modes to interface with external devices (Table 2, Table 3).

Table 2. Clock Mode Setting

Mode	PMPLL bit	M/S bit	PLL3-0 bits	Figure
PLL Master Mode	1	1	Table 5	Figure 15
PLL Slave Mode (PLL Reference Clock: BICK pin)	1	0	Table 5	Figure 16
EXT Slave Mode	0	0	x	Figure 17
EXT Master Mode	0	1	x	Figure 18

(x: Do not care)

Table 3. Clock pins state in Clock Mode

Mode	MCKI pin	BICK pin	LRCK pin
PLL Master Mode	Input Frequency of Table 5 (Selected by PLL3-0 bits)	Output (Selected by BCKO bit)	Output (1fs)
PLL Slave Mode (PLL Reference Clock: BICK pin)	GND	Input (Selected by PLL3-0 bits)	Input (1fs)
EXT Slave Mode	Input Frequency of Table 11 (Selected by CM1-0 bits)	Input (≥ 32fs)	Input (1fs)
EXT Master Mode	Input Frequency of Table 14 (Selected by CM1-0 bits)	Output (Selected by BCKO bit)	Output (1fs)

■ Master Mode/Slave Mode

The M/S bit selects either master or slave mode. M/S bit = “1” selects master mode and “0” selects slave mode. When the AK4951A is in power-down mode (PDN pin = “L”) and when exits reset state, the AK4951A is in slave mode. After exiting reset state, the AK4951A goes to master mode by changing M/S bit to “1”.

When the AK4951A is in master mode, the LRCK and BICK pins are a floating state until M/S bit becomes “1”. The LRCK and BICK pins of the AK4951A must be pulled-down or pulled-up by a resistor (about 100kΩ) externally to avoid the floating state.

Table 4. Select Master/Slave Mode

M/S bit	Mode	
0	Slave Mode	(default)
1	Master Mode	

■ PLL Mode

When PMPLL bit is “1”, a fully integrated analog phase locked loop (PLL) circuit generates a clock that is selected by PLL3-0 and FS3-0 bits. The PLL lock times, when the AK4951A is supplied stable clocks after PLL is powered-up (PMPLL bit = “0” → “1”) or the sampling frequency is changed, are shown in Table 5.

1) PLL Mode Reference Clock Setting

Table 5. PLL Mode Setting

Mode	PLL3 bit	PLL2 bit	PLL1 bit	PLL0 bit	PLL Reference Clock Input Pin	Input Frequency	PLL Lock Time (max)	
0	0	0	0	0	MCKI pin	16MHz	5ms	
2	0	0	1	0	BICK pin	32fs	2ms	
3	0	0	1	1	BICK pin	64fs	2ms	
4	0	1	0	0	MCKI pin	11.2896MHz	5ms	
5	0	1	0	1	MCKI pin	12.288MHz	5ms	(default)
6	0	1	1	0	MCKI pin	12MHz	5ms	
7	0	1	1	1	MCKI pin	24MHz	5ms	
12	1	1	0	0	MCKI pin	13.5MHz	5ms	
13	1	1	0	1	MCKI pin	27MHz	5ms	
Others	Others				N/A			

(*fs: Sampling Frequency, N/A: Not Available)

2) Setting of sampling frequency in PLL Mode (PLL reference clock input pin = MCKI pin)
When PLL reference clock input is MCKI pin, the sampling frequency is selected by FS3-0 bits as defined in Table 6.

Table 6. Setting of Sampling Frequency (Reference Clock = MCKI pin)

Mode	FS3 bit	FS2 bit	FS1 bit	FS0 bit	Sampling Frequency (Note 32)	
0	0	0	0	0	8kHz mode	
1	0	0	0	1	12kHz mode	
2	0	0	1	0	16kHz mode	
5	0	1	0	1	11.025kHz mode	
7	0	1	1	1	22.05kHz mode	
9	1	0	0	1	24kHz mode	
10	1	0	1	0	32kHz mode	
11	1	0	1	1	48kHz mode	(default)
15	1	1	1	1	44.1kHz mode	
Others	Others				N/A	

(N/A: Not Available)

Note 32. When the MCKI pin is the PLL reference clock input, the sampling frequency generated by PLL differs from the sampling frequency of mode name in some combinations of MCKI frequency(PLL3-0 bits) and sampling frequency (FS3-0 bits). Refer to Table 7 for the details of sampling frequency. In master mode, LRCK and BICK output frequency correspond to sampling frequencies shown in Table 7.

Table 7. Sampling Frequency at PLL mode (Reference clock is MCKI) (1)

Input Frequency MCKI[MHz]	Sampling Frequency Mode	Sampling Frequency generated by PLL [kHz] (Note 33)
12	8kHz mode	8.000000
	12kHz mode	12.000000
	16kHz mode	16.000000
	24kHz mode	24.000000
	32kHz mode	32.000000
	48kHz mode	48.000000
	11.025kHz mode	11.024877
	22.05kHz mode	22.049753
	44.1kHz mode	44.099507
24	8kHz mode	8.000000
	12kHz mode	12.000000
	16kHz mode	16.000000
	24kHz mode	24.000000
	32kHz mode	32.000000
	48kHz mode	48.000000
	11.025kHz mode	11.024877
	22.05kHz mode	22.049753
	44.1kHz mode	44.099507
13.5	8kHz mode	8.000300
	12kHz mode	12.000451
	16kHz mode	16.000601
	24kHz mode	24.000901
	32kHz mode	32.001202
	48kHz mode	48.001803
	11.025kHz mode	11.025218
	22.05kHz mode	22.050436
	44.1kHz mode	44.100871
27	8kHz mode	8.000300
	12kHz mode	12.000451
	16kHz mode	16.000601
	24kHz mode	24.000901
	32kHz mode	32.001202
	48kHz mode	48.001803
	11.025kHz mode	11.025218
	22.05kHz mode	22.050436
	44.1kHz mode	44.100871
11.2896	8kHz mode	8.000000
	12kHz mode	12.000000
	16kHz mode	16.000000
	24kHz mode	24.000000
	32kHz mode	32.000000
	48kHz mode	48.000000
	11.025kHz mode	Note 34
	22.05kHz mode	Note 34
	44.1kHz mode	Note 34

Sampling frequency that differs from sampling frequency of mode name

Note 33. These values are rounded off to six decimal places.
Note 34. The AK4951A must be in EXT master mode when selecting this mode.

Table 7. Sampling Frequency at PLL mode (Reference clock is MCKI) (2)

Input Frequency MCKI[MHz]	Sampling Frequency Mode	Sampling Frequency generated by PLL [kHz] (Note 33)
12.288	8kHz mode	8.000000
	12kHz mode	Note 34
	16kHz mode	16.000000
	24kHz mode	Note 34
	32kHz mode	32.000000
	48kHz mode	Note 34
	11.025kHz mode	11.025000
	22.05kHz mode	22.050000
	44.1kHz mode	44.100000
16	8kHz mode	8.000000
	12kHz mode	12.000000
	16kHz mode	16.000000
	24kHz mode	24.000000
	32kHz mode	32.000000
	48kHz mode	48.000000
	11.025kHz mode	11.024877
	22.05kHz mode	22.049753
	44.1kHz mode	44.099507
	Sampling frequency that differs from sampling frequency of mode name	

Note 33. These values are rounded off to six decimal places.
Note 34. The AK4951A must be in EXT master mode when selecting this mode.

3) Setting of sampling frequency in PLL Mode (PLL reference clock input pin = BICK pin)
When PLL reference clock input is BICK pin, the sampling frequency is selected by FS3-0 bits as defined in Table 8.

Table 8. Setting of Sampling Frequency (Reference Clock = BICK pin)

Mode	FS3 bit	FS2 bit	FS1 bit	FS0 bit	Sampling Frequency (Note 35)	
0	0	0	0	0	8kHz mode	
1	0	0	0	1	12kHz mode	
2	0	0	1	0	11.025kHz mode	
5	0	1	0	1	16kHz mode	
6	0	1	1	0	24kHz mode	
7	0	1	1	1	22.05kHz mode	
8	1	0	0	0	44.1kHz mode	
10	1	0	1	0	32kHz mode	
11	1	0	1	1	48kHz mode	(default)
Others	Others				N/A	

(N/A: Not Available)

Note 35. **Please note that the setting of the FS3-0 bits (Sampling Frequency) is different from the other modes, when the BICK pin is the PLL reference clock input.** The sampling frequency generated by PLL is the same sampling frequency of mode name.

■ PLL Unlock State

In this mode, LRCK and BICK pins go to “L” until the PLL goes to lock state after PMPLL bit = “0” → “1” (Table 9).

After the PLL is locked, a first period of LRCK and BICK may be invalid clock, but these clocks return to normal state after a period of 1/fs.

The BICK and LRCK pins do not output invalid clocks such as PLL unlock state by setting PMPLL bit to “0”. During PMPLL bit = “0”, these pins output the same clock as EXT master mode.

Table 9. Clock Operation at PLL Master Mode (PMPLL bit = “1”, M/S bit = “1”)

PLL State	BICK pin	LRCK pin
After PMPLL bit “0” → “1”	“L” Output	“L” Output
PLL Unlock (except the case above)	Invalid	Invalid
PLL Lock	Table 10	1fs Output

■ PLL Master Mode (PMPLL bit = "1", M/S bit = "1")

When an external clock (11.2896MHz, 12MHz, 12.288MHz, 13.5MHz, 16MHz, 24MHz or 27MHz) is input to the MCKI pin, the internal PLL circuit generates BICK and LRCK clocks. When the state of AK4951A is ADC power-down or Loopback mode, the output of BICK, LRCK and SDTO pins can be stopped by CKOFF bit. When CKOFF bit = "1", BICK, LRCK and SDTO pins output "L". The BICK output frequency is selected between 32fs or 64fs, by BCKO bit (Table 10).

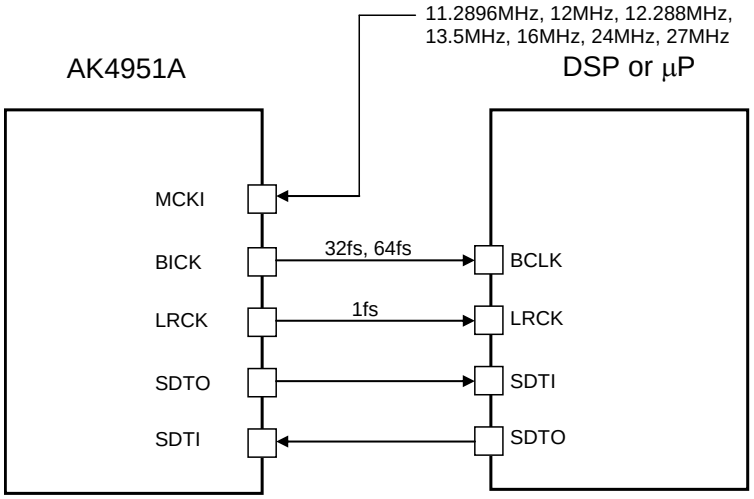


Figure 15. PLL Master Mode

Table 10. BICK Output Frequency at Master Mode

BCKO bit	BICK Output Frequency	
0	32fs	(default)
1	64fs	

■ PLL Slave Mode (PMPLL bit = "1", M/S bit = "0")

A reference clock of PLL is selected among the input clocks to the BICK pin. The required clock for the AK4951A is generated by an internal PLL circuit. Input frequency is selected by PLL3-0 bits (Table 5).

The BICK and LRCK inputs must be synchronized. The sampling frequency can be selected by FS3-0 bits (Table 6).

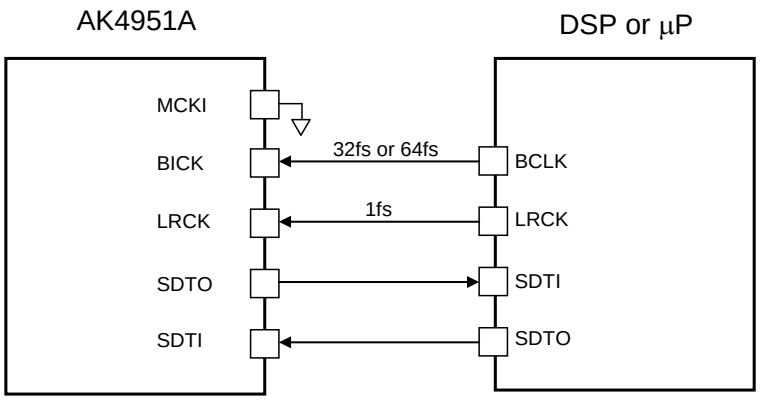


Figure 16. PLL Slave Mode (PLL Reference Clock: BICK pin)

■ EXT Slave Mode (PMPLL bit = "0", M/S bit = "0")

When PMPLL bit is "0", the AK4951A becomes EXT mode. Master clock can be input to the internal ADC and DAC directly from the MCKI pin without internal PLL circuit operation. This mode is compatible with I/F of a normal audio CODEC. The external clocks required to operate this mode are MCKI (256fs, 384fs, 512fs or 1024fs), LRCK (fs) and BICK (≥32fs). The master clock (MCKI) must be synchronized with LRCK. The phase between these clocks is not important. The input frequency of MCKI is selected by CM1-0 bits (Table 11) and the sampling frequency is selected by FS3-0 bits (Table 12).

Table 11. MCKI Frequency at EXT Slave Mode (PMPLL bit = "0", M/S bit = "0")

Mode	CM1 bit	CM0 bit	MCKI Input Frequency	Sampling Frequency Range	
0	0	0	256fs	8kHz ≤ fs ≤ 48kHz	(default)
1	0	1	384fs	8kHz ≤ fs ≤ 48kHz	
2	1	0	512fs	8kHz ≤ fs ≤ 48kHz	
3	1	1	1024fs	8kHz ≤ fs ≤ 24kHz	

Table 12. Setting of Sampling Frequency

Mode	FS3 bit	FS2 bit	FS1 bit	FS0 bit	Sampling Frequency	
0	0	0	0	0	8kHz mode	
1	0	0	0	1	12kHz mode	
2	0	0	1	0	16kHz mode	
5	0	1	0	1	11.025kHz mode	
7	0	1	1	1	22.05kHz mode	
9	1	0	0	1	24kHz mode	
10	1	0	1	0	32kHz mode	
11	1	0	1	1	48kHz mode	(default)
15	1	1	1	1	44.1kHz mode	
Others	Others				N/A	

(N/A: Not Available)

The S/N of the DAC at low sampling frequencies is worse than at high sampling frequencies due to out-of-band noise. The out-of-band noise can be reduced by using higher frequency of the master clock. The S/N of the DAC output through HPL/HPR pins is shown in Table 13.

Table 13. Relationship between MCKI and S/N of HPL/HPR pins

MCKI	S/N (fs=8kHz, 20kHzLPF + A-weighted)
256fs	82dB
384fs	82dB
512fs	95dB
1024fs	97dB

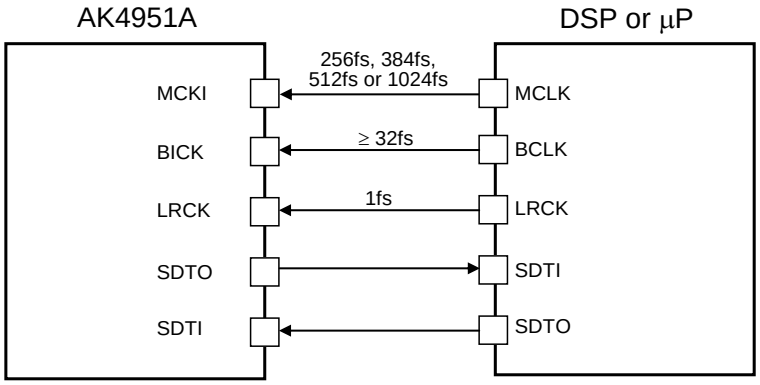


Figure 17. EXT Slave Mode

■ EXT Master Mode (PMPLL bit = “0”, M/S bit = “1”)

The AK4951A becomes EXT Master Mode by setting PMPLL bit = “0” and M/S bit = “1”. Master clock can be input to the internal ADC and DAC directly from the MCKI pin without the internal PLL circuit operation. The external clock required to operate the AK4951A is MCKI (256fs, 384fs, 512fs or 1024fs). The input frequency of MCKI is selected by CM1-0 bits (Table 14) and the sampling frequency is selected by FS3-0 bits (Table 15). When the state of AK4951A is ADC power-down or Loopback mode, the output of BICK, LRCK and SDTO pins can be stopped by CKOFF bit. When CKOFF bit = “1”, BICK, LRCK and SDTO pins output “L”. The BICK output frequency is selected between 32fs or 64fs, by BCKO bit (Table 17).

Table 14. MCKI Frequency at EXT Master Mode (PMPLL bit = “0”, M/S bit = “1”)

Mode	CM1 bit	CM0 bit	MCKI Input Frequency	Sampling Frequency Range	
0	0	0	256fs	8kHz ≤ fs ≤ 48kHz	(default)
1	0	1	384fs	8kHz < fs ≤ 48kHz	
2	1	0	512fs	8kHz < fs ≤ 48kHz	
3	1	1	1024fs	8kHz ≤ fs ≤ 24kHz	

Table 15. Setting of Sampling Frequency

Mode	FS3 bit	FS2 bit	FS1 bit	FS0 bit	Sampling Frequency	
0	0	0	0	0	8kHz mode	
1	0	0	0	1	12kHz mode	
2	0	0	1	0	16kHz mode	
5	0	1	0	1	11.025kHz mode	
7	0	1	1	1	22.05kHz mode	
9	1	0	0	1	24kHz mode	
10	1	0	1	0	32kHz mode	
11	1	0	1	1	48kHz mode	(default)
15	1	1	1	1	44.1kHz mode	
Others	Others				N/A	

(N/A: Not Available)

The S/N of the DAC at low sampling frequencies is worse than at high sampling frequencies due to out-of-band noise. The out-of-band noise can be reduced by using higher frequency of the master clock. The S/N of the DAC output through HPL/HPR pins is shown in Table 16.

Table 16. Relationship between MCKI and S/N of HPL/HPR pins

MCKI	S/N (fs=8kHz, 20kHzLPF + A-weighted)
256fs	82dB
384fs	82dB
512fs	95dB
1024fs	97dB

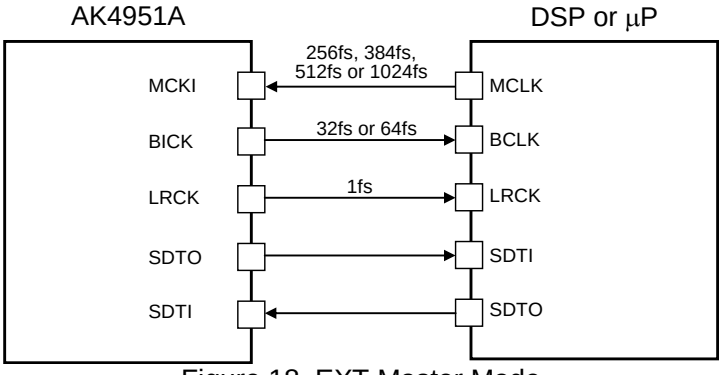


Figure 18. EXT Master Mode

Table 17. BICK Output Frequency at Master Mode

BCKO bit	BICK Output Frequency	
0	32fs	(default)
1	64fs	

■ System Reset

Upon power-up, the AK4951A must be reset by bringing the PDN pin = “L”. This reset is released when a dummy command is input after the PDN pin = “H”. This ensures that all internal registers reset to their initial value. Dummy command is executed by writing all “0” to the register address 00H (Figure 19). It is recommended to set the PDN pin to “L” before power up the AK4951A.

In I^2C Bus mode, the AK4951A does not return an ACK after receiving a slave address by a dummy command as shown in Figure 19. In the actual case, initializing cycle starts by 8 SCL clocks during the PDN pin = “H” regardless of the SDA line. Therefore, retry command is not required (Figure 20). Executing a write or read command to the other device that is connected to the same I^2C Bus also resets the AK4951A.

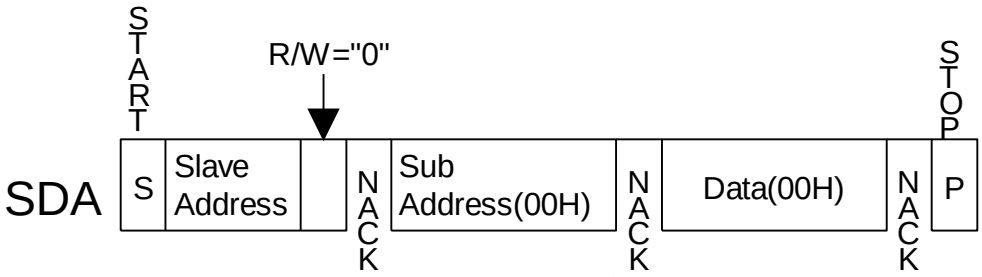


Figure 19. Dummy Command in I^2C Bus Mode

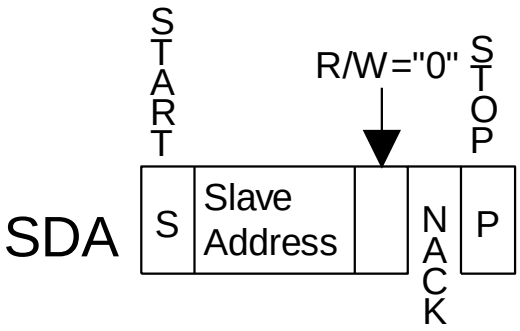


Figure 20. Reset Completion for example

The ADC starts an initialization cycle if the one of PMADL or PMADR is set to “1” when both of the PMADL and PMADR bits are “0”. The initialization cycle is set by ADRST1-0 bits (Table 18). During the initialization cycle, the ADC digital data outputs of both channels are forced to “0” in 2's complement. The ADC output reflects the analog input signal after the initialization cycle is finished. When using a digital microphone (PMDML/R bits =“0” → “1”), the initialization cycle is the same as ADC’s.

Note 36. The initial data of ADC has offset data that depends on microphones and the cut-off frequency of HPF. If this offset is not small, make initialization cycle longer by setting ADRST1-0 bits or do not use the first data of ADC outputs.

Table 18. ADC Initialization Cycle

ADRST1-0 bits	Initialize Cycle				
	Cycle	fs = 8kHz	fs = 16kHz	fs = 48kHz	
00	1059/fs	132.4ms	66.2ms	22ms	(default)
01	267/fs	33.4ms	16.7ms	5.6ms	
10	531/fs	66.4ms	33.2ms	11.1ms	
11	135/fs	16.9ms	8.4ms	2.8ms	

The DAC is initialized by setting PMDAC bit “0” → “1”. The initialization cycle is 2/fs. Therefore, the DAC outputs signals after group delay period and 2/fs when power up the device. Normally, this group delay period or 2/fs initialization cycle mentioned above is absorbed by power-up time of amplifiers after the DAC (Headphone-amp, Lineout-amp and SPK-amp).

■ Audio Interface Format

Four types of data formats are available and selected by setting the DIF1-0 bits (Table 19). In all modes, the serial data is MSB first, 2's complement format. Audio interface formats are supported in both master and slave modes. LRCK and BICK are output from the AK4951A in master mode, but must be input to the AK4951A in slave mode. The SDTO is clocked out on the falling edge ("↓") of BICK and the SDTI is latched on the rising edge ("↑") of BICK.

Table 19. Audio Interface Format

Mode	DIF1 bit	DIF0 bit	SDTO (ADC)	SDTI (DAC)	BICK	Figure	
0	0	0	24bit MSB justified	24bit LSB justified	≥ 48fs	Figure 21	
1	0	1	24bit MSB justified	16bit LSB justified	≥ 32fs	Figure 22	
2	1	0	24bit MSB justified	24bit MSB justified	≥ 48fs	Figure 23	(default)
3	1	1	I^2S Compatible	I^2S Compatible	=32fs or ≥ 48fs	Figure 24	

If 24-bit (16-bit) data, the output of ADC, is converted to 8-bit data by removing LSB 16-bit (8-bit), "−1" at 24-bit (16bit) data is converted to "−1" at 8-bit data. And when the DAC playbacks this 8-bit data, "−1" at 8-bit data will be converted to "−65536" at 24-bit ("−256" at 16-bit) data which is a large offset. This offset can be removed by adding the offset of "32768" at 24-bit ("128" at 16-bit) to 24-bit (16-bit) data before converting to 8-bit data.

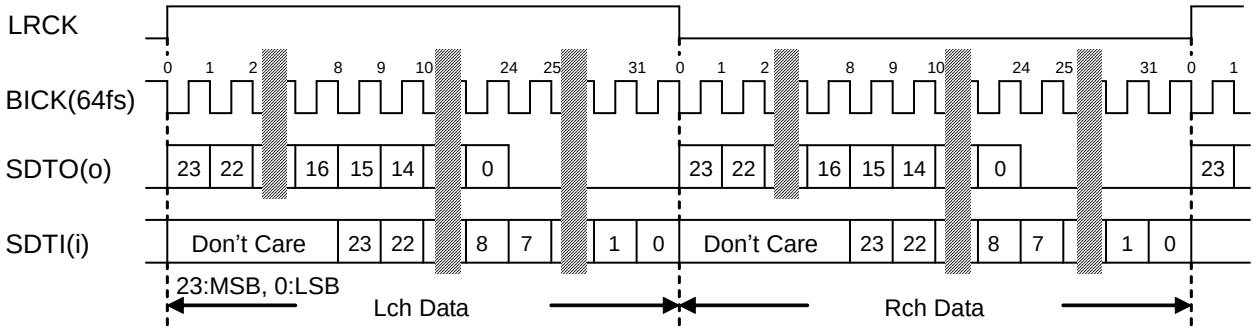


Figure 21. Mode 0 Timing

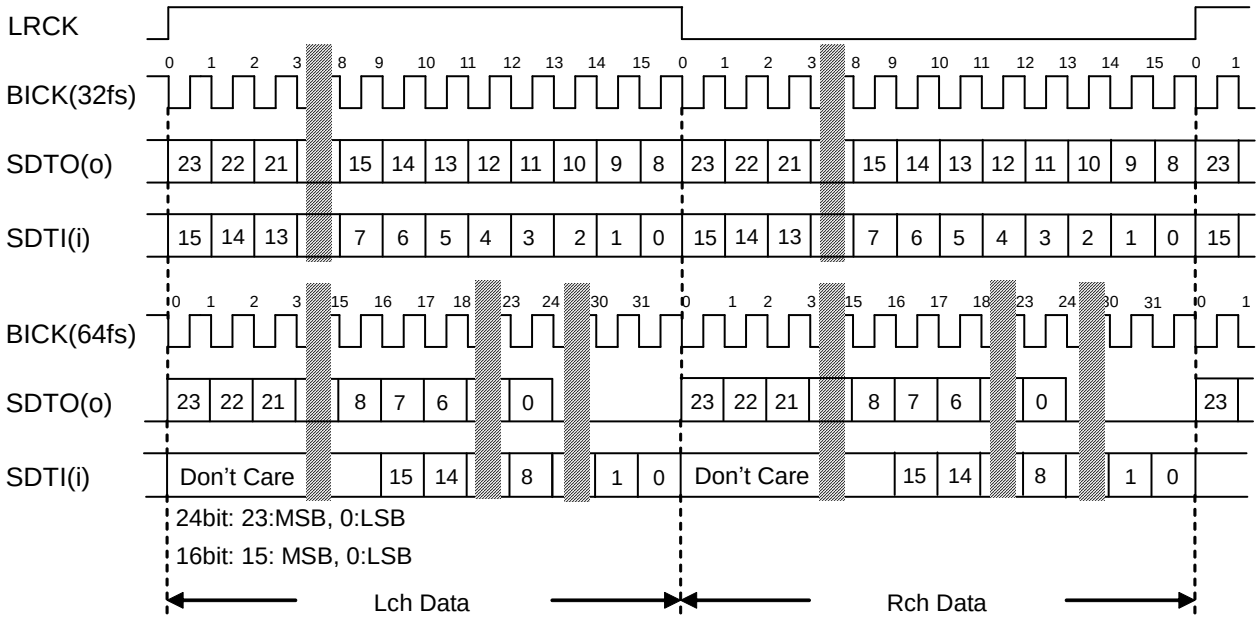


Figure 22. Mode 1 Timing

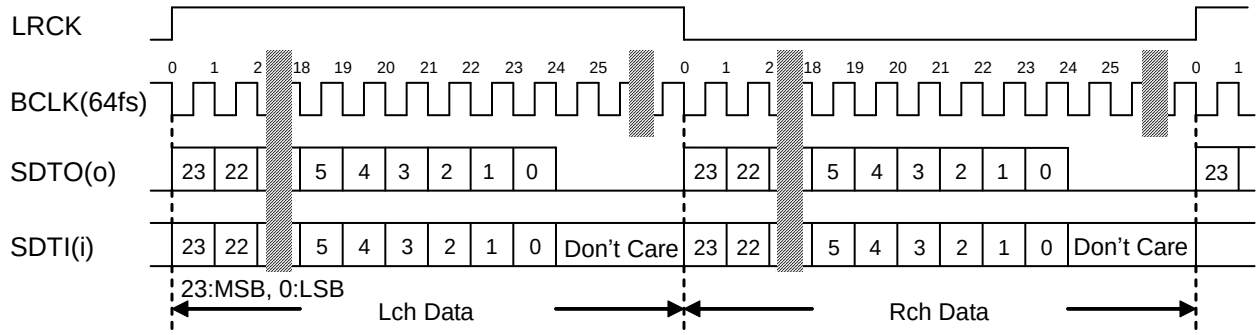


Figure 23. Mode 2 Timing

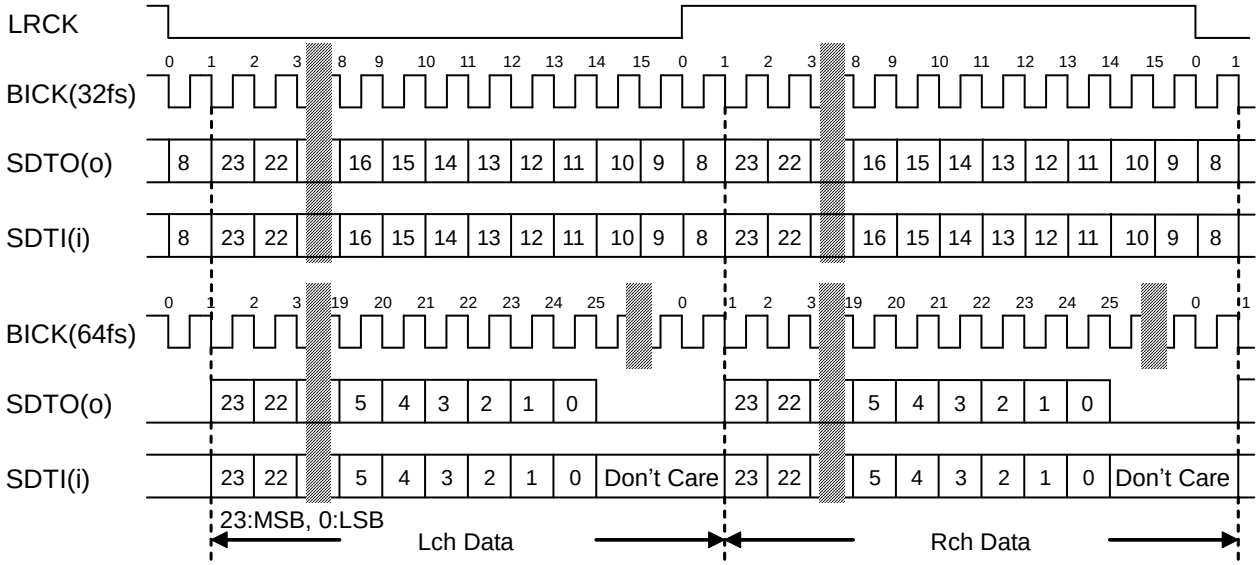


Figure 24. Mode 3 Timing

■ ADC Mono/Stereo Mode

PMADL, PMADR, PMDML and PMDMR bits set mono/stereo ADC operation. When changing ADC operation and analog/digital microphone, PMADL, PMADR, PMDML and PMDMR bits must be set “0” at first. When DMIC bit = “1”, PMADL and PMADR bit settings are ignored. When DMIC bit = “0”, PMDML and PMDMR bit settings are ignored.

Table 20. Mono/Stereo ADC operation (Analog Microphone)

PMADL bit	PMADR bit	ADC Lch data	ADC Rch data	
0	0	All “0”	All “0”	(default)
0	1	Rch Input Signal	Rch Input Signal	
1	0	Lch Input Signal	Lch Input Signal	
1	1	Lch Input Signal	Rch Input Signal	

Table 21. Mono/Stereo ADC operation (Digital Microphone)

PMDML bit	PMDMR bit	ADC Lch data	ADC Rch data	
0	0	All “0”	All “0”	(default)
0	1	Rch Input Signal	Rch Input Signal	
1	0	Lch Input Signal	Lch Input Signal	
1	1	Lch Input Signal	Rch Input Signal	

■ MIC/LINE Input Selector

The AK4951A has an input selector. INL1-0 and INR1-0 bits select LIN1/LIN2/LIN3 and RIN1/RIN2/RIN3, respectively. When DMIC bit = “1”, digital microphone input is selected regardless of INL1-0 and INR1-0 bits. RIN3 pin is shared with BEEP pin. When PMBP bit = “0”, RIN3 pin can be selected.

Table 22. MIC/Line In Path Select

DMIC bit	INL1 bit	INL0 bit	INR1 bit	INR0 bit	Lch	Rch	
0	0	0	0	0	LIN1	RIN1	(default)
	0	0	0	1	LIN1	RIN2	
	0	0	1	0	LIN1	RIN3	
	0	1	0	0	LIN2	RIN1	
	0	1	0	1	LIN2	RIN2	
	0	1	1	0	LIN2	RIN3	
	1	0	0	0	LIN3	RIN1	
	1	0	0	1	LIN3	RIN2	
	1	0	1	0	LIN3	RIN3	
	Others				N/A	N/A	
1	x	x	x	x	Digital Microphone		

(x: Do not care, N/A: Not available)

■ Microphone Gain Amplifier

The AK4951A has a gain amplifier for microphone input. It is powered-up by PMADL/R bit = "1". The gain of MIC-Amp is selected by the MGAIN3-0 bits. The typical input impedance is 30kΩ. A click noise may occur if the MIC-Amp gain is changed when both MIC-Amp and ADC (PMADL/R bits = "1") are powered up.
High frequency characteristics are attenuated when MIC-Amp = +30dB. The attenuation amount of when MIC-Amp = +30dB is -0.5dB at 10kHz frequency and -1.5dB at 20kHz frequency comparing with when MIC-Amp = +18dB.

Table 23. Input Gain

MGAIN3 bit	MGAIN2 bit	MGAIN1 bit	MGAIN0 bit	Input Gain	
0	0	0	0	0dB	
0	0	0	1	+3dB	
0	0	1	0	+6dB	
0	0	1	1	+9dB	
0	1	0	0	+12dB	
0	1	0	1	+15dB	
0	1	1	0	+18dB	(default)
0	1	1	1	+21dB	
1	0	0	0	+24dB	
1	0	0	1	+27dB	
1	0	1	0	+30dB	
Others				N/A	

(N/A: Not available)

■ Microphone Power

When PMMP bit = "1", the MPWR1 or MPWR2 pin supplies the power for microphones. This output voltage is typically 2.4V @MICL bit ="0", and typically 2.0V@MICL bit = "1". The load resistance is minimum 1.0kΩ In case of using two sets of stereo microphones, the load resistance is minimum 2kΩ for each channel. Any capacitor must not be connected directly to the MPWR1 and MPWR2 pins (Figure 25).

Table 24. Microphone Power

PMMP bit	MPSEL bit	MPWR1 pin	MPWR2 pin	
0	x	Hi-Z	Hi-Z	(default)
1	0	Output	Pull-down (13kΩ)	
	1	Pull-down (13kΩ)	Output	

(x: Do not care)

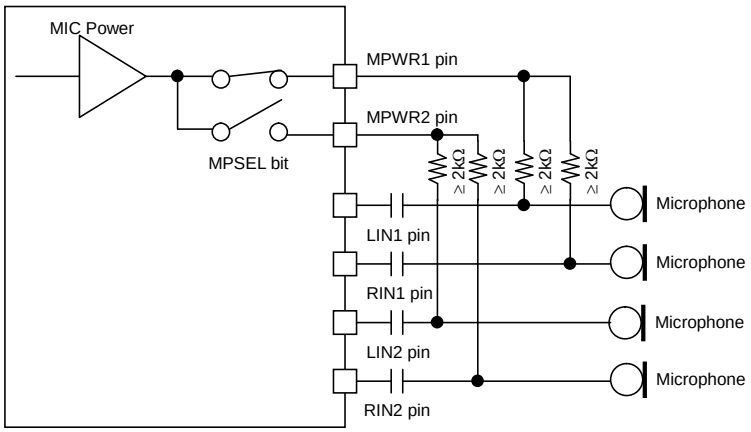


Figure 25. Microphone Block Circuit

■ Digital Microphone

1. Connection to Digital Microphones

When DMIC bit is set to “1”, the LIN1 and RIN1 pins become DMDAT (digital microphone data input) and DMCLK (digital microphone clock supply) pins, respectively. The same voltage as AVDD must be provided to the digital microphone. The Figure 26 and Figure 27 show stereo/mono connection examples. The DMCLK clock is input to a digital microphone from the AK4951A. The digital microphone outputs 1bit data, which is generated by ΔΣModulator using DMCLK clock, to the DMDAT pin. PMDML/R bits control power up/down of the digital block (Decimation Filter and Digital Filter). (PMADL/PMADR bits settings do not affect the digital microphone power management. Set PMMP = PMMICL/R bits to “0” when using a digital microphone.) The DCLKE bit controls ON/OFF of the output clock from the DMCLK pin. When the AK4951A is powered down (PDN pin= “L”), the DMCLK and DMDAT pins become floating state. Pull-down resistors must be connected to DMCLK and DMDAT pins externally to avoid this floating state.

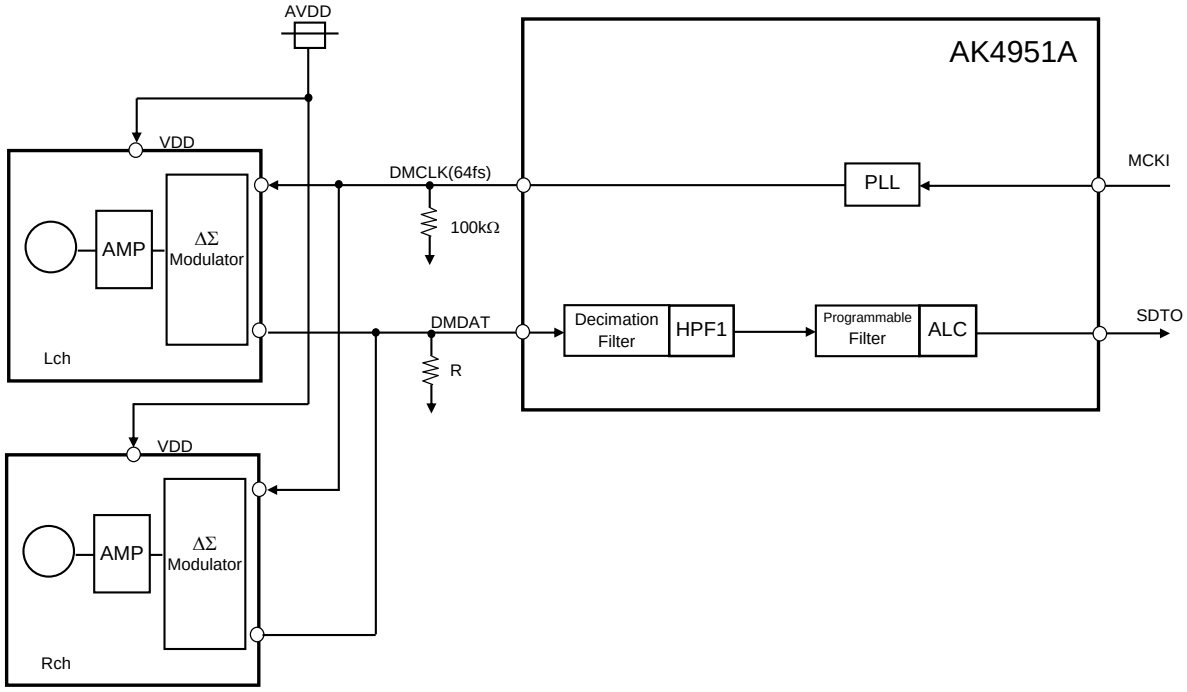


Figure 26. Connection Example of Stereo Digital Microphone

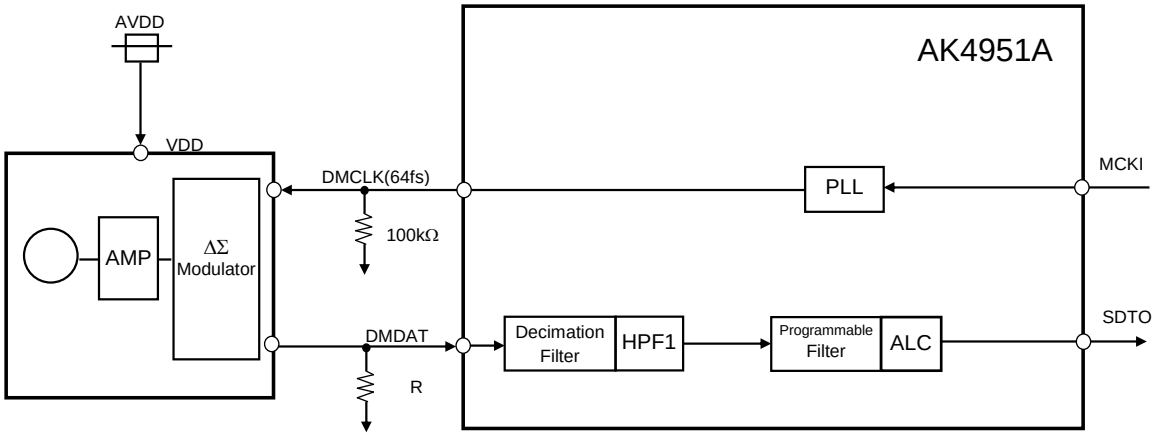


Figure 27. Connection Example of Mono Digital Microphone

2. Interface

The input data channel of the DMDAT pin is set by DCLKP bit. When DCLKP bit = “1”, L channel data is input to the decimation filter if DMCLK = “H”, and R channel data is input if DMCLK = “L”. When DCLKP bit = “0”, R channel data is input to the decimation filter while DMCLK pin= “H”, and L channel data is input while DMCLK pin= “L”. The DMCLK pin only supports 64fs. It outputs “L” when DCLKE bit = “0”, and outputs 64fs when DCLKE bit = “1”. In this case, necessary clocks must be supplied to the AK4951A for ADC operation. The output data through “the Decimation and Digital Filters” is 24bit full scale when the 1bit data density is 0%~100%.

Table 25. Data In/Output Timing with Digital Microphone (DCLKP bit = “0”)

DCLKP bit	DMCLK pin= “H”	DMCLK pin= “L”	
0	Rch	Lch	(default)
1	Lch	Rch	

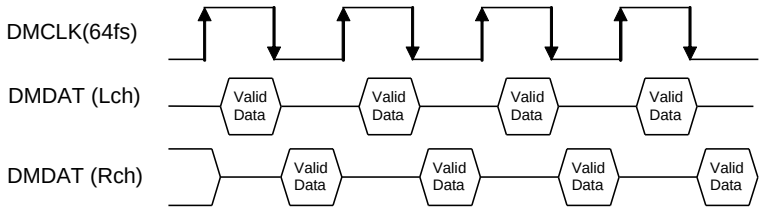


Figure 28. Data In/Output Timing with Digital Microphone (DCLKP bit = “1”)

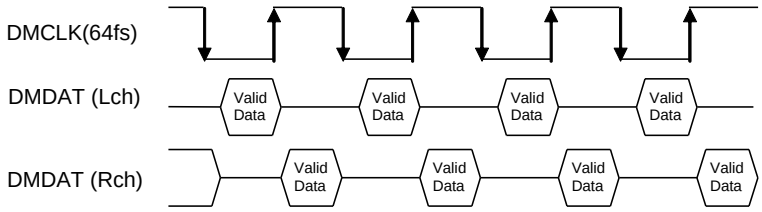
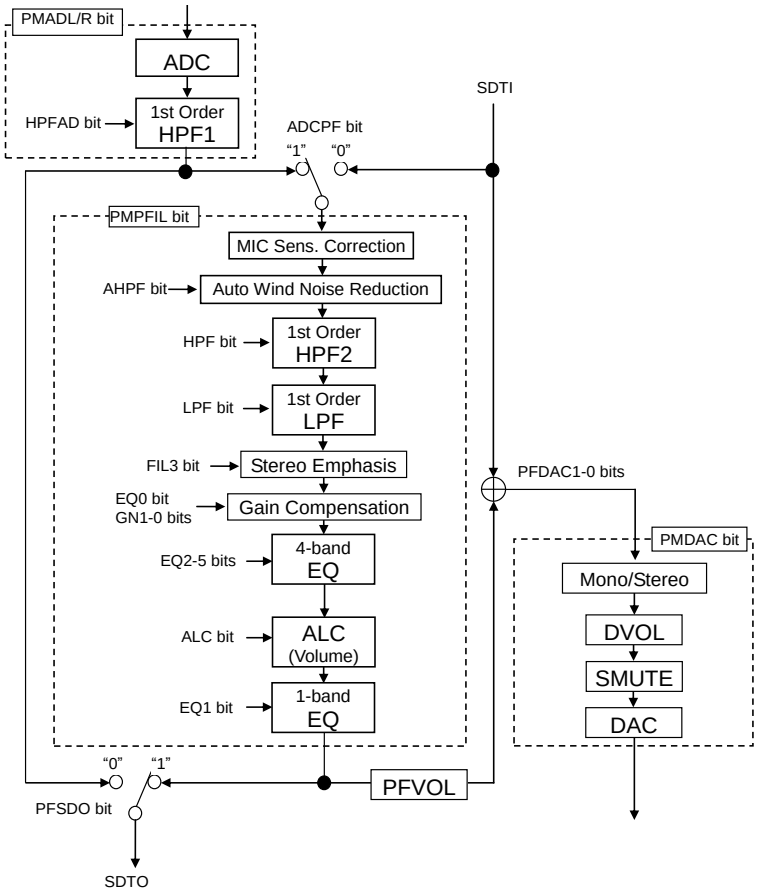


Figure 29. Data In/Output Timing with Digital Microphone (DCLKP bit = “0”)

■ Digital Block

The digital block consists of the blocks shown in Figure 30. Recording path and playback path is selected by setting ADCPF bit, PFDAC1-0 bits and PFSDO bit (Figure 31 ~ Figure 34, Table 26).



(1) ADC: Includes the Digital Filter (LPF) for ADC as shown in "Filter Characteristics".
(2) HPF1: High Pass Filter (HPF) for ADC as shown in "Digital HPF1".
(3) Microphone Sensitivity Correction: Microphone volume control between L and R channels. (See "Microphone Sensitivity Correction")
(4) Automatic Wind Noise Reduction Filter: Automatic HPF (See "Automatic Wind Noise Reduction Filter")
(5) HPF2: High Pass Filter. (See "Digital Programmable Filter Circuit")
(6) LPF: Low Pass Filter (See "Digital Programmable Filter Circuit")
(7) Stereo Emphasis: Stereo emphasis Filter. (See "Digital Programmable Filter Circuit")
(8) Gain Compensation: Gain compensation consists of EQ and Gain control. It corrects frequency response after stereo separation emphasis filter. (See "Digital Programmable Filter Circuit")
(9) 4 Band EQ: Applicable for use as Equalizer or Notch Filter. (See "Digital Programmable Filter Circuit")
(10) ALC (Volume): Digital Volume with ALC Function. (See "Input Digital Volume (Manual Mode)" and "ALC Operation")
(11) 1 Band EQ: Applicable for use as Notch Filter (See "Digital Programmable Filter Circuit")
(12) PFVOL: Sidetone digital volume (See "Sidetone digital Volume")
(13) Mono/Stereo Switching: Mono/Stereo lineout outputs select from DAC which described in <Mono Mixing Output> at "DAC Mono/Stereo Mode".
(14) DVOL: Digital volume for playback path (See "Output Digital Volume")
(15) SMUTE: Soft mute function (See "Soft Mute")

Figure 30. Digital Block Path Select

Table 26. Recording Playback Mode Example

Mode Example	ADCPF bit	PFDAC1-0 bits	PFSDO bit	Figure	
Recording Mode 1 & Playback Mode 2	1	00	1	Figure 31	(default)
Recording Mode 2 & Playback Mode 1	0	01	0	Figure 32	
Recording Mode 2 & Playback Mode 2 (Programmable Filter Bypass Mode: PMPFIL bit = "0")	x	00	0	Figure 33	
Loopback Mode	1	01	1	Figure 34	

(x: Do not care)

When changing those modes, PMPFIL bit must be "0".

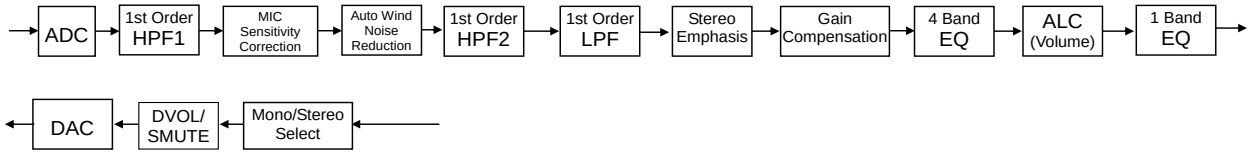


Figure 31. The Path in Recording Mode 1 & Playback Mode 2 (default)

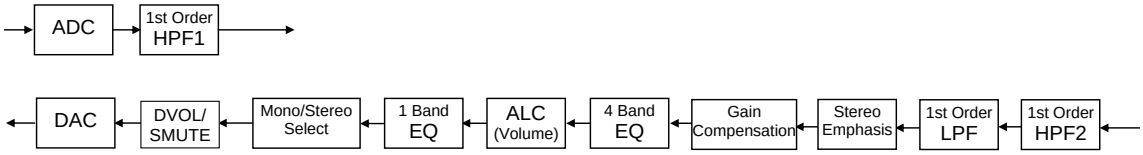


Figure 32. The Path in Recording Mode 2 & Playback Mode 1

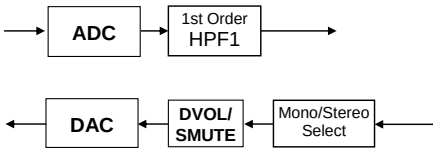


Figure 33. The Path in Recording Mode 2 & Playback Mode 2

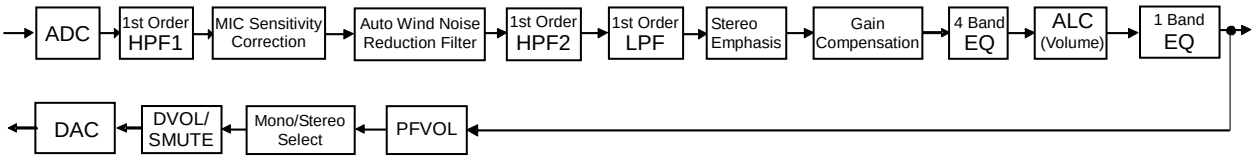


Figure 34. The Path in Loopback Mode

■ Digital HPF1

A digital High Pass Filter (HPF) is integrated for DC offset cancellation of the ADC input. The cut-off frequencies (fc) of the HPF1 are set by HPFC1-0 bits. It is proportional to the sampling frequency (fs) and the default value is 3.7Hz (@fs = 48kHz). HPFAD bit controls the ON/OFF of the HPF1 (HPF ON is recommended).

Table 27. HPF1 Cut-off Frequency

HPFC1 bit	HPFC0 bit	fc			
		fs=8kHz	fs=16kHz	fs=48kHz	
0	0	0.62Hz	1.2Hz	3.7Hz	(default)
0	1	2.47Hz	4.9Hz	14.8Hz	
1	0	19.7Hz	39.5Hz	118.4Hz	
1	1	39.5Hz	78.9Hz	236.8Hz	

■ Microphone Sensitivity Correction

The AK4951A has linear microphone sensitivity correction function controlled by MGL/R7-0 bits. MGL/R7-0 bits must be set when PMADL/R bits = “0” or PMPFIL bit = “0”.

Table 28. Microphone Sensitivity Correction

MGL7-0 bits MGR7-0 bits	MG_DATA	GAIN (dB)	Calculation	
00H	0	Mute	-	
01H	1	-42.144	$20 \log_{10}(MG\_DATA/128)$	(default)
02H	2	-36.124		
:	:	:		
7EH	126	-0.137		
7FH	127	-0.068		
80H	128	0.000		
81H	129	+0.068		
82H	130	+0.135		
:	:	:		
FDH	253	+5.918		
FEH	254	+5.952		
FFH	255	+5.987		

■ Automatic Wind Noise Reduction Filter

The AK4951A has an automatic wind noise reduction filter that is controlled by AHPF bit. The automatic wind noise reduction filter is ON when AHPF bit = “1”. It attenuates the wind noise when detecting a wind noise and adjusts the attenuation level dynamically. When AHPF bit = “0”, the audio data passes this block by 0dB gain. SENC2-0 bits control the wind noise detection sensitivity, and STG1-0 bits control the attenuation level of the maximum attenuation. SENC2-0 bits and STG1-0 bits must be set when AHPF bit = “0” or PMPF bit = “0”.

The automatic wind noise reduction filter has peak detection function for voice band. When the AK4951A detects peak level in voice band during the wind noise reduction, it suppresses the wind noise reduction level automatically in order to ensure the voice band bandwidth. When VODETN bit = “1”, the voice peak detection is disable, and the wind noise reduction will continue working even if the voice peak level increases. VODETN bit must be set when PMPFIL bit = “0”.

Table 29. Wind Noise Detection Sensitivity

SENC2-0 bits	Sensitivity Level		
000	0.5	Low ⇧	
001	1.0		
010	1.5		
011	2.0		(default)
100	2.5		
101	3.0	⇩	
110	3.5		
111	4.0	High	

Table 30. Attenuation Level of Automatic Wind Noise Reduction Filter

STG1-0 bits	Attenuation Level		
00	Low	Low	(default)
01	Middle1	⇩	
10	Middle2		
11	High	High	

■ Digital Programmable Filter Circuit

(1) High Pass Filter (HPF2)

This is composed 1st order HPF. The coefficient of HPF is set by F1A13-0 bits and F1B13-0 bits. HPF bit controls ON/OFF of the HPF2. When the HPF2 is OFF, the audio data passes this block by 0dB gain. The coefficient must be set when PMPFIL bit = "0" or HPF bit = "0". The HPF2 starts operation 4/fs (max) after when HPF bit = PMPFIL bit = "1" is set.

fs: Sampling Frequency
fc: Cutoff Frequency

Register Setting (Note 37)
HPF: F1A[13:0] bits =A, F1B[13:0] bits =B
(MSB=F1A13, F1B13; LSB=F1A0, F1B0)

$$A = \frac{1 / \tan(\pi fc/fs)}{1 + 1 / \tan(\pi fc/fs)}, \quad B = \frac{1 - 1 / \tan(\pi fc/fs)}{1 + 1 / \tan(\pi fc/fs)}$$

Transfer Function

$$H(z) = A \frac{1 - z^{-1}}{1 + Bz^{-1}}$$

The cut-off frequency must be set as below.
fc/fs ≥ 0.0001 (fc min = 4.8Hz at 48kHz)

(2) Low Pass Filter (LPF)

This is composed with 1st order LPF. F2A13-0 bits and F2B13-0 bits set the coefficient of LPF. LPF bit controls ON/OFF of the LPF. When the LPF is OFF, the audio data passes this block by 0dB gain. The coefficient must be set when PMPFIL bit = "0" or LPF bit = "0". The LPF starts operation 4/fs (max) after when LPF bit =PMPFIL bit= "1" is set.

fs: Sampling Frequency
fc: Cutoff Frequency

Register Setting (Note 37)
LPF: F2A[13:0] bits =A, F2B[13:0] bits =B
(MSB=F2A13, F2B13; LSB=F2A0, F2B0)

$$A = \frac{1}{1 + 1 / \tan(\pi fc/fs)}, \quad B = \frac{1 - 1 / \tan(\pi fc/fs)}{1 + 1 / \tan(\pi fc/fs)}$$

Transfer Function

$$H(z) = A \frac{1 + z^{-1}}{1 + Bz^{-1}}$$

The cut-off frequency must be set as below.
fc/fs ≥ 0.05 (fc min = 2400Hz at 48kHz)

(3) Stereo Separation Emphasis Filter (FIL3)

The FIL3 is used to emphasize the stereo separation of stereo microphone recording data and playback data. F3A13-0 bits and F3B13-0 bits set the filter coefficients of the FIL3. When F3AS bit = "0", the FIL3 performs as a High Pass Filter (HPF), and it performs as a Low Pass Filter (LPF) when F3AS bit = "1". FIL3 bit controls ON/OFF of the FIL3. When the stereo separation emphasis filter is OFF, the audio data passes this block by 0dB gain. The coefficient should be set when FIL3 bit or PMPFIL bit is "0". The FIL3 starts operation 4/fs(max) after when FIL3 bit = PMPFIL bit = "1" is set.

1) In case of setting FIL3 as HPF

fs: Sampling Frequency
fc: Cutoff Frequency
K: Gain [dB] (0dB ≥ K ≥ –10dB)

Register Setting (Note 37)
FIL3: F3AS bit = "0", F3A[13:0] bits =A, F3B[13:0] bits =B
(MSB=F3A13, F3B13; LSB=F3A0, F3B0)

$$A = 10^{K/20} \times \frac{1 / \tan(\pi fc/fs)}{1 + 1 / \tan(\pi fc/fs)}, \quad B = \frac{1 - 1 / \tan(\pi fc/fs)}{1 + 1 / \tan(\pi fc/fs)}$$

Transfer Function

$$H(z) = A \frac{1 - z^{-1}}{1 + Bz^{-1}}$$

The cut-off frequency must be set as below.
fc/fs ≥ 0.0001 (fc min = 4.8Hz @fs=48kHz)

2) In case of setting FIL3 as LPF

fs: Sampling Frequency
fc: Cutoff Frequency
K: Gain [dB] (0dB ≥ K ≥ –10dB)

Register Setting (Note 37)
FIL3: F3AS bit = "1", F3A[13:0] bits =A, F3B[13:0] bits =B
(MSB=F3A13, F3B13; LSB= F3A0, F3B0)

$$A = 10^{K/20} \times \frac{1}{1 + 1 / \tan(\pi fc/fs)}, \quad B = \frac{1 - 1 / \tan(\pi fc/fs)}{1 + 1 / \tan(\pi fc/fs)}$$

Transfer Function

$$H(z) = A \frac{1 + z^{-1}}{1 + Bz^{-1}}$$

The cut-off frequency must be set as below.
fc/fs ≥ 0.0001 (fc min = 4.8Hz @fs=48kHz)

(4) Gain Compensation (EQ0)

Gain compensation is used to compensate the frequency response and the gain that is changed by the stereo separation emphasis filter. Gain compensation is composed of the Equalizer (EQ0) and the Gain (0dB/+12dB/+24dB). E0A15-0 bits, E0B13-0 bits and E0C15-0 bits set the coefficient of EQ0. GN1-0 bits set the gain (Table 31). EQ0 bit controls ON/OFF of EQ0. When EQ is OFF and the gain is 0dB, the audio data passes this block by 0dB gain. The coefficient should be set when EQ0 bit = "0" or PMPFIL bit = "0". The EQ0 starts operation 4/fs(max) after when EQ0 bit =PMPFIL bit= "1" is set.

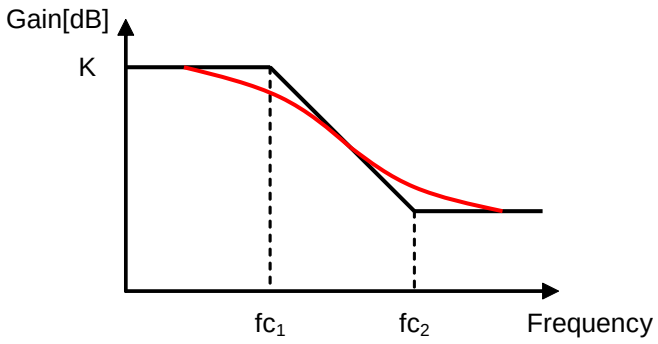
fs: Sampling Frequency
fc_1: Polar Frequency
fc_2: Zero-point Frequency
K: Gain [dB] (Maximum setting is +12dB.)

Register Setting (Note 37)
E0A[15:0] bits =A, E0B[13:0] bits =B, E0C[15:0] bits =C
(MSB=E0A15, E0B13, E0C15; LSB=E0A0, E0B0, E0C0)

$$A = 10^{K/20} \times \frac{1 + 1 / \tan(\pi fc_2/fs)}{1 + 1 / \tan(\pi fc_1/fs)}, \quad B = \frac{1 - 1 / \tan(\pi fc_1/fs)}{1 + 1 / \tan(\pi fc_1/fs)}, \quad C = 10^{K/20} \times \frac{1 - 1 / \tan(\pi fc_2/fs)}{1 + 1 / \tan(\pi fc_1/fs)}$$

Transfer Function

$$H(z) = \frac{A + Cz^{-1}}{1 + Bz^{-1}}$$



(Note) Black: Diagrammatic Line, Red: Actual Curve
Figure 35. EQ0 Frequency Response

Table 31. Gain Setting

GN1 bit	GN0 bit	Gain	
0	0	0dB	(default)
0	1	+12dB	
1	x	+24dB	

(x: Do not care)

(5) 4-band Equalizer & 1-band Equalizer after ALC

This block can be used as equalizer or Notch Filter. 4-band equalizers (EQ2~EQ5) are switched ON/OFF independently by EQ2, EQ3, EQ4 and EQ5 bits. EQ1 bit controls ON/OFF switching of the equalizer after ALC (EQ1). When the equalizer is OFF, the audio data passes this block by 0dB gain. E1A15-0 bits, E1B15-0 bits and E1C15-0 bits set the coefficient of EQ1. E2A15-0 bits, E2B15-0 bits and E2C15-0 bits set the coefficient of EQ2. E3A15-0 bits, E3B15-0 bits and E3C15-0 bits set the coefficient of EQ3. E4A15-0 bits, E4B15-0 bits and E4C15-0 bits set the coefficient of EQ4. E5A15-0 bits, E5B15-0 bits and E5C15-0 bits set the coefficient of EQ5. The EQn (n=1, 2, 3, 4 or 5) coefficient must be set when EQn bit = "0" or PMPFIL bit = "0". EQn starts operation 4/fs(max) after when EQn = PMPFIL bit = "1" is set.

Each EQ2 ~ 5 blocks have a gain controller (EQ2G ~ EQ5G) independently after the equalizer. EQnG5-0 bits (n = 2~5) setting is reflected by writing "1" to EQCn bit (n = 2~5). EQnG5-0 bits and EQCn bit (n=2~5) can be set during operation (EQn =PMPFIL bit= "1").

fs: Sampling Frequency
fo_1 ~ fo_5: Center Frequency
fb_1 ~ fb_5: Band width where the gain is 3dB different from the center frequency
K_1 ~ K_5: Gain ($-1 \le K_n < 3$)

Register Setting (Note 37)
EQ1: E1A[15:0] bits =A_1, E1B[15:0] bits =B_1, E1C[15:0] bits =C_1
EQ2: E2A[15:0] bits =A_2, E2B[15:0] bits =B_2, E2C[15:0] bits =C_2
EQ3: E3A[15:0] bits =A_3, E3B[15:0] bits =B_3, E3C[15:0] bits =C_3
EQ4: E4A[15:0] bits =A_4, E4B[15:0] bits =B_4, E4C[15:0] bits =C_4
EQ5: E5A[15:0] bits =A_5, E5B[15:0] bits =B_5, E5C[15:0] bits =C_5
(MSB=E1A15, E1B15, E1C15, E2A15, E2B15, E2C15, E3A15, E3B15, E3C15, E4A15, E4B15, E4C15, E5A15, E5B15, E5C15 ; LSB= E1A0, E1B0, E1C0, E2A0, E2B0, E2C0, E3A0, E3B0, E3C0, E4A0, E4B0, E4C0, E5A0, E5B0, E5C0)

$$A_n = K_n \times \frac{\tan(\pi fb_n/fs)}{1+\tan(\pi fb_n/fs)}, \quad B_n = \cos(2\pi fo_n/fs) \times \frac{2}{1+\tan(\pi fb_n/fs)}, \quad C_n = -\frac{1-\tan(\pi fb_n/fs)}{1+\tan(\pi fb_n/fs)}$$

(n = 1, 2, 3, 4, 5)

Transfer Function

$$H(z) = \{1 + G_2 \times h_2(z) + G_3 \times h_3(z) + G_4 \times h_4(z) + G_5 \times h_5(z)\} \times \{1 + h_1(z)\}$$

($G_{2,3,4,5}$ = 1 or G)

$$h_n(z) = A_n \frac{1 - z^{-2}}{1 - B_n z^{-1} - C_n z^{-2}}$$

(n = 1, 2, 3, 4, 5)

The center frequency must be set as below.
$0.003 < fo_n / fs < 0.497$

When gain of K is set to "–1", this equalizer becomes a notch filter. When EQ2 ~EQ5 is used as a notch filter, central frequency of a real notch filter deviates from the above-mentioned calculation, if its central frequency of each band is near. The control soft that is attached to the evaluation board has functions that revises a gap of frequency and calculates the coefficient. When its central frequency of each band is near, the central frequency should be revised and confirm the frequency response.

Note 37. [Translation the filter coefficient calculated by the equations above from real number to binary code (2's complement)]
X = (Real number of filter coefficient calculated by the equations above) x 2^{13}

X should be rounded to integer, and then should be translated to binary code (2's complement).
MSB of each filter coefficient setting register is sine bit.

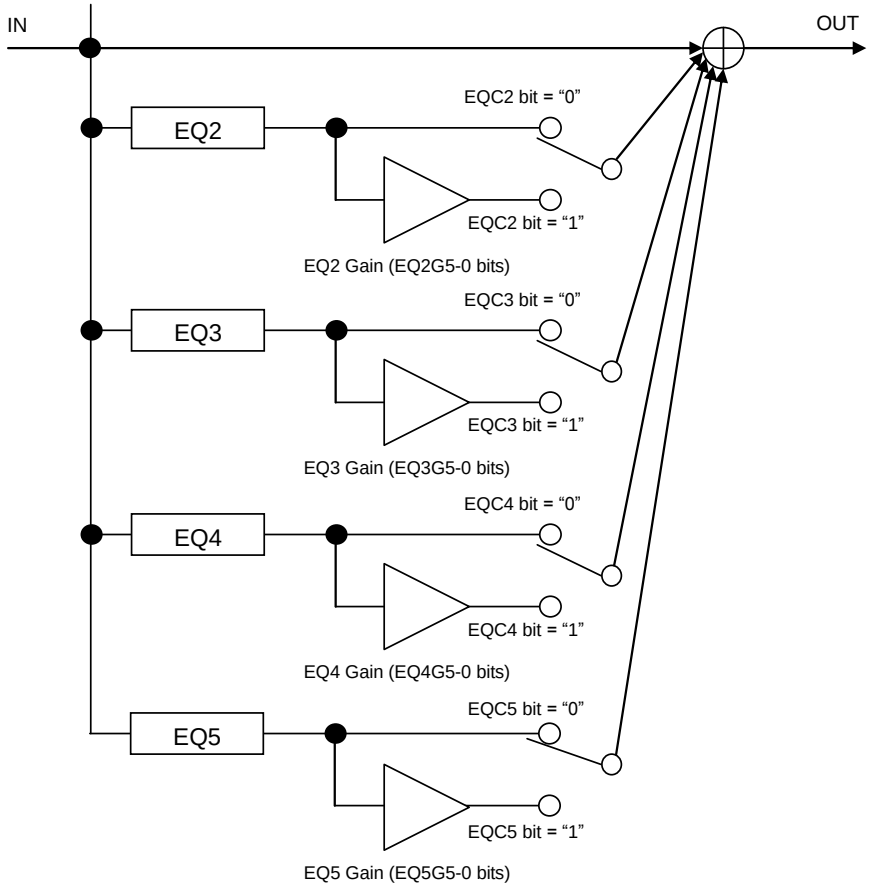


Figure 36. 4-Band EQ Structure

Table 32. EQn Gain Setting (n=2, 3, 4, 5)

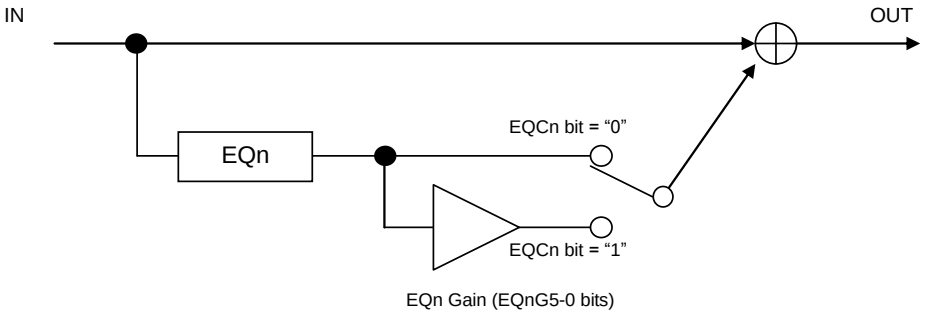
EQnG5-0 bits	EQG_DATA	Gain [dB]	Formula	
3FH	255	0	$20 \log_{10}$ (EQG_DATA/256)	
3EH	251	-0.17		
3DH	247	-0.31		
:				
02H	11	-27.34		
01H	7	-31.26		
00H	0	MUTE		(default)

Table 33. Transition Time of EQn Gain (n= 2, 3, 4, 5)

EQnT1-0 bits	Transition Time of EQnG5-0 bits = 3FH ~ 00H			
	Setting Value	fs=8kHz	fs=48kHz	
00	256/fs	32ms	5.3ms	(default)
01	2048/fs	256ms	42.7ms	
10	8192/fs	1024ms	170.7ms	
11	16384/fs	2048ms	341.3ms	

Common Gain Sequence Examples

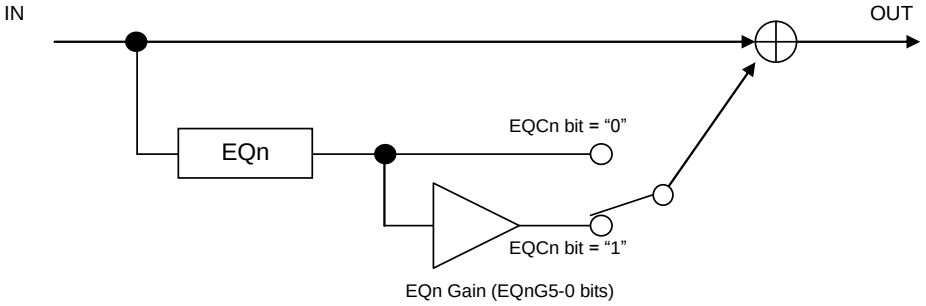
<When noise is generated>



(assuming the noise continues)

(1) Set EQCn bit: “1” → “0” (Path Setting). The gain changes immediately by this setting.
(2) Set EQnT1-0 bits: “xx” → “00” (Transition Time)
(3) Set EQnG5-0 bits: “xxH” → “3FH” (Gain Setting; should be set to 0dB)

<When noise is stopped>



(4) Set EQCn bit: “0” → “1” (Path Setting), EQnT1-0 bits Setting
(Transition Time: It should be set longer when noise is stopped.) (Note 38)
(5) Set EQnG5-0 bits (Gain Setting)
The gain of EQn is changed after a transition time set by EQnT1-0 bits.

Note 38. When changing a path of EQC2-5 by setting EQC2-5 bits “0” → “1”, the gain should be transitioned to 0dB before the settings. Otherwise, pop noise may occur on the path change.

■ ALC Operation

The ALC (Automatic Level Control) is operated by ALC block. When ADCPF bit is "1", the ALC circuit operates for recording path, and the ALC circuit operates for playback path when ADCPF bit is "0". ALC bit controls ON/OFF of ALC operation.

The ALC block consists of these blocks shown below. The ALC limiter detection level is monitored at the level detection2 block after EQ block. The level detection1 block also monitors clipping detection level (+0.53dBFS).

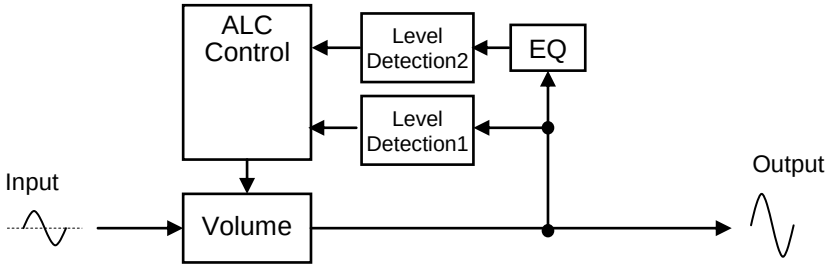


Figure 37. ALC Block

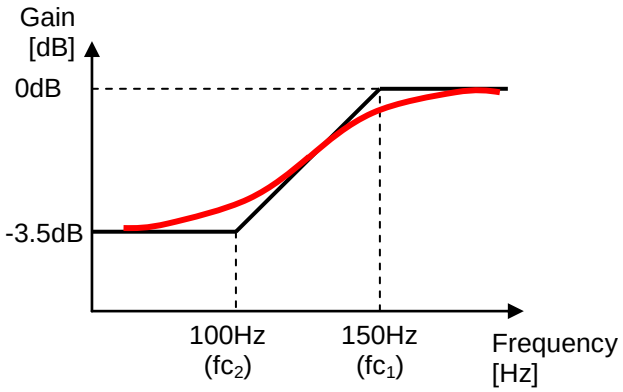
The polar (fc_1) and the zero point (fs_2) frequencies of EQ block are set by EQFC1-0 bits. Set ALCEQ bits according to the sampling frequency. When ALCEQ bit is OFF (ALCEQ bit = "1"), the level detection is not executed on this block.

Table 34. ALCEQ Frequency Setting

EQFC1-0 bits	Sampling Frequency Range	Polar Frequency (fc_1)	Zero-point Frequency (fc_2)	
00	8kHz ≤ fs ≤ 12kHz	150Hz @ fs=12kHz	100Hz @ fs=12kHz	
01	12kHz < fs ≤ 24kHz	150Hz @ fs=24kHz	100Hz @ fs=24kHz	
10	24kHz < fs ≤ 48kHz	150Hz @ fs=48kHz	100Hz @ fs=48kHz	(default)
11	N/A			

(N/A: Not available)

[ALCEQ: First order zero pole high pass filter]



Note 39. Black: Diagrammatic Line, Red: Actual Curve

Figure 38. ALCEQ Frequency Response (fs = 48kHz)

1. ALC Limiter Operation

During ALC limiter operation, when either L or R channel output level exceeds the ALC limiter detection level (Table 35), the VOL value (same value for both L and R) is attenuated automatically by the amount defined by the ALC limiter ATT step (Table 36). (Once this ALC limiter operation is started, attenuation will be repeated sixteen times.)

After completing the attenuate operation, unless ALC bit is changed to “0”, the operation repeats when the input signal level exceeds ALC limiter detection level.

Table 35. ALC Limiter Detection Level/ Recovery Counter Reset Level

LMTH2 bit	LMTH1 bit	LMTH0 bit	ALC Limiter Detection Level	ALC Recovery Counter Reset Level	
0	0	0	ALC Output ≥ –2.5dBFS	–2.5dBFS > ALC Output ≥ –4.1dBFS	(default)
0	0	1	ALC Output ≥ –2.5dBFS	–2.5dBFS > ALC Output ≥ –3.3dBFS	
0	1	0	ALC Output ≥ –4.1dBFS	–4.1dBFS > ALC Output ≥ –6.0dBFS	
0	1	1	ALC Output ≥ –4.1dBFS	–4.1dBFS > ALC Output ≥ –5.0dBFS	
1	0	0	ALC Output ≥ –6.0dBFS	–6.0dBFS > ALC Output ≥ –8.5dBFS	
1	0	1	ALC Output ≥ –6.0dBFS	–6.0dBFS > ALC Output ≥ –7.2dBFS	
1	1	0	ALC Output ≥ –8.5dBFS	–8.5dBFS > ALC Output ≥ –12.0dBFS	
1	1	1	ALC Output ≥ –8.5dBFS	–8.5dBFS > ALC Output ≥ –10.1dBFS	

Table 36. ALC Limiter ATT Step

Output	ATT Amount [dB]
+0.53dBFS ≤ Output Level (*)	0.38148
–1.16dBFS ≤ Output Level < +0.53dBFS	0.06812
LM-LEVEL ≤ Output Level < –1.16dBFS	0.02548

(*) Comparison with the next output data.

2. ALC Recovery Operation

ALC recovery operation wait for the WTM1-0 bits (Table 37) to be set after completing ALC limiter operation. If the input signal does not exceed "ALC recovery waiting counter reset level" (Table 35) during the wait time, ALC recovery operation is executed. The VOL value is automatically incremented by the setting value of RGAIN2-0 bits (Table 38) up to the set reference level (Table 39) in every sampling. When the VOL value exceeds the reference level (REF value), the VOL values are not increased. The recovery speed gets slower when the VOL peak level exceeds -12dBFS to make the recovery speed for low VOL level faster relatively.

When
"ALC recovery waiting counter reset level ≤ Output Signal < ALC limiter detection level"
during the ALC recovery operation, the waiting timer of ALC recovery operation is reset. When
"ALC recovery waiting counter reset level > Output Signal",
the waiting timer of ALC recovery operation starts.

ALC operations correspond to the impulse noise. When FRN bit = "0", the impulse noise is input, the ALC recovery operation becomes faster than a normal recovery operation. When large noise is input to a microphone instantaneously, the quality of small level in the large noise can be improved by this fast recovery operation. The speed of fast recovery operation is set by RFST1-0 bits (Table 40). When FRN bit = "1", the fast recovery does not operate though the impulse noise is input. Limiter amount of Fast recovery is set by FRATT bit (Table 41).

Table 37. ALC Recovery Operation Waiting Period

WTM1 bit	WTM0 bit		ALC Recovery Cycle			
			8kHz	16kHz	48kHz	
0	0	128/fs	16ms	8ms	2.7ms	(default)
0	1	256/fs	32ms	16ms	5.3ms	
1	0	512/fs	64ms	32ms	10.7ms	
1	1	1024/fs	128ms	64ms	21.3ms	

Table 38. ALC Recovery Gain Step

RGAIN2 bit	RGAIN1 bit	RGAIN0 bit	GAIN Step [dB]	GAIN Change Timing	
0	0	0	0.00424	1/fs	(default)
0	0	1	0.00212	1/fs	
0	1	0	0.00106	1/fs	
0	1	1	0.00106	2/fs	
1	0	0	0.00106	4/fs	
1	0	1	0.00106	8/fs	
1	1	0	0.00106	16/fs	
1	1	1	0.00106	32/fs	

Table 39. Reference Level of ALC Recovery Operation

REF7-0 bits	GAIN (dB)	Step	
F1H	+36.0	0.375dB	(default)
F0H	+35.625		
EFH	+35.25		
:	:		
E1H	+30.0		
:	:		
92H	+0.375		
91H	0.0		
90H	–0.375		
:	:		
06H	–52.125		
05H	–52.5		
04H~00H	MUTE		

Table 40. Fast Recovery Speed Setting (FRN bit = “0”)

RFST1-0 bits	Fast Recovery Gain Step [dB]	
00	0.0032	(default)
01	0.0042	
10	0.0064	
11	0.0127	

Table 41. Fast Recovery Reference Volume Attenuation Amount

FRATT bit	ATT Amount [dB]	ATT Switch Timing	
0	-0.00106	4/fs	(default)
1	-0.00106	16/fs	

3. The Volume at ALC Operation

The volume value during ALC operation is reflected in VOL7-0 bits. It is possible to check the current volume in 0.75dB step by reading the register value of VOL7-0 bits.

Table 42. Value of VOL7-0 bits

VOL7-0 bits	GAIN [dB]
FFH	+36.0 ≤ Gain
FEH	+35.25 ≤ Gain < +36.0
FCH	+34.5 ≤ Gain < +35.25
FAH	+33.75≤ Gain < +34.5
:	:
A2H	+0.75 ≤ Gain < +1.5
A0H	0.0 ≤ Gain < +0.75
9EH	-0.75 ≤ Gain < 0.0
:	:
12H	-53.25 ≤ Gain < -52.5
10H	-72 ≤ Gain < -53.25
00H	MUTE

4. Example of ALC Setting

Table 43 and Table 44 show the examples of the ALC setting for recording and playback path.

Table 43. Example of the ALC Setting (Recording)

Register Name	Comment	fs=8kHz		fs=48kHz	
		Data	Operation	Data	Operation
LMTH2-0	Limiter detection Level	010	–4.1dBFS	010	–4.1dBFS
FRN	Fast Recovery mode	0	Enable	0	Enable
WTM1-0	Recovery waiting period	01	32ms	11	21.3ms
REF7-0	Maximum gain at recovery operation	E1H	+30dB	E1H	+30dB
IVL7-0, IVR7-0	Gain of IVOL	E1H	+30dB	E1H	+30dB
RGAIN2-0	Recovery GAIN	000	0.00424dB	011	0.00106dB (2/fs)
RFST1-0	Fast Recovery GAIN	11	0.0127dB	00	0.0032dB
EQFC1-0	ALC EQ Frequency	00	fc1=100Hz, fc2=67Hz	10	fc1=150Hz, fc2=100Hz
ALCEQN	ALC EQ disable	0	Enable	0	Enable
ALC	ALC enable	1	Enable	1	Enable

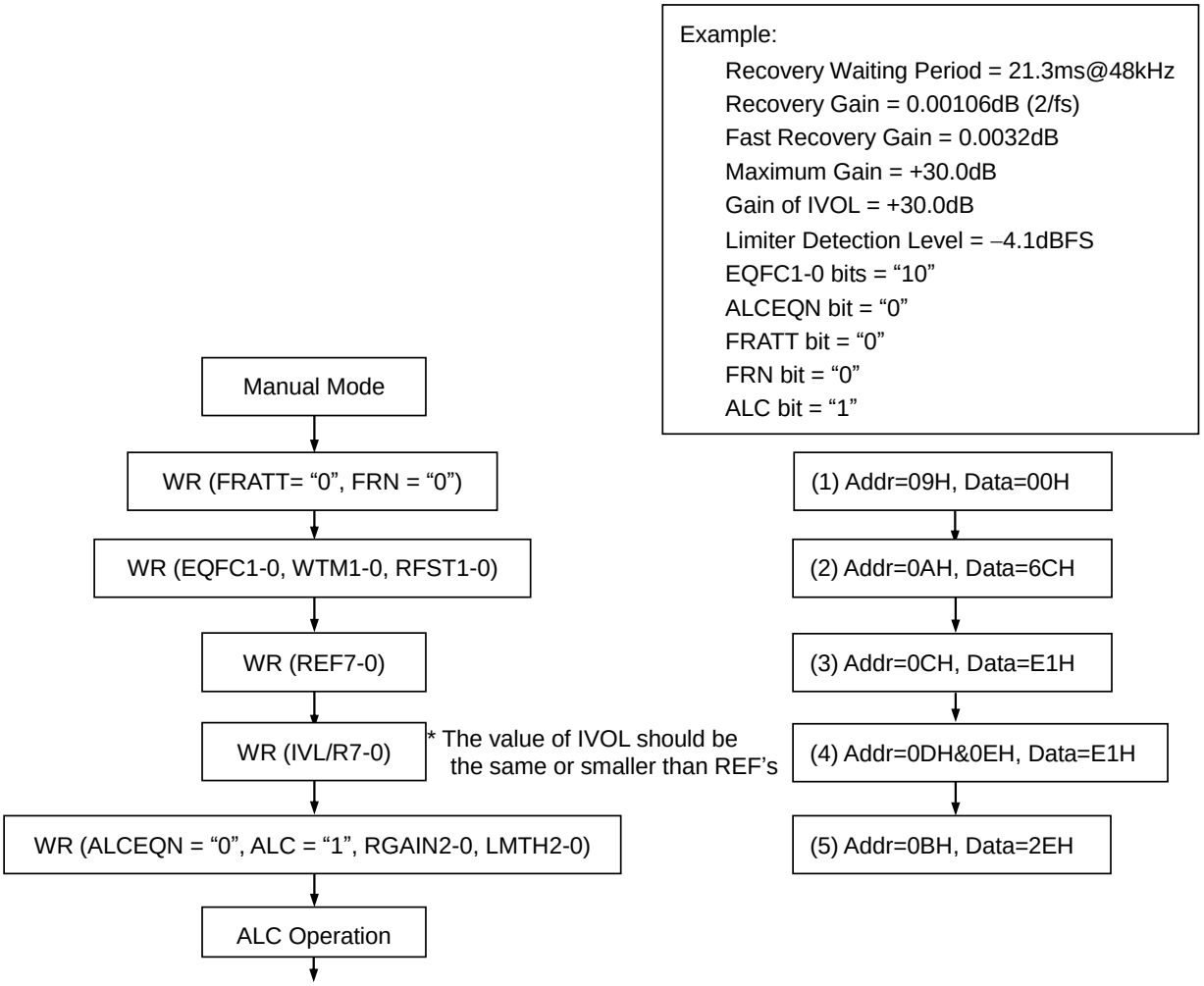
Table 44. Example of the ALC Setting (Playback)

Register Name	Comment	fs=8kHz		fs=48kHz	
		Data	Operation	Data	Operation
LMTH2-0	Limiter detection Level	010	–4.1dBFS	010	–4.1dBFS
FRN	Fast Recovery mode	0	Enable	0	Enable
WTM1-0	Recovery waiting period	01	32ms	11	21.3ms
REF5-0	Maximum gain at recovery operation	28H	+6dB	28H	+6dB
IVL7-0, IVR7-0	Gain of IVOL	91H	0dB	91H	0dB
RGAIN2-0	Recovery GAIN	000	0.00424dB	011	0.00106dB (2/fs)
RFST1-0	Fast Recovery GAIN	11	0.0127dB	00	0.0032dB
EQFC1-0	ALC EQ Frequency	00	fc1=100Hz, fc2=67Hz	10	fc1=150Hz, fc2=100Hz
ALCEQN	ALC EQ disable	0	Enable	0	Enable
ALC	ALC enable	1	Enable	1	Enable

5. Example of registers set-up sequence of ALC Operation

The following registers must not be changed during ALC operation. These bits must be changed after ALC operation is stopped by ALC bit = “0”. ALC output is “0” data until the AK4951A becomes manual mode after writing “0” to ALC bit.

LMTH2-0, WTM1-0, RGAIN2-0, REF7-0, RFST1-0, EQFC1-0, FRATT, FRN and ALCEQN bits



WR: Write

Figure 39. Registers Set-up Sequence at ALC Operation (Recording path)

■ Input Digital Volume (Manual Mode)

The input digital volume becomes manual mode when ALC bit is set to “0” while ADCPF bit is “1”. This mode is used in the cases shown below.

1. After exiting reset state, when setting up the registers for ALC operation (LMTH and etc.)
2. When the registers for ALC operation (Limiter period, Recovery period and etc.) are changed. For example; when the sampling frequency is changed.
3. When IVOL is used as a manual volume control.

IVL7-0 and IVR7-0 bits set the gain of the volume control (Table 45). Lch and Rch volumes are set individually by IVL7-0 and IVR7-0 bits when IVOLC bit = “0”. IVL7-0 bits control both Lch and Rch volumes together when IVOLC bit = “1”.

This volume has a soft transition function. Therefore no switching noise occurs during the transition. IVTM bit set the transition time (Table 46). When IVTM bit = “1”, it takes 944/fs (19.7ms@fs=48kHz) from F1H (+36dB) to 05H (-52.5dB). The volume is muted after transitioned to -72dB in the period set by IVTM bit when changing the volume from 05H (-52.5dB) to 00H (MUTE).

Table 45. Input Digital Volume Setting

IVL7-0 bits IVR7-0 bits	GAIN (dB)	Step	
F1H	+36.0	0.375dB	
F0H	+35.625		
EFH	+35.25		
:	:		
E2H	+30.375		
E1H	+30.0		(default)
E0H	+29.625		
:	:		
92H	+0.375		
91H	0.0		
90H	–0.375		
:	:		
06H	–52.125		
05H	–52.5		
04H~00H	MUTE		

Table 46. Transition Time of Input Digital Volume

IVTM bit	Transition Time of Input Digital Volume IVL/R7-0 bits = “F1H” → “05H”			
	Setting Value	fs=8kHz	fs=48kHz	
0	236/fs	29.5ms	4.9ms	
1	944/fs	118ms	19.7ms	(default)

If IVL7-0 or IVR7-0 bits are written during PMPFIL bit = “0”, IVOL operation starts with the written values after PMPFIL bit is changed to “1”.

■ Sidetone Digital Volume

The AK4951A has the digital volume control (4 levels, 6dB step) for the programmable filter output.

Table 47. Sidetone Digital Volume

PFVOL1-0 bits	Gain	
00	0dB	(default)
01	-6dB	
10	-12dB	
11	-18dB	

■ DAC Input Selector

PFDAC1-0 bits select the signal of the DAC input or set the data mixing for each channel data.

Table 48. DAC Input Selector

PFDAC1 bit	PFDAC0 bit	DAC Lch Input Signal	DAC Rch Input Signal	
0	0	SDTI Lch	SDTI Rch	(default)
0	1	PFVOL Lch Output	PFVOL Rch Output	
1	0	[(SDTI Lch) + (PFVOL Lch)]/2	[(SDTI Rch) + (PFVOL Rch)]/2	
1	1	N/A	N/A	

(N/A: Not available)

■ DAC Mono/Stereo Mode

Mono mixing outputs are available by setting MONO1-0 bits. Input data from the SDTI pin can be converted to mono signal [(L+R)/2] and are output from DAC.

Table 49. Mono/Stereo DAC operation

MONO1 bit	MONO0 bit	DAC Lch Output Signal	DAC Rch Output Signal	
0	0	Lch	Rch	(default)
0	1	Lch	Lch	
1	0	Rch	Rch	
1	1	(Lch+Rch)/2	(Lch+Rch)/2	

■ Output Digital Volume

The AK4951A has a digital output volume (205 levels, 0.5dB step, Mute). The volume is included in front of a DAC block. The input data of DAC is changed from +12 to –89.5dB or MUTE. DVL7-0 bits control both Lch and Rch volumes together when DVOLC bit = “1” (default). Lch and Rch volumes are set individually by DVL7-0 and DVR7-0 bits when DVOLC bit = “0”. This volume has soft transition function. In automatic attenuation, the volume is attenuated by soft transition in 204/fs or 816/fs to reduce switching noises. When DVTM bit = “0”, it takes 816/fs (17.0ms@fs=48kHz) from 00H (+12dB) to CCH (MUTE).

Table 50. Output Digital Volume Setting

DVL7-0 bits DVR7-0 bits	Gain	Step	
00H	+12.0dB	0.5dB	(default)
01H	+11.5dB		
02H	+11.0dB		
:	:		
18H	0dB		
:			
CAH	−89.0dB		
CBH	−89.5dB		
CCH~FFH	Mute (− ∞)		

Table 51. Transition Time Setting of Output Digital Volume

DVTM bit	Transition Time between DVL/R7-0 bits = 00H and CCH			
	Setting	fs=8kHz	fs=48kHz	
0	816/fs	102ms	17.0ms	(default)
1	204/fs	25.5ms	4.3ms	

■ Soft Mute

Soft mute operation is performed in the digital domain. When the SMUTE bit is set "1", the output signal is attenuated by -∞ ("0") from the value (ATT DATA) set by DVL/R7-0 bits during the cycle set by DVTM bit. When the SMUTE bit is returned to "0", the mute is cancelled and the output attenuation gradually changes to ATT DATA from -∞ during the cycle set by DVTM bit. If the soft mute is cancelled within the cycle set by DVTM bit after starting the operation, the attenuation is discontinued and returned to ATT DATA. The soft mute is effective for changing the signal source without stopping the signal transaction.

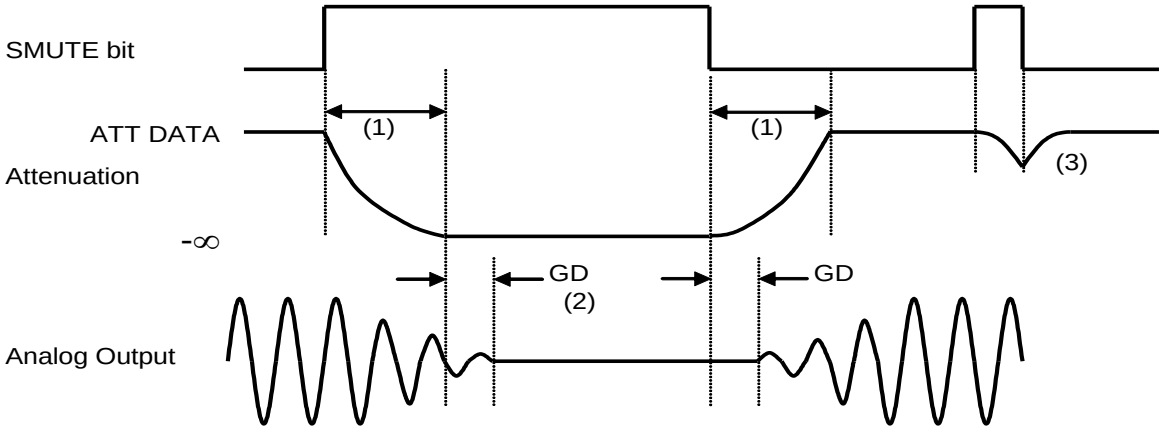


Figure 40. Soft Mute Function

(1) The input signal is attenuated to −∞ ("0") in the cycle set by DVTM bit. When ATT DATA = +12dB (DVL/R7-0 bits = 00H), 816/fs = 17ms@ fs=48kHz, DVTM bit= "0".
(2) Analog output corresponding to digital input has group delay (GD).
(3) If soft mute is cancelled before attenuating to −∞, the attenuation is discounted and returned to the level set by DVL/R7-0 bits within the same cycle.

■ BEEP Input

When BEEPS bit is set to “1” during PMBP = PMSL = SPLSN bits = “1”, the input signal from the RIN3/BEEP pin is output to the speaker-amp (LOSEL bit = “0”) or stereo line output (LOSEL bit = “1”). When BEEPH bit is set to “1” during PMHPL or PMHPR bit = “1”, the input signal from the RIN3/BEEP pin is output to the stereo headphone amplifier. BPLVL3-0 bits set the gain of BEEP-Amp, and the total gain is defined according to SPKG1-0 bits setting. When the BEEP signal is output to the stereo headphone amplifier, AK4951A operates without the system clock. In order to operate the charge pump circuit, it is necessary to power up the internal oscillator (PMOSC bit = “1”).

When PMDAC bit = “1” and PMHPL bit or PMHPR bit = “1”, switching noise of connection between the BEEP generating circuit and headphone amplifier can be suppressed by soft transition. The transition time of ON/OFF switching is set by PTS1-0 bits. Soft transition Enable/Disable is controlled by MOFF bit. When this bit is “1”, soft transition is disabled and the headphone is switched ON/OFF immediately.

Table 52. BEEP ON/OFF Transition Time (MOFF bit = “0”)

PTS1 bit	PTS0 bit	ON/OFF Time				
		8kHz ≤ fs ≤ 24kHz		24kHz < fs ≤ 48kHz		
0	0	64/fs	2.7~8ms	128/fs	2.7~5.3ms	
0	1	128/fs	5.3~16ms	256/fs	5.3~10.7ms	(default)
1	0	256/fs	10.7~32ms	512/fs	10.7~21.3ms	
1	1	512/fs	21.3~64ms	1024/fs	21.3~42.7ms	

BPVCM bit set the common voltage of BEEP input amplifier (Table 53).

Table 53. Common Potential Setting of BEEP-Amp

BPVCM bit	BEEP-Amp Common Voltage (typ)	
0	1.15V	(default)
1	1.65V (Note 14, Note 40)	

Note 14. The maximum value is AVDD Vpp when BPVCM bit = “1”. However, a click noise may occur when the amplitude after BEEP-Amp is 0.5Vpp or more. (set by BPLVL3-0 bits)

Note 40. When the BEEP signal is output to the speaker amplifier and BPVCM bit = “1”, SVDD must be supplied 2.8V or more.

Input BEEP gain is controlled by BPLVL3-0 bits (Table 54).

Table 54. BEEP Output Gain Setting

BPLVL3 bit	BPLVL2 bit	BPLVL1 bit	BPLVL0 bit	BEEP Gain	
0	0	0	0	0dB	(default)
0	0	0	1	−6dB	
0	0	1	0	−12dB	
0	0	1	1	−18dB	
0	1	0	0	−24dB	
0	1	0	1	−30dB	
0	1	1	0	−33dB	
0	1	1	1	−36dB	
1	0	0	0	−39dB	
1	0	0	1	−42dB	
Others				N/A	

(N/A: Not available)

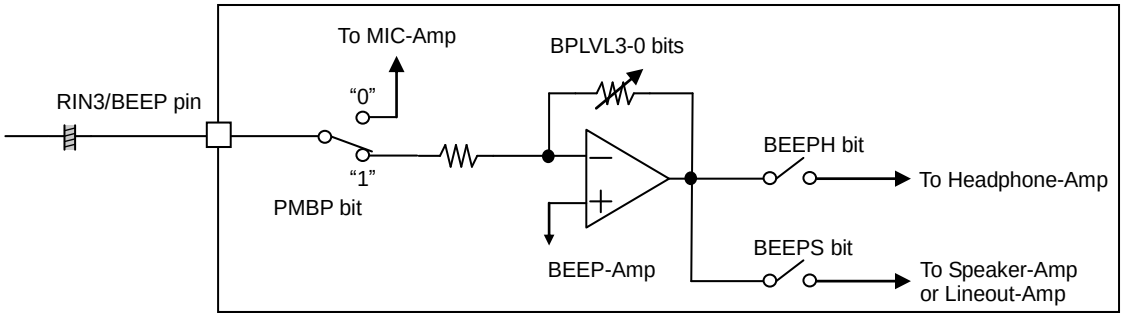


Figure 41. Block Diagram of BEEP pin

■ Charge Pump Circuit

The internal charge pump circuit generates negative voltage (VEE) from AVDD voltage. The VEE voltage is used for the headphone amplifier. The charge pump circuit starts operation when PMHPL or PMHPR bit = "1". PMVCM bit must be set "1" to power up the charge pump circuit. When the BEEP signal is output to the stereo headphone amplifier without the system clock, the charge pump circuit can be operated using the internal oscillator by setting PMOSC bit = "1". The operating frequency of the internal oscillator is 2.68MHz (typ) and the power up time of the internal oscillator is 1.1μs (typ).

The power-up time of the charge pump circuit is 12.1ms (max). The headphone amplifier and speaker amplifier will be powered up after the charge pump circuit is powered up (when PMHPL or PMHPR bit = "1"). The operating frequency of the charge pump circuit is dependent on the sampling frequency.

■ Headphone Amplifier (HPL/HPR pins)

The positive voltage of the headphone amplifier uses the power supply to the DVDD pin, therefore 150mA of the maximum power supply capacity is needed. The internal charge pump circuit generates negative voltage (VEE) from AVDD voltage. The headphone amplifier output is single-ended and centered around on VSS (0V). Therefore, the capacitor for AC-coupling can be removed. The minimum load resistance is 16Ω.

<External Circuit of Headphone Amplifier>

An oscillation prevention circuit (0.22μF±20% capacitor and 33Ω±20% resistor) should be put because it has the possibility that Headphone Amplifier oscillates in type of headphone.

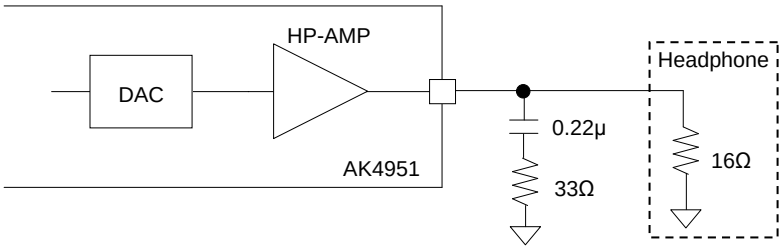


Figure 42. External Circuit of Headphone

When PMHPL, PMHPR bits = "1", headphone outputs are in normal operation. By setting PMHPL and PMHPR bits = "0", the headphone-amps are powered-down completely. At that time, the HPL and HPR pins go to VSS voltage via the internal pulled-down resistor when HPZ bit = "0". The pulled-down resistor is 10Ω (typ). Crosstalk can be reduced by bringing the HPL and HPR pins to Hi-Z state when it occurs on the path from speaker output to headphone output by enabling the speaker output in this pulled-down status of the HPL and HPR pins. The HPL and HPR pins become Hi-Z state by setting HPZ bit to "1" when PMHPL and PMHPR bit = "0". The headphone-amps can be powered-up/down regardless the HPZ bit setting.

The power-up time of the headphone amplifiers is max. 34.2ms (internal oscillator: 66.2ms), and power-down is executed immediately.

Table 55. Headphone Output Status

PMVCM bit	PMHPL/R bits	HPZ bit	Mode	HPL/R pins
x	0	0	Power-down & Mute	Pull-down by 10Ω (typ)
x	0	1	Power-down	Hi-Z
1	1	0	Normal Operation	Normal Operation
1	1	1	Normal Operation	Normal Operation

(default)

(x: Do not care)

■ Speaker Output (SPP/SPN pins, LOSEL bit = "0")

When LOSEL bit = "0", the DAC output signal is input to the speaker amplifier as mono signal [(L+R)/2]. The speaker amplifier has mono output as it is BTL capable. The gain and output level are set by SPKG1-0 bits. The output level depends on SVDD and SPKG1-0 bits setting.

Table 56. SPK-Amp Gain

SPKG1-0 bits	Gain	SPK-Amp Output Level (DAC Input =0dBFS, SVDD=3.3V)
00	+6.4dB	3.37Vpp
01	+8.4dB	4.23Vpp (Note 41)
10	+11.1dB	5.33Vpp (Note 41)
11	+14.9dB	8.47Vpp (SVDD=5.0V; Note 41)

(default)

Note 41. The output level is calculated on the assumption that the signal is not clipped. However, in the actual case, the SPK-Amp output signal is clipped when DAC outputs 0dBFS signal. The SPK-Amp output level should be kept under 4.0Vpp (SVDD=3.3V) by adjusting digital volume to prevent clipped noise.

< Speaker-Amp Control Sequence >

The speaker amplifier is powered-up/down by PMSL bit. When PMSL bit is "0" at LOSEL bit = "0", both SPP and SPN pins are pulled-down to VSS3 by 100kΩ (typ). When PMSL bit is "1" and SLPSN bit is "0" at LOSEL bit = "0", the speaker amplifier enters power-save mode. In this mode, the SPP pin is placed in Hi-Z state and the SPN pin outputs SVDD/2 voltage (Note 42).

When the PMSL bit is "1" at LOSEL bit = "0" after the PDN pin is changed from "L" to "H", the SPP and SPN pins rise up in power-save mode. In this mode, the SPP pin is placed in a Hi-Z state and the SPN pin goes to SVDD/2 voltage (Note 42). Because the SPP and SPN pins rise up in power-save mode, pop noise can be reduced. When the AK4951A is powered-down (PMSL bit = "0"), pop noise can also be reduced by first entering power-save-mode.

Note 42. When the SVDD more than 4.6V is supplied, the voltage cannot rise up to SVDD/2.

Table 57 Speaker-Amp Mode Setting

PMSL bit	SLPSN bit	Mode	SPP pin	SPN pin
0	x	Power-down	Pull-down to VSS3	Pull-down to VSS3
1	0	Power-save	Hi-Z	SVDD/2 (Note 42)
	1	Normal Operation	Normal Operation	Normal Operation

(default)

(x: Do not care)

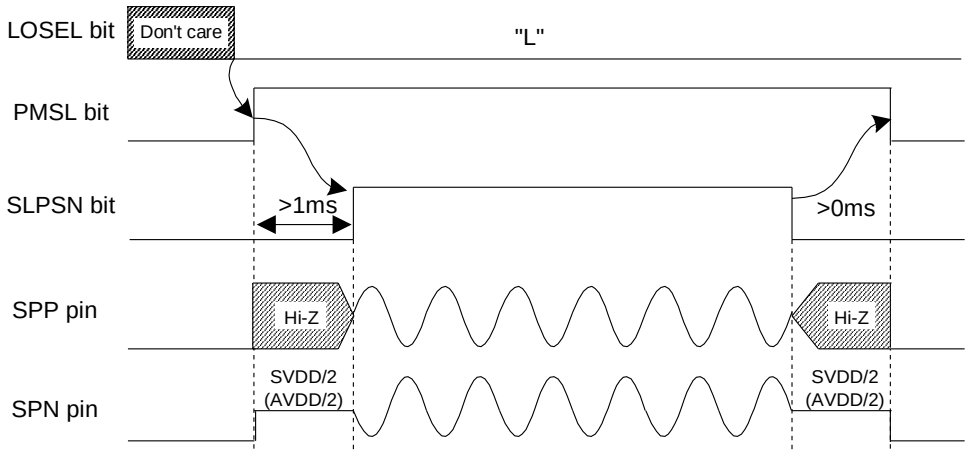


Figure 43. Power-up/Power-down Timing for Speaker-Amp

■ Thermal Shutdown Function

When the internal temperature of the device rises up irregularly (e.g. Output pins of speaker-amp or headphone-amp are shortened), the speaker-amp, the headphone-amp and charge-pump circuit are automatically powered down and then THDET bit becomes “1” (thermal shutdown). When TSDSEL bit = “0” (default), the internal temperature goes down and the thermal shutdown is released, the speaker-amp, the headphone-amp and charge-pump circuit is powered up automatically and THDET bit returns to “0”. When TSDSEL bit = “1”, these blocks will not return to a normal operation until being reset by the PDN pin. THDET bit becomes “0” by this PDN pin reset.

■ Stereo Line Output (LOUT/ROUT pin, LOSEL bit = "1")

When LOSEL bit is set to "1", L and R channel signals of DAC are output in single-ended format via LOUT and ROUT pins. The stereo line output is valid at SVDD = 2.8~3.5V. The same voltage as AVDD must be supplied to the stereo lineout. When DACL bit is "0" at LOSEL = PMSL = SLPSN bits = "1", output signals are muted and LOUT and ROUT pins output common voltage. The load impedance is 10kΩ (min.). When PMSL bit = "0" at LOSEL = SLPSN bits = "1", the stereo line output enters power-down mode and the output is pulled-down to VSS3 by 100kΩ (typ). Pop noise at power-up/down can be reduced by changing PMSL bit when SLPSN bit = "0" at LOSEL bit = "1". In this case, output signal line should be pulled-down to VSS by 22kΩ after AC coupled as Figure 45. Rise/Fall time is 300ms (max) when C=1μF and R_L=10kΩ. When LOSEL = PMSL = SLPSN bits = "1", stereo line output is in normal operation.

LVCM1-0 bits set the gain of stereo line output.
The DAC output signal cannot be output from stereo line out and headphone amplifier at the same time. When the DAC output signal is output from stereo line out, the headphone amplifier should be powered down (PMHPL=PMHPR bits="0").

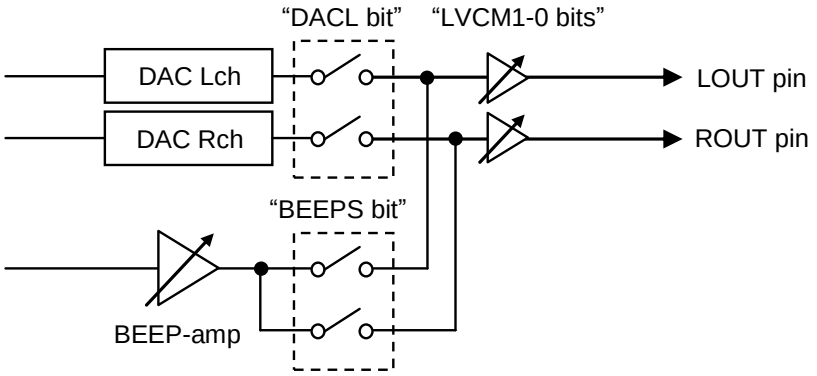


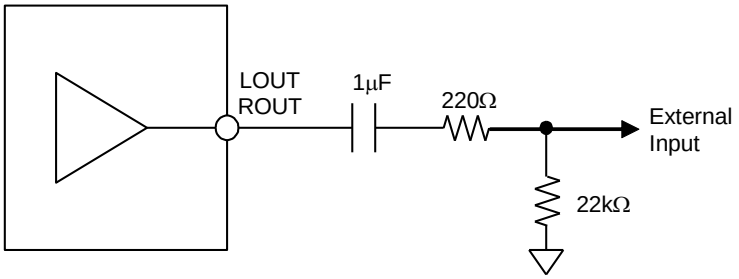
Figure 44. Stereo Line Output

Table 58. Stereo Line Output Mode Select

PMSL bit	SLPSN bit	Mode	LOUT/ROUT pins	
0	0	Power Down	Fall-down to VSS3	(default)
	1	Power Down	Pull-down to VSS3	
1	0	Power Save	Rise up to Common Voltage	
	1	Normal Operation	Normal Operation	

Table 59. Stereo Lineout Volume Setting

LVCM1-0 bits	SVDD (=AVDD)	Gain	Common Voltage (typ)	
00	2.8 ~ 3.6V	0dB	1.3V	
01	3.0 ~ 3.6V	+2dB	1.5V	(default)
10	2.8 ~ 3.6V	+2dB	1.3V	
11	3.0 ~ 3.6V	+4dB	1.5V	



Note 43. If the value of 22kΩ resistance at pop noise reduction circuit is increased, the power-up time of stereo line output is increased but the pop noise level is not decreased. Do not use a resistor less than 22kΩ at the pop noise reduction circuit since the line output drivability is minimum 10kΩ.

Figure 45. External Circuit for Stereo Line Output (in case of using a Pop Noise Reduction Circuit)

[Stereo Line Output Control Sequence (in case of using a Pop Noise Reduction Circuit)]

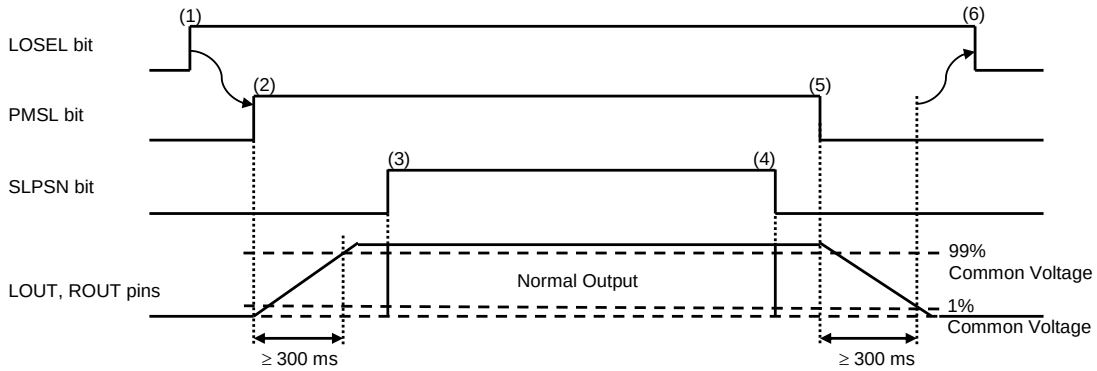


Figure 46. Stereo Line Output Control Sequence (in case of using a Pop Noise Reduction Circuit)

(1) Set LOSEL bit = “1”. Enable stereo line output.
(2) Set PMSL bit = “1”. Stereo line output exits power-down mode.
LOUT and ROUT pins rise up to common voltage. Rise time to 99% common voltage is 200ms (max. 300ms) when C=1μF.
(3) Set SLPSN bit = “0” after LOUT and ROUT pins rise up. Stereo line output exits power-save mode.
Stereo line output is enabled.
(4) Set SLPSN bit = “1”. Stereo line output enters power-save mode.
(5) Set PMSL bit = “0”. Stereo line output enters power-down mode.
LOUT and ROUT pins fall down to 1% of the common voltage. Fall time is 200ms (max. 300ms) when C=1μF.
(6) Set LOSEL bit = “0” after wait time (≥300ms). Disable stereo line output.

[Stereo Line Output Control Sequence (SLPSN bit = “1”: in case of not using a Pop Noise Reduction Circuit)]

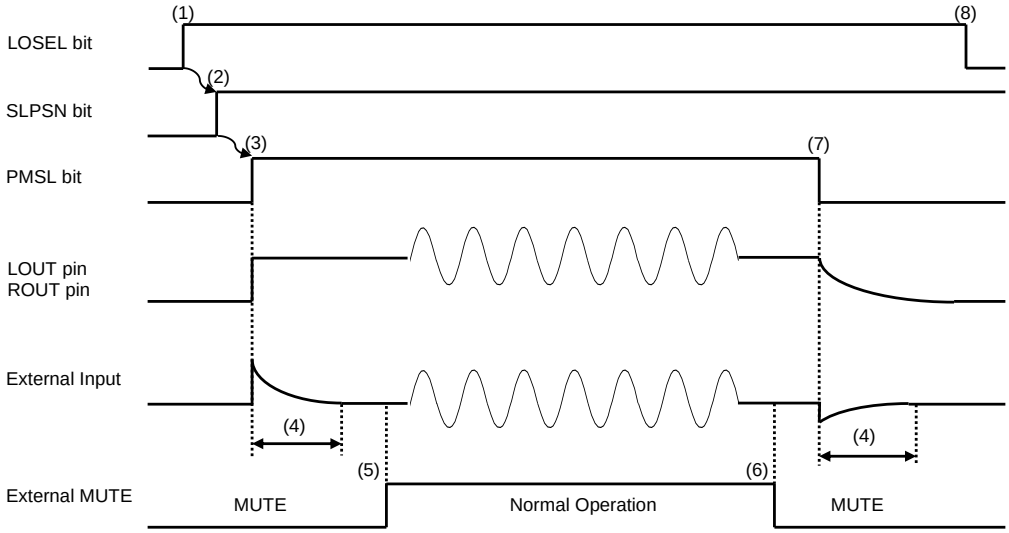


Figure 47. Stereo Line Output Control Sequence
(SLPSN bit = “1”: in case of not using a Pop Noise Reduction Circuit)

(1) Set LOSEL bit = “1”. Enable stereo line output.
(2) Set SLPSN bit = “1”. Disable pop noise reduction circuit.
(3) Set PMSL bit = “1”. Stereo line output is powered-up.
LOUT and ROUT pins rise up to common voltage.
(4) Time constant is defined according to external capacitor (C) and resistor (R_L).
(5) Release external MUTE when the external input is stabled.
Stereo line output is enabled.
(6) Set external MUTE ON
(7) Set PMSL bit = “0”. Stereo line output is powered-down.
LOUT and ROUT pins fall down.
(8) Set LOSEL bit = “0” after wait time (≥300ms). Disable stereo line output.

■ Regulator Block

The AK4951A integrates a regulator. The 3.3V (typ) power supply voltage from the AVDD pin is converted to 2.3V (typ) by the regulator and supplied to the analog blocks (MIC-Amp, ADC, DAC, BEEP). The regulator is powered up by PMVCM bit = “1”, and powered down by PMVCM = “0”. Connect a 2.2μF (± 20%) capacitor to the REGFIL pin to reduce noise on AVDD.

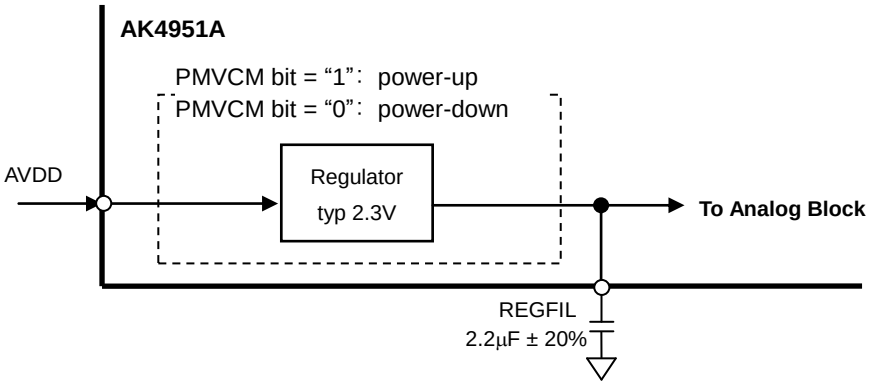


Figure 48 Regulator Block

■ Serial Control Interface

The AK4951A supports the fast-mode I^2C Bus (max: 400kHz). Pull-up resistors at the SDA and SCL pins must be connected to a voltage in the range from TVDD or more to 6V or less.

1. WRITE Operations

Figure 49 shows the data transfer sequence for the I^2C Bus mode. All commands are preceded by a START condition. A HIGH to LOW transition on the SDA line while SCL is HIGH indicates a START condition (Figure 55). After the START condition, a slave address is sent. This address is 7 bits long followed by the eighth bit that is a data direction bit (R/W). The most significant seven bits of the slave address are fixed as “0010010” (Figure 50). If the slave address matches that of the AK4951A, the AK4951A generates an acknowledge and the operation is executed. The master must generate the acknowledge-related clock pulse and release the SDA line (HIGH) during the acknowledge clock pulse (Figure 56). A R/W bit value of “1” indicates that the read operation is to be executed, and “0” indicates that the write operation is to be executed.

The second byte consists of the control register address of the AK4951A. The format is MSB first, and those most significant 1bit is fixed to zero (Figure 51). The data after the second byte contains control data. The format is MSB first, 8bits (Figure 52). The AK4951A generates an acknowledge after each byte is received. Data transfer is always terminated by a STOP condition generated by the master. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition (Figure 55).

The AK4951A can perform more than one byte write operation per sequence. After receipt of the third byte the AK4951A generates an acknowledge and awaits the next data. The master can transmit more than one byte instead of terminating the write cycle after the first data byte is transferred. After receiving each data packet the internal address counter is incremented by one, and the next data is automatically taken into the next address. The address counter will “roll over” to 00H and the previous data will be overwritten if the address exceeds “4FH” prior to generating a stop condition.

The data on the SDA line must remain stable during the HIGH period of the clock. HIGH or LOW state of the data line can only be changed when the clock signal on the SCL line is LOW (Figure 57) except for the START and STOP conditions.

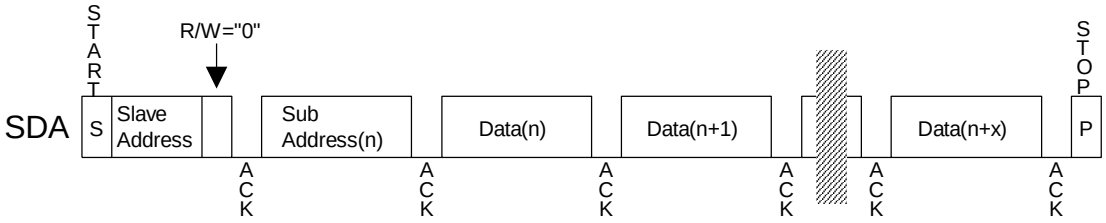


Figure 49. Data Transfer Sequence at I^{2}C Bus Mode

0	0	1	0	0	1	0	R/W

Figure 50. The First Byte

0	A6	A5	A4	A3	A2	A1	A0

Figure 51. The Second Byte

D7	D6	D5	D4	D3	D2	D1	D0

Figure 52. The Third Byte

2. READ Operations

Set the R/W bit = “1” for the READ operation of the AK4951A. After transmission of data, the master can read the next address’s data by generating an acknowledge instead of terminating the write cycle after the receipt of the first data word. After receiving each data packet the internal address counter is incremented by one, and the next data is automatically taken into the next address. The address counter will “roll over” to 00H and the data of 00H will be read out if the address exceeds “4FH” of Register map prior to generating a stop condition.

The AK4951A supports two basic read operations: CURRENT ADDRESS READ and RANDOM ADDRESS READ.

2-1. CURRENT ADDRESS READ

The AK4951A has an internal address counter that maintains the address of the last accessed word incremented by one. Therefore, if the last access (either a read or write) were to address “n”, the next CURRENT READ operation would access data from the address “n+1”. After receipt of the slave address with R/W bit “1”, the AK4951A generates an acknowledge, transmits 1-byte of data to the address set by the internal address counter and increments the internal address counter by 1. If the master does not generate an acknowledge but generates a stop condition instead, the AK4951A ceases the transmission.

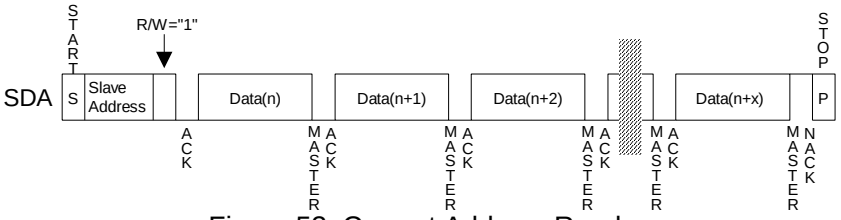


Figure 53. Current Address Read

2-2. RANDOM ADDRESS READ

The random read operation allows the master to access any memory location at random. Prior to issuing the slave address with the R/W bit “1”, the master must first perform a “dummy” write operation. The master issues a start request, a slave address (R/W bit = “0”) and then the register address to read. After the register address is acknowledged, the master immediately reissues the start request and the slave address with the R/W bit “1”. The AK4951A then generates an acknowledge, 1 byte of data and increments the internal address counter by 1. If the master does not generate an acknowledge but generates a stop condition instead, the AK4951A ceases the transmission.

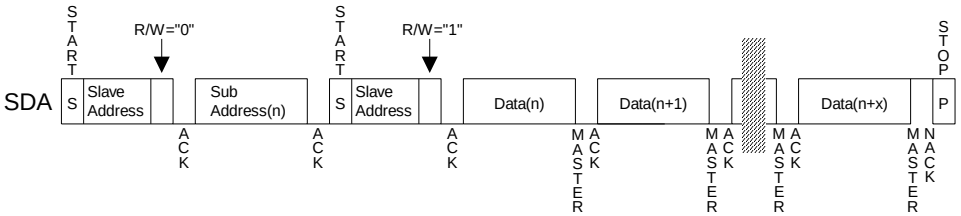


Figure 54. Random Address Read

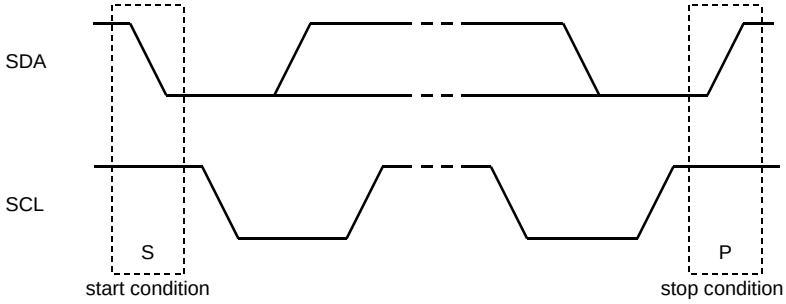


Figure 55. Start Condition and Stop Condition

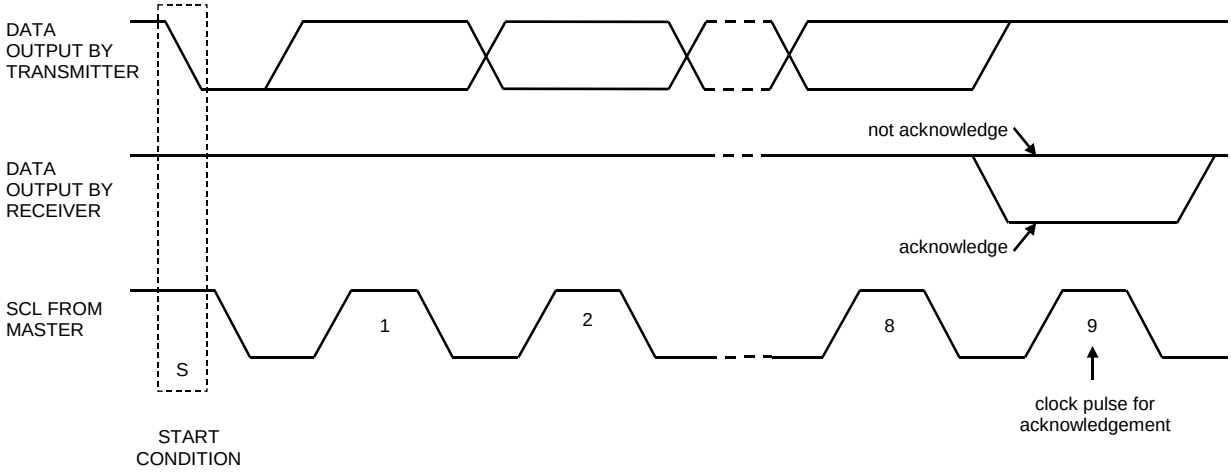


Figure 56. Acknowledge (I^2C Bus)

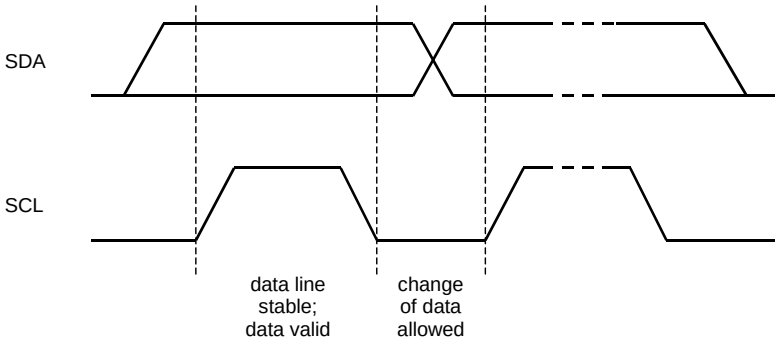


Figure 57. Bit Transfer (I^2C Bus)

■ Register Map

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Power Management 1	PMPFIL	PMVCM	PMBP	0	0	PMDAC	PMADR	PMADL
01H	Power Management 2	PMOSC	0	PMHPR	PMHPL	M/S	PMPLL	PMSL	LOSEL
02H	Signal Select 1	SLPSN	MGAIN3	DACS	MPSEL	PMMP	MGAIN2	MGAIN1	MGAIN0
03H	Signal Select 2	SPKG1	SPKG0	VODETN	MICL	INL1	INL0	INR1	INR0
04H	Signal Select 3	LVCM1	LVCM0	DACL	0	PTS1	PTS0	MONO1	MONO0
05H	Mode Control 1	PLL3	PLL2	PLL1	PLL0	BCKO	CKOFF	DIF1	DIF0
06H	Mode Control 2	CM1	CM0	0	0	FS3	FS2	FS1	FS0
07H	Mode Control 3	TSDSEL	THDET	SMUTE	DVOLC	0	IVOLC	0	0
08H	Digital MIC	0	0	PMDMR	PMDML	DCLKE	0	DCLKP	DMIC
09H	Timer Select	ADRST1	ADRST0	FRATT	FRN	0	0	MOFF	DVTM
0AH	ALC Timer Select	0	IVTM	EQFC1	EQFC0	WTM1	WTM0	RFST1	RFST0
0BH	ALC Mode Control 1	ALCEQN	LMTH2	ALC	RGAIN2	RGAIN1	RGAIN0	LMTH1	LMTH0
0CH	ALC Mode Control 2	REF7	REF6	REF5	REF4	REF3	REF2	REF1	REF0
0DH	Lch Input Volume Control	IVL7	IVL6	IVL5	IVL4	IVL3	IVL2	IVL1	IVL0
0EH	Rch Input Volume Control	IVR7	IVR6	IVR5	IVR4	IVR3	IVR2	IVR1	IVR0
0FH	ALC Volume	VOL7	VOL6	VOL5	VOL4	VOL3	VOL2	VOL1	VOL0
10H	Lch MIC Gain Setting	MGL7	MGL6	MGL5	MGL4	MGL3	MGL2	MGL1	MGL0
11H	Rch MIC Gain Setting	MGR7	MGR6	MGR5	MGR4	MGR3	MGR2	MGR1	MGR0
12H	BEEP Control	HPZ	BPVCM	BEEPS	BEEPH	BPLVL3	BPLVL2	BPLVL1	BPLVL0
13H	Lch Digital Volume Control	DVL7	DVL6	DVL5	DVL4	DVL3	DVL2	DVL1	DVL0
14H	Rch Digital Volume Control	DVR7	DVR6	DVR5	DVR4	DVR3	DVR2	DVR1	DVR0
15H	EQ Common Gain Select	0	0	0	EQC5	EQC4	EQC3	EQC2	0
16H	EQ2 Common Gain Setting	EQ2G5	EQ2G4	EQ2G3	EQ2G2	EQ2G1	EQ2G0	EQ2T1	EQ2T0
17H	EQ3 Common Gain Setting	EQ3G5	EQ3G4	EQ3G3	EQ3G2	EQ3G1	EQ3G0	EQ3T1	EQ3T0
18H	EQ4 Common Gain Setting	EQ4G5	EQ4G4	EQ4G3	EQ4G2	EQ4G1	EQ4G0	EQ4T1	EQ4T0
19H	EQ5 Common Gain Setting	EQ5G5	EQ5G4	EQ5G3	EQ5G2	EQ5G1	EQ5G0	EQ5T1	EQ5T0
1AH	Auto HPF Control	0	0	AHPF	SENC2	SENC1	SENC0	STG1	STG0
1BH	Digital Filter Select 1	0	0	0	0	0	HPFC1	HPFC0	HPFAD
1CH	Digital Filter Select 2	GN1	GN0	EQ0	FIL3	0	0	LPF	HPF
1DH	Digital Filter Mode	0	0	PFVOL1	PFVOL0	PFDAC1	PFDAC0	ADCPF	PFSDO
1EH	HPF2 Co-efficient 0	F1A7	F1A6	F1A5	F1A4	F1A3	F1A2	F1A1	F1A0
1FH	HPF2 Co-efficient 1	0	0	F1A13	F1A12	F1A11	F1A10	F1A9	F1A8
20H	HPF2 Co-efficient 2	F1B7	F1B6	F1B5	F1B4	F1B3	F1B2	F1B1	F1B0
21H	HPF2 Co-efficient 3	0	0	F1B13	F1B12	F1B11	F1B10	F1B9	F1B8
22H	LPF Co-efficient 0	F2A7	F2A6	F2A5	F2A4	F2A3	F2A2	F2A1	F2A0
23H	LPF Co-efficient 1	0	0	F2A13	F2A12	F2A11	F2A10	F2A9	F2A8
24H	LPF Co-efficient 2	F2B7	F2B6	F2B5	F2B4	F2B3	F2B2	F2B1	F2B0
25H	LPF Co-efficient 3	0	0	F2B13	F2B12	F2B11	F2B10	F2B9	F2B8
26H	FIL3 Co-efficient 0	F3A7	F3A6	F3A5	F3A4	F3A3	F3A2	F3A1	F3A0
27H	FIL3 Co-efficient 1	F3AS	0	F3A13	F3A12	F3A11	F3A10	F3A9	F3A8
28H	FIL3 Co-efficient 2	F3B7	F3B6	F3B5	F3B4	F3B3	F3B2	F3B1	F3B0
29H	FIL3 Co-efficient 3	0	0	F3B13	F3B12	F3B11	F3B10	F3B9	F3B8
2AH	EQ Co-efficient 0	E0A7	E0A6	E0A5	E0A4	E0A3	E0A2	E0A1	E0A0
2BH	EQ Co-efficient 1	E0A15	E0A14	E0A13	E0A12	E0A11	E0A10	E0A9	E0A8
2CH	EQ Co-efficient 2	E0B7	E0B6	E0B5	E0B4	E0B3	E0B2	E0B1	E0B0
2DH	EQ Co-efficient 3	0	0	E0B13	E0B12	E0B11	E0B10	E0B9	E0B8
2EH	EQ Co-efficient 4	E0C7	E0C6	E0C5	E0C4	E0C3	E0C2	E0C1	E0C0
2FH	EQ Co-efficient 5	E0C15	E0C14	E0C13	E0C12	E0C11	E0C10	E0C9	E0C8

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
30H	Digital Filter Select 3	0	0	0	EQ5	EQ4	EQ3	EQ2	EQ1
31H	Device Information	REV3	REV2	REV1	REV0	DVN3	DVN2	DVN1	DVN0
32H	E1 Co-efficient 0	E1A7	E1A6	E1A5	E1A4	E1A3	E1A2	E1A1	E1A0
33H	E1 Co-efficient 1	E1A15	E1A14	E1A13	E1A12	E1A11	E1A10	E1A9	E1A8
34H	E1 Co-efficient 2	E1B7	E1B6	E1B5	E1B4	E1B3	E1B2	E1B1	E1B0
35H	E1 Co-efficient 3	E1B15	E1B14	E1B13	E1B12	E1B11	E1B10	E1B9	E1B8
36H	E1 Co-efficient 4	E1C7	E1C6	E1C5	E1C4	E1C3	E1C2	E1C1	E1C0
37H	E1 Co-efficient 5	E1C15	E1C14	E1C13	E1C12	E1C11	E1C10	E1C9	E1C8
38H	E2 Co-efficient 0	E2A7	E2A6	E2A5	E2A4	E2A3	E2A2	E2A1	E2A0
39H	E2 Co-efficient 1	E2A15	E2A14	E2A13	E2A12	E2A11	E2A10	E2A9	E2A8
3AH	E2 Co-efficient 2	E2B7	E2B6	E2B5	E2B4	E2B3	E2B2	E2B1	E2B0
3BH	E2 Co-efficient 3	E2B15	E2B14	E2B13	E2B12	E2B11	E2B10	E2B9	E2B8
3CH	E2 Co-efficient 4	E2C7	E2C6	E2C5	E2C4	E2C3	E2C2	E2C1	E2C0
3DH	E2 Co-efficient 5	E2C15	E2C14	E2C13	E2C12	E2C11	E2C10	E2C9	E2C8
3EH	E3 Co-efficient 0	E3A7	E3A6	E3A5	E3A4	E3A3	E3A2	E3A1	E3A0
3FH	E3 Co-efficient 1	E3A15	E3A14	E3A13	E3A12	E3A11	E3A10	E3A9	E3A8
40H	E3 Co-efficient 2	E3B7	E3B6	E3B5	E3B4	E3B3	E3B2	E3B1	E3B0
41H	E3 Co-efficient 3	E3B15	E3B14	E3B13	E3B12	E3B11	E3B10	E3B9	E3B8
42H	E3 Co-efficient 4	E3C7	E3C6	E3C5	E3C4	E3C3	E3C2	E3C1	E3C0
43H	E3 Co-efficient 5	E3C15	E3C14	E3C13	E3C12	E3C11	E3C10	E3C9	E3C8
44H	E4 Co-efficient 0	E4A7	E4A6	E4A5	E4A4	E4A3	E4A2	E4A1	E4A0
45H	E4 Co-efficient 1	E4A15	E4A14	E4A13	E4A12	E4A11	E4A10	E4A9	E4A8
46H	E4 Co-efficient 2	E4B7	E4B6	E4B5	E4B4	E4B3	E4B2	E4B1	E4B0
47H	E4 Co-efficient 3	E4B15	E4B14	E4B13	E4B12	E4B11	E4B10	E4B9	E4B8
48H	E4 Co-efficient 4	E4C7	E4C6	E4C5	E4C4	E4C3	E4C2	E4C1	E4C0
49H	E4 Co-efficient 5	E4C15	E4C14	E4C13	E4C12	E4C11	E4C10	E4C9	E4C8
4AH	E5 Co-efficient 0	E5A7	E5A6	E5A5	E5A4	E5A3	E5A2	E5A1	E5A0
4BH	E5 Co-efficient 1	E5A15	E5A14	E5A13	E5A12	E5A11	E5A10	E5A9	E5A8
4CH	E5 Co-efficient 2	E5B7	E5B6	E5B5	E5B4	E5B3	E5B2	E5B1	E5B0
4DH	E5 Co-efficient 3	E5B15	E5B14	E5B13	E5B12	E5B11	E5B10	E5B9	E5B8
4EH	E5 Co-efficient 4	E5C7	E5C6	E5C5	E5C4	E5C3	E5C2	E5C1	E5C0
4FH	E5 Co-efficient 5	E5C15	E5C14	E5C13	E5C12	E5C11	E5C10	E5C9	E5C8

Note 44. PDN pin = “L” resets the registers to their default values.
Note 45. The bits defined as 0 must contain a “0” value.
Note 46. Writing access to 50H ~ 7FH is prohibited.

■ Register Definitions

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Power Management 1	PMPFIL	PMVCM	PMBP	0	0	PMDAC	PMADR	PMADL
R/W		R/W	R/W	R/W	R	R	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

PMADL: Microphone Amplifier Lch and ADC Lch Power Management
0: Power-down (default)
1: Power-up
When the PMADL or PMADR bit is changed from “0” to “1”, the initialization cycle (1059/fs = 22ms @48kHz, ADRST1-0 bits = “00”) starts. After initializing, digital data of the ADC is output.

PMADR: Microphone Amplifier Rch and ADC Rch Power Management
0: Power-down (default)
1: Power-up
When the PMADL or PMADR bit is changed from “0” to “1”, the initialization cycle (1059/fs = 22ms @48kHz, ADRST1-0 bits = “00”) starts. After initializing, digital data of the ADC is output.

PMDAC: DAC Power Management
0: Power down (default)
1: Power up

PMBP: BEEP Input Select and Power Management
0: Power down (RIN3 pin) (default)
1: Power up (BEEP pin)

PMVCM: VCOM and Regulator (2.3V) Power Management
0: Power down (default)
1: Power up

PMPFIL: Programmable Filter Block Power Management
0: Power down (default)
1: Power up

The AK4951A can be powered down by writing “0” to the address “00H” and PMPLL, PMMP, PMHPL, PMHPR, PMSL, PMDML, PMDMR and PMOSC bits. In this case, register values are maintained.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
01H	Power Management 2	PMOSC	0	PMHPR	PMHPL	M/S	PMPLL	PMSL	LOSEL
R/W		R/W	R	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

LOSEL: Stereo Line Output Select
0: Speaker Output (SPP/SPN pins) (default)
1: Stereo Line Output (LOUT/ROUT pins)

PMSL: Speaker Amplifier or Stereo Line Output Power Management
0: Power down (default)
1: Power up

PMPLL: PLL Power Management
0: EXT Mode and Power down (default)
1: PLL Mode and Power up

M/S: Master / Slave Mode Select
0: Slave Mode (default)
1: Master Mode

PMHPL: Lch Headphone Amplifier and Charge Pump Power Management
0: Power down (default)
1: Power up

PMHPR: Rch Headphone Amplifier and Charge Pump Power Management
0: Power down (default)
1: Power up

PMOSC: Internal Oscillator Power Management
0: Power down (default)
1: Power up

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
02H	Signal Select 1	SLPSN	MGAIN3	DACS	MPSEL	PMMP	MGAIN2	MGAIN1	MGAIN0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	1	1	0

MGAIN3-0: Microphone Amplifier Gain Control (Table 23)
Default: “0110” (+18dB)

PMMP: MPWR pin Power Management
0: Power down: Hi-Z (default)
1: Power up

MPSEL: MPWR Output Select
0: MPWR1 pin (default)
1: MPWR2 pin

DACS: Signal Switch Control from DAC to Speaker Amplifier
0: OFF (default)
1: ON

SLPSN: Speaker Amplifier or Stereo Line Output Power-Save Mode
LOSEL bit = “0” (Speaker Output Select)
0: Power Save Mode (default)
1: Normal Operation
When SLPSN bit is “0”, Speaker Amplifier is in power-save mode. In this mode, the SPP pin goes to Hi-Z and the SPN pin outputs SVDD/2 voltage. When PMSL bit = “1”, SLPSN bit is enabled. After the PDN pin is set to “L”, Speaker Amplifier is in power-down mode since PMSL bit is “0”.

LOSEL bit = “1” (Stereo Line Output Select)
0: Power Save Mode (default)
1: Normal Operation
When SLPSN bit is “0”, Stereo line output is in power-save mode. In this mode, the LOUT/ROUT pins output 1.5V or 1.3V. When PMSL bit = “1”, SLPSN bit is enabled. After the PDN pin is set to “L”, Stereo line output is in power-down mode since PMSL bit is “0”.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
03H	Signal Select 2	SPKG1	SPKG0	VODETN	MICL	INL1	INL0	INR1	INR0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

INR1-0: ADC Rch Input Source Select (Table 22)
Default: “00” (RIN1 pin)

INL1-0: ADC Lch Input Source Select (Table 22)
Default: “00” (LIN1 pin)

MICL: MPWR pin Output Voltage Select
0: typ 2.4V (default)
1: typ 2.0V

VODETN: Voice Peak Detection Disable for Automatic Wind Noise Reduction Filter
0: Enable (default)
1: Disable
When AHPF and VODETN bits = “1”, voice peak detection is disable. VODETN bit must be set when PMPFIL bit = “0”.

SPKG1-0: Speaker Amplifier Output Gain Select (Table 56)
Default: “00” (+6.4dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
04H	Signal Select 3	LVCM1	LVCM0	DACL	0	PTS1	PTS0	MONO1	MONO0
R/W		R/W	R/W	R/W	R	R/W	R/W	R/W	R/W
Default		0	1	0	0	0	1	0	0

MONO1-0: Mono/Stereo Setting for DAC Input (Table 49)
Default: “00” (Stereo)

PTS1-0: Soft Transition Control of “BEEP → Headphone” Connection ON/OFF (Table 52)
Default: “01”

DACL: Signal Switch Control from DAC to Stereo Line Amplifier
0: OFF (default)
1: ON

LVCM1-0: Stereo Line Output Gain and Common Voltage Setting (Table 59)
Default: “01” (+2dB, 1.5V)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
05H	Mode Control 1	PLL3	PLL2	PLL1	PLL0	BCKO	CKOFF	DIF1	DIF0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	1	0	1	0	0	1	0

DIF1-0: Audio Interface Format (Table 19)
Default: “10” (MSB justified)

CKOFF: LRCK, BICK and SDTO Output Setting in Master Mode
0: LRCK, BICK and SDTO Output (default)
1: LRCK, BICK and SDTO Stop (“L” output)

BCKO: BICK Output Frequency Setting in Master Mode (Table 10, Table 17)
0: 32fs (default)
1: 64fs

PLL3-0: PLL Reference Clock Select (Table 5)
Default: “0101” (MCKI, 12.288MHz)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
06H	Mode Control 2	CM1	CM0	0	0	FS3	FS2	FS1	FS0
R/W		R/W	R/W	R	R	R/W	R/W	R/W	R/W
Default		0	0	0	0	1	0	1	1

FS3-0: Sampling frequency Setting (Table 6, Table 8, Table 12, Table 15)
Default: “1011” (fs=48kHz)

CM1-0: MCKI Input Frequency Setting in EXT mode (Table 11, Table 14)
Default: “00” (256fs)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
07H	Mode Control 3	TSDSEL	THDET	SMUTE	DVOLC	0	IVOLC	0	0
R/W		R/W	R	R/W	R/W	R	R/W	R	R
Default		0	0	0	1	0	1	0	0

IVOLC: Input Digital Volume Control Mode Select
0: Independent
1: Dependent (default)
When IVOLC bit = “1”, IVL7-0 bits control both Lch and Rch volume levels, while register values of IVL7-0 bits are not written to IVR7-0 bits. When IVOLC bit = “0”, IVL7-0 bits control Lch level and IVR7-0 bits control Rch level, respectively. PMPFIL bit must be “0” when changing the IVOLC bit setting.

DVOLC: Output Digital Volume Control Mode Select
0: Independent
1: Dependent (default)
When DVOLC bit = “1”, DVL7-0 bits control both Lch and Rch volume levels, while register values of DVL7-0 bits are not written to DVR7-0 bits. When DVOLC bit = “0”, DVL7-0 bits control Lch level and DVR7-0 bits control Rch level, respectively.

SMUTE: Soft Mute Control
0: Normal Operation (default)
1: DAC outputs soft-muted

THDET: Thermal Shutdown Detection Result
0: Normal Operation (default)
1: During Thermal Shutdown

TSDSEL: Thermal Shutdown Mode Select
0: Automatic Power up (default)
1: Manual Power up

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
08H	Digital MIC	0	0	PMDMR	PMDML	DCLKE	0	DCLKP	DMIC
R/W		R/W	R	R/W	R/W	R/W	R	R/W	R/W
Default		0	0	0	0	0	0	0	0

DMIC: Digital Microphone Connection Select
0: Analog Microphone (default)
1: Digital Microphone

DCLKP: Data Latching Edge Select
0: Lch data is latched on the DMCLK rising edge ("↑"). (default)
1: Lch data is latched on the DMCLK falling edge ("↓").

DCLKE: DMCLK pin Output Clock Control
0: "L" Output (default)
1: 64fs Output

PMDML/R: Input Signal Select with Digital Microphone (Table 21)
Default: "00"
ADC digital block is powered-down by PMDML = PMDMR bits = "0" when selecting a digital microphone input (DMIC bit = "1").

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
09H	Timer Select	ADRST1	ADRST0	FRATT	FRN	0	0	MOFF	DVTM
R/W		R/W	R/W	R/W	R/W	R	R	R/W	R/W
Default		0	0	0	0	0	0	0	0

DVTM: Output Digital Volume Soft Transition Time Setting (Table 51)
0: 816/fs (default)
1: 204/fs
This is the transition time between DVL/R7-0 bits = 00H and CCH.

MOFF: Soft Transition Control of "BEEP → Headphone" Connection ON/OFF
0: Enable (default)
1: Disable

FRN: ALC Fast Recovery Function Enable
0: Enable (default)
1: Disable

RFATT: Fast Recovery Reference Volume Attenuation Amount (Table 41)
0: -0.00106dB (4/fs) (default)
1: -0.00106dB (16/fs)

ADRST1-0: ADC Initialization Cycle Setting (Table 18)
Default: "00" (1059/fs)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0AH	ALC Timer Select	0	IVTM	EQFC1	EQFC0	WTM1	WTM0	RFST1	RFST0
R/W		R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	1	1	0	0	0	0	0

RFST1-0: ALC First Recovery Speed (Table 40)
Default: “00” (0.0032dB)

WTM1-0: ALC Recovery Waiting Period (Table 37)
Default: “00” (128/fs)

EQFC1-0: ALCEQ Frequency Setting (Table 34)
Default: “10” (Extreme value=150Hz, Zero point=100Hz @ fs = 48kHz)

IVTM: Input Digital Volume Soft Transition Time Setting (Table 46)
0: 236/fs
1: 944/fs (default)
A transition time when changing IVL7-0/IVR7-0 bits to F1H from 05H.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0BH	ALC Mode Control 1	ALCEQN	LMTH2	ALC	RGAIN2	RGAIN1	RGAIN0	LMTH1	LMTH0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

LMTH2-0: ALC Limiter Detection Level / Recovery Counter Reset Level (Table 35)
Default: “000”

RGAIN2-0: ALC Recovery Gain Step (Table 38)
Default: “000” (0.00424dB)

ALC: ALC Enable
0: ALC Disable (default)
1: ALC Enable

ALCEQN: ALC EQ Enable
0: ALC EQ On (default)
1: ALC EQ Off

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0CH	ALC Mode Control 2	REF7	REF6	REF5	REF4	REF3	REF2	REF1	REF0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	1	1	0	0	0	0	1

REF7-0: Reference Value at ALC Recovery Operation. 0.375dB step, 242 Level (Table 39)
Default: “E1H” (+30.0dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0DH	Lch Input Volume Control	IVL7	IVL6	IVL5	IVL4	IVL3	IVL2	IVL1	IVL0
0EH	Rch Input Volume Control	IVR7	IVR6	IVR5	IVR4	IVR3	IVR2	IVR1	IVR0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	1	1	0	0	0	0	1

IVL7-0, IVR7-0: Digital Input Volume; 0.375dB step, 242 Level (Table 45)
Default: “E1H” (+30.0dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0FH	ALC Volume	VOL7	VOL6	VOL5	VOL4	VOL3	VOL2	VOL1	VOL0
R/W		R	R	R	R	R	R	R	R
Default		-	-	-	-	-	-	-	-

VOL7-0: Current ALC volume value; 0.375dB step, 242 Level. Read operation only. (Table 42)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
10H	Lch MIC Gain Setting	MGL7	MGL6	MGL5	MGL4	MGL3	MGL2	MGL1	MGL0
11H	Rch MIC Gain Setting	MGR7	MGR6	MGR5	MGR4	MGR3	MGR2	MGR1	MGR0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	0	0	0	0	0	0	0

MGL7-0, MGR7-0: Lch and Rch Microphone Sensitivity Correction (Table 28)
Default: “80H” (0dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
12H	Beep Control	HPZ	BPVCM	BEEPS	BEEPH	BPLVL3	BPLVL2	BPLVL1	BPLVL0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

BPLVL3-0:BEEP Output Level Setting (Table 54)
Default: “0000” (0dB)

BEEPH: Signal Switch Control from the BEEP pin to Headphone Amplifier
0: OFF (default)
1: ON

BEEPS: Signal Switch Control from the BEEP pin to Speaker Amplifier
0: OFF (default)
1: ON

BPVCM: Common Voltage Setting of BEEP Input Amplifier (Table 53)
0: 1.15V (default)
1: 1.65V

HPZ: Pull-down Setting of Headphone Amplifier
0: Pull-down by a 10Ω(typ) resistor (default)
1: Hi-Z

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
13H	Lch Digital Volume Control	DVL7	DVL6	DVL5	DVL4	DVL3	DVL2	DVL1	DVL0
14H	Rch Digital Volume Control	DVR7	DVR6	DVR5	DVR4	DVR3	DVR2	DVR1	DVR0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	1	1	0	0	0

DVL7-0, DVR7-0: Digital Output Volume (Table 50)
Default: “18H” (0dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
15H	EQ Common Gain Select	0	0	0	EQC5	EQC4	EQC3	EQC2	0
R/W		R	R	R	R/W	R/W	R/W	R/W	R
Default		0	0	0	0	0	0	0	0

EQC2: Equalizer 2 Common Gain Selector
0: Disable (default)
1: Enable
When EQC2 bit = “1”, the common gain setting (EQ2G) is reflected.

EQC3: Equalizer 3 Common Gain Selector
0: Disable (default)
1: Enable
When EQC3 bit = “1”, the common gain setting (EQ3G) is reflected.

EQC4: Equalizer 4 Common Gain Selector
0: Disable (default)
1: Enable
When EQC4 bit = “1”, the common gain setting (EQ4G) is reflected.

EQC5: Equalizer 5 Common Gain Selector
0: Disable (default)
1: Enable
When EQC5 bit = “1”, the common gain setting (EQ5G) is reflected.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
16H	EQ2 Common Gain Setting	EQ2G5	EQ2G4	EQ2G3	EQ2G2	EQ2G1	EQ2G0	EQ2T1	EQ2T0
17H	EQ3 Common Gain Setting	EQ3G5	EQ3G4	EQ3G3	EQ3G2	EQ3G1	EQ3G0	EQ3T1	EQ3T0
18H	EQ4 Common Gain Setting	EQ4G5	EQ4G4	EQ4G3	EQ4G2	EQ4G1	EQ4G0	EQ4T1	EQ4T0
19H	EQ5 Common Gain Setting	EQ5G5	EQ5G4	EQ5G3	EQ5G2	EQ5G1	EQ5G0	EQ5T1	EQ5T0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

EQ2T1-0, EQ3T1-0, EQ4T1-0, EQ5T1-0: Transition Time of EQ2~EQ5 Gain (Table 33)
Default: “00H” (256/fs)

EQ2G5-0, EQ3G5-0, EQ4G5-0, EQ5G5-0: Gain setting of EQ2~EQ5 (Table 32)
Default: “00H” (Mute)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
1AH	Auto HPF Control	0	0	AHPF	SENC2	SENC1	SENC0	STG1	STG0
R/W		R	R	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	1	1	0	0

STG1-0: Automatic Wind Noise Reduction Filter Maximum Attenuation Level (Table 30)
Default: “00” (Low)

SENC2-0: Wind Noise Detection Sensitivity (Table 29)
Default: “011” (2.0)

AHPF: Automatic Wind Noise Reduction Filter Control
0: OFF (default)
1: ON
When AHPF bit = “1”, the automatic wind noise reduction filter is enabled. The audio data passes this block by 0dB gain when AHPF bit = “0”.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
1BH	Digital Filter Select 1	0	0	0	0	0	HPFC1	HPFC0	HPFAD
R/W		R	R	R	R	R	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	1

HPFAD: HPF1 Control after ADC
0: OFF
1: ON (default)
When HPFAD bit is “1”, the settings of HPFC1-0 bits are enabled. When HPFAD bit is “0”, the audio data passes the HPFAD block by 0dB gain.
When PMADL bit = “1” or PMADR bit = “1”, set HPFAD bit to “1”.

HPFC1-0: Cut-off Frequency Setting of HPF1 (ADC) (Table 27)
Default: “00” (3.7Hz @ fs = 48kHz)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
1CH	Digital Filter Select 2	GN1	GN0	EQ0	FIL3	0	0	LPF	HPF
R/W		R/W	R/W	R/W	R/W	R	R	R/W	R/W
Default		0	0	0	0	0	0	0	0

HPF: HPF2 Coefficient Setting Enable
0: OFF (default)
1: ON
When HPF bit is “1”, the settings of F1A13-0 and F1B13-0 bits are enabled. When HPF bit is “0”, the audio data passes the HPF2 block by is 0dB gain.

LPF: LPF Coefficient Setting Enable
0: OFF (default)
1: ON
When LPF bit is “1”, the settings of F2A13-0 and F2B13-0 bits are enabled. When LPF bit is “0”, the audio data passes the LPF block by 0dB gain.

FIL3: FIL3 (Stereo Emphasis Filter) Coefficient Setting Enable
0: Disable (default)
1: Enable
When FIL3 bit = “1”, the settings of F3A13-0 and F3B13-0 bits are enabled. When FIL3 bit = “0”, FIL3 block is OFF (MUTE).

EQ0: EQ0 (Gain Compensation Filter) Coefficient Setting Enable
0: OFF (default)
1: ON
When EQ0 bit = “1”, the settings of E0A15-0, E0B13-0 and E0C15-0 bits are enabled. When EQ0 bit = “0”, the audio data passes the EQ0 block by 0dB gain.

GN1-0: Gain Setting of the Gain Block (Table 31)
Default: “00” (0dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
1DH	Digital Filter Mode	0	0	PFVOL1	PFVOL0	PFDAC1	PFDAC0	ADCPF	PFSDO
R/W		R	R	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	1	1

PFSDO: SDTO Output Signal Select
0: ADC (+ 1st order HPF) Output
1: Programmable Filter / ALC Output (default)

ADCPF: Programmable Filter / ALC Input Signal Select
0: SDTI
1: ADC Output (default)

PFDAC1-0: DAC Input Signal Select (Table 48)
Default: 00 (SDTI)

PFVOL1-0: Sidetone Digital Volume (Table 47)
Default: 00 (0dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
1EH	HPF2 Co-efficient 0	F1A7	F1A6	F1A5	F1A4	F1A3	F1A2	F1A1	F1A0
1FH	HPF2 Co-efficient 1	0	0	F1A13	F1A12	F1A11	F1A10	F1A9	F1A8
20H	HPF2 Co-efficient 2	F1B7	F1B6	F1B5	F1B4	F1B3	F1B2	F1B1	F1B0
21H	HPF2 Co-efficient 3	0	0	F1B13	F1B12	F1B11	F1B10	F1B9	F1B8
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		F1A13-0 bits = 0x1FB0, F1B13-0 bits = 0x209F							

F1A13-0, F1B13-0: HPF2 Coefficient (14bit x 2)
Default: F1A13-0 bits = 0x1FB0, F1B13-0 bits = 0x209F (fc = 150Hz@fs=48kHz)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
22H	LPF Co-efficient 0	F2A7	F2A6	F2A5	F2A4	F2A3	F2A2	F2A1	F2A0
23H	LPF Co-efficient 1	0	0	F2A13	F2A12	F2A11	F2A10	F2A9	F2A8
24H	LPF Co-efficient 2	F2B7	F2B6	F2B5	F2B4	F2B3	F2B2	F2B1	F2B0
25H	LPF Co-efficient 3	0	0	F2B13	F2B12	F2B11	F2B10	F2B9	F2B8
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

F2A13-0, F2B13-0: LPF Coefficient (14bit x 2)
Default: “0000H”

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
26H	FIL3 Co-efficient 0	F3A7	F3A6	F3A5	F3A4	F3A3	F3A2	F3A1	F3A0
27H	FIL3 Co-efficient 1	F3AS	0	F3A13	F3A12	F3A11	F3A10	F3A9	F3A8
28H	FIL3 Co-efficient 2	F3B7	F3B6	F3B5	F3B4	F3B3	F3B2	F3B1	F3B0
29H	FIL3 Co-efficient 3	0	0	F3B13	F3B12	F3B11	F3B10	F3B9	F3B8
2AH	EQ Co-efficient 0	E0A7	E0A6	E0A5	E0A4	E0A3	E0A2	E0A1	E0A0
2BH	EQ Co-efficient 1	E0A15	E0A14	E0A13	E0A12	E0A11	E0A10	E0A9	E0A8
2CH	EQ Co-efficient 2	E0B7	E0B6	E0B5	E0B4	E0B3	E0B2	E0B1	E0B0
2DH	EQ Co-efficient 3	0	0	E0B13	E0B12	E0B11	E0B10	E0B9	E0B8
2EH	EQ Co-efficient 4	E0C7	E0C6	E0C5	E0C4	E0C3	E0C2	E0C1	E0C0
2FH	EQ Co-efficient 5	E0C15	E0C14	E0C13	E0C12	E0C11	E0C10	E0C9	E0C8
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

F3A13-0, F3B13-0: FIL3 (Stereo Emphasis Filter) Coefficient (14bit x 2)
Default: “0000H”

F3AS: FIL3 (Stereo Emphasis Filter) Select
0: HPF (default)
1: LPF

E0A15-0, E0B13-0, E0C15-C0: EQ0 (Gain Compensation Filter) Coefficient (14bit x 1 + 16bit x 2)
Default: “0000H”

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
30H	Digital Filter Select 3	0	0	0	EQ5	EQ4	EQ3	EQ2	EQ1
R/W		R	R	R	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

EQ1: Equalizer 1 Coefficient Setting Enable
0: Disable (default)
1: Enable
When EQ1 bit is “1”, the settings of E1A15-0, E1B15-0 and E1C15-0 bits are enabled. When EQ1 bit is “0”, the audio data passes the EQ1 block by 0dB gain.

EQ2: Equalizer 2 Coefficient Setting Enable
0: Disable (default)
1: Enable
When EQ2 bit is “1”, the settings of E2A15-0, E2B15-0 and E2C15-0 bits are enabled. When EQ2 bit is “0”, the audio data passes the EQ2 block by 0dB gain.

EQ3: Equalizer 3 Coefficient Setting Enable
0: Disable (default)
1: Enable
When EQ3 bit is “1”, the settings of E3A15-0, E3B15-0 and E3C15-0 bits are enabled. When EQ3 bit is “0”, the audio data passes the EQ3 block by 0dB gain.

EQ4: Equalizer 4 Coefficient Setting Enable
0: Disable (default)
1: Enable
When EQ4 bit is “1”, the settings of E4A15-0, E4B15-0 and E4C15-0 bits are enabled. When EQ4 bit is “0”, the audio data passes the EQ4 block by 0dB gain.

EQ5: Equalizer 5 Coefficient Setting Enable
0: Disable (default)
1: Enable
When EQ5 bit is “1”, the settings of E5A15-0, E5B15-0 and E5C15-0 bits are enabled. When EQ5 bit is “0”, the audio data passes the EQ5 block by 0dB gain.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
31H	Device Information	REV3	REV2	REV1	REV0	DVN3	DVN2	DVN1	DVN0
R/W		R	R	R	R	R	R	R	R
Default		1	1	0	1	0	0	0	1

DVN3-0: Device No. ID (Read operation only.)
0001: AK4951

REV3-0: Device Revision ID (Read operation only.)
1101: AK4951A

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
32H	E1 Co-efficient 0	E1A7	E1A6	E1A5	E1A4	E1A3	E1A2	E1A1	E1A0
33H	E1 Co-efficient 1	E1A15	E1A14	E1A13	E1A12	E1A11	E1A10	E1A9	E1A8
34H	E1 Co-efficient 2	E1B7	E1B6	E1B5	E1B4	E1B3	E1B2	E1B1	E1B0
35H	E1 Co-efficient 3	E1B15	E1B14	E1B13	E1B12	E1B11	E1B10	E1B9	E1B8
36H	E1 Co-efficient 4	E1C7	E1C6	E1C5	E1C4	E1C3	E1C2	E1C1	E1C0
37H	E1 Co-efficient 5	E1C15	E1C14	E1C13	E1C12	E1C11	E1C10	E1C9	E1C8
38H	E2 Co-efficient 0	E2A7	E2A6	E2A5	E2A4	E2A3	E2A2	E2A1	E2A0
39H	E2 Co-efficient 1	E2A15	E2A14	E2A13	E2A12	E2A11	E2A10	E2A9	E2A8
3AH	E2 Co-efficient 2	E2B7	E2B6	E2B5	E2B4	E2B3	E2B2	E2B1	E2B0
3BH	E2 Co-efficient 3	E2B15	E2B14	E2B13	E2B12	E2B11	E2B10	E2B9	E2B8
3CH	E2 Co-efficient 4	E2C7	E2C6	E2C5	E2C4	E2C3	E2C2	E2C1	E2C0
3DH	E2 Co-efficient 5	E2C15	E2C14	E2C13	E2C12	E2C11	E2C10	E2C9	E2C8
3EH	E3 Co-efficient 0	E3A7	E3A6	E3A5	E3A4	E3A3	E3A2	E3A1	E3A0
3FH	E3 Co-efficient 1	E3A15	E3A14	E3A13	E3A12	E3A11	E3A10	E3A9	E3A8
40H	E3 Co-efficient 2	E3B7	E3B6	E3B5	E3B4	E3B3	E3B2	E3B1	E3B0
41H	E3 Co-efficient 3	E3B15	E3B14	E3B13	E3B12	E3B11	E3B10	E3B9	E3B8
42H	E3 Co-efficient 4	E3C7	E3C6	E3C5	E3C4	E3C3	E3C2	E3C1	E3C0
43H	E3 Co-efficient 5	E3C15	E3C14	E3C13	E3C12	E3C11	E3C10	E3C9	E3C8
44H	E4 Co-efficient 0	E4A7	E4A6	E4A5	E4A4	E4A3	E4A2	E4A1	E4A0
45H	E4 Co-efficient 1	E4A15	E4A14	E4A13	E4A12	E4A11	E4A10	E4A9	E4A8
46H	E4 Co-efficient 2	E4B7	E4B6	E4B5	E4B4	E4B3	E4B2	E4B1	E4B0
47H	E4 Co-efficient 3	E4B15	E4B14	E4B13	E4B12	E4B11	E4B10	E4B9	E4B8
48H	E4 Co-efficient 4	E4C7	E4C6	E4C5	E4C4	E4C3	E4C2	E4C1	E4C0
49H	E4 Co-efficient 5	E4C15	E4C14	E4C13	E4C12	E4C11	E4C10	E4C9	E4C8
4AH	E5 Co-efficient 0	E5A7	E5A6	E5A5	E5A4	E5A3	E5A2	E5A1	E5A0
4BH	E5 Co-efficient 1	E5A15	E5A14	E5A13	E5A12	E5A11	E5A10	E5A9	E5A8
4CH	E5 Co-efficient 2	E5B7	E5B6	E5B5	E5B4	E5B3	E5B2	E5B1	E5B0
4DH	E5 Co-efficient 3	E5B15	E5B14	E5B13	E5B12	E5B11	E5B10	E5B9	E5B8
4EH	E5 Co-efficient 4	E5C7	E5C6	E5C5	E5C4	E5C3	E5C2	E5C1	E5C0
4FH	E5 Co-efficient 5	E5C15	E5C14	E5C13	E5C12	E5C11	E5C10	E5C9	E5C8
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

E1A15-0, E1B15-0, E1C15-0: Equalizer 1 Coefficient (16bit x3)
Default: “0000H”

E2A15-0, E2B15-0, E2C15-0: Equalizer 2 Coefficient (16bit x3)
Default: “0000H”

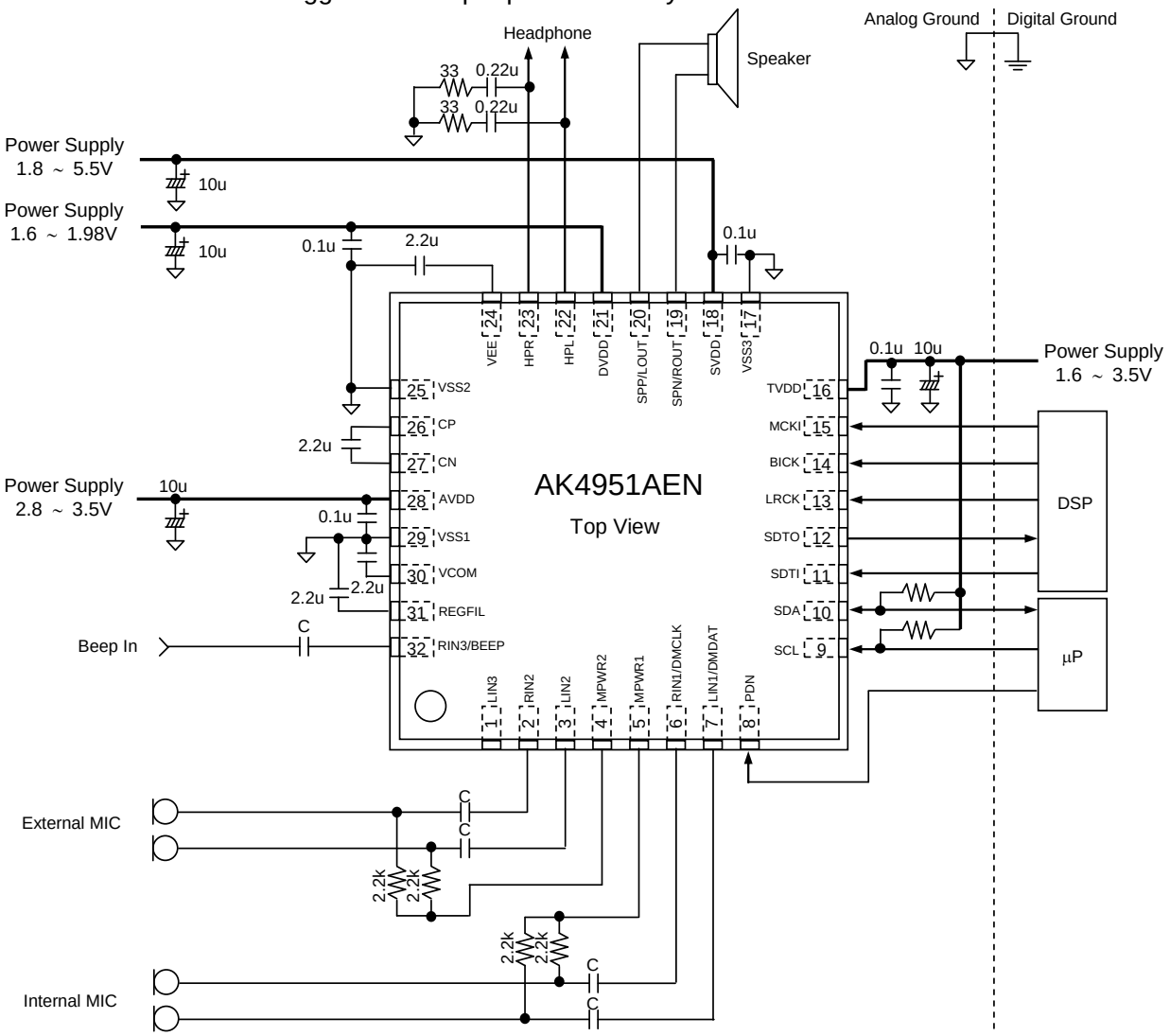
E3A15-0, E3B15-0, E3C15-0: Equalizer 3 Coefficient (16bit x3)
Default: “0000H”

E4A15-0, E4B15-0, E4C15-0: Equalizer 4 Coefficient (16bit x3)
Default: “0000H”

E5A15-0, E5B15-0, E5C15-0: Equalizer 5 Coefficient (16bit x3)
Default: “0000H”

10. Recommended External Circuits

Figure 58 shows the system connection diagram. An evaluation board (AKD4951AEN) is available for fast evaluation as well as suggestions for peripheral circuitry.



Notes:

- VSS1, VSS2 and VSS3 of the AK4951A must be distributed separately from the ground of external controllers.
- All digital input pins must not be allowed to float.
- When the AK4951A is used in master mode, LRCK and BICK pins are floating before M/S bit is changed to "1". Therefore, a pull-up or pull-down resistor around 100kΩ must be connected to LRCK and BICK pins of the AK4951A.
- The pull-up resistors of the SCL and SDA pins must be connected to a voltage in the range from TVDD or more to 6V or less.
- 0.1µF capacitors at power supply pins and 2.2µF capacitors between CP and CN pins, and between VEE and VSS2 pins should be ceramic capacitors. Other capacitors do not have specific types.

Figure 58. System Connection Diagram

1. Grounding and Power Supply Decoupling

The AK4951A requires careful attention to power supply and grounding arrangements. AVDD and SVDD are usually supplied from the system's analog supply, and DVDD and TVDD are supplied from the system's digital power supply. If AVDD, DVDD, TVDD and SVDD are supplied separately, the power-up sequence is not critical. The PDN pin should be held "L" when power supplies are tuning on. The PDN pin is allowed to be "H" after all power supplies are applied and settled.

To avoid pop noise on headphone output and line output when power up/down, the AK4951A should be operated along the following recommended power-up/down sequence.

1) Power-up
   - The PDN pin should be held "L" when power supplies are turning on. The AK4951A can be reset by keeping the PDN pin "L" for 200ns or longer after all power supplies are applied and settled.
2) Power-down
   - Each of power supplies can be powered OFF after the PDN pin is set to "L".

VSS1, VSS2 and VSS3 of the AK4951A should be connected to the analog ground plane. System analog ground and digital ground should be wired separately and connected together as close as possible to where the supplies are brought onto the printed circuit board. Decoupling capacitors should be as close the power supply pins as possible. Especially, the small value ceramic capacitor is to be closest.

2. Internal Regulated Voltage Power Supply

REGFIL is a power supply of the analog circuit (typ. 2.3V). A 2.2μF ±20% capacitor attached to the VSS1 pin eliminates the effects of high frequency noise. This capacitor should be placed as near as possible to the AK4951A. No load current may be drawn from the REGFIL pin. All digital signals, especially clocks, should be kept away from the REGFIL pin in order to avoid unwanted coupling into the AK4951A.

3. Reference Voltage

VCOM is a signal ground of this chip. A 2.2μF ±20% capacitor attached to the VSS1 pin eliminates the effects of high frequency noise. This capacitor should be placed as near as possible to the AK4951A. No load current may be drawn from the VCOM pin. All signals, especially clocks, should be kept away from the VCOM pin in order to avoid unwanted coupling into the AK4951A. Attention must be paid to the printing pattern and the material of the capacitors to prevent superimposed noises and voltage drops since the VCOM voltage is the reference of many functions.

4. Charge Pump

2.2μF±20% capacitors between the CP and CN pins, and the VEE and VSS2 pins should be low ESR ceramic capacitors. These capacitors must be connected as close as possible to the pins. No load current may be drawn from the VEE pin.

5. Analog Inputs

The microphone and line inputs support single-ended format. The input signal range scales with nominally at typ. 2.07Vpp (@ MGAIN = 0dB), centered around the internal signal ground (typ. 1.15V). Usually the input signal is AC coupled with a capacitor. The cut-off frequency is $fc = 1/(2\pi RC)$.

6. Analog Outputs

The input data format for the DAC is 2's complement. The output voltage is a positive full scale for 7FFFFFH (@24bit) and a negative full scale for 800000H (@24bit). The ideal output is VCOM voltage for 000000H (@24bit data). The headphone output is single-ended and centered around VSS (0V). There is no need for AC coupling capacitors. The speaker amplifier (SPP and SPN pins) is BTL output, and they should be connected directly to a speaker. There is no need for AC coupling capacitors. The stereo line outputs (LOUT and ROUT pins) are single-ended and centered on 1.5V (LVCM0 bit = "1": default). These pins must be AC-coupled using a capacitor.

11. Control Sequence

■ Clock Set Up

When ADC, DAC or Programmable Filter is powered-up, the clocks must be supplied. Turn off the power management bits first when switching the clock. The power management bits should be turned on after the clock is stabilized.

1. PLL Master Mode

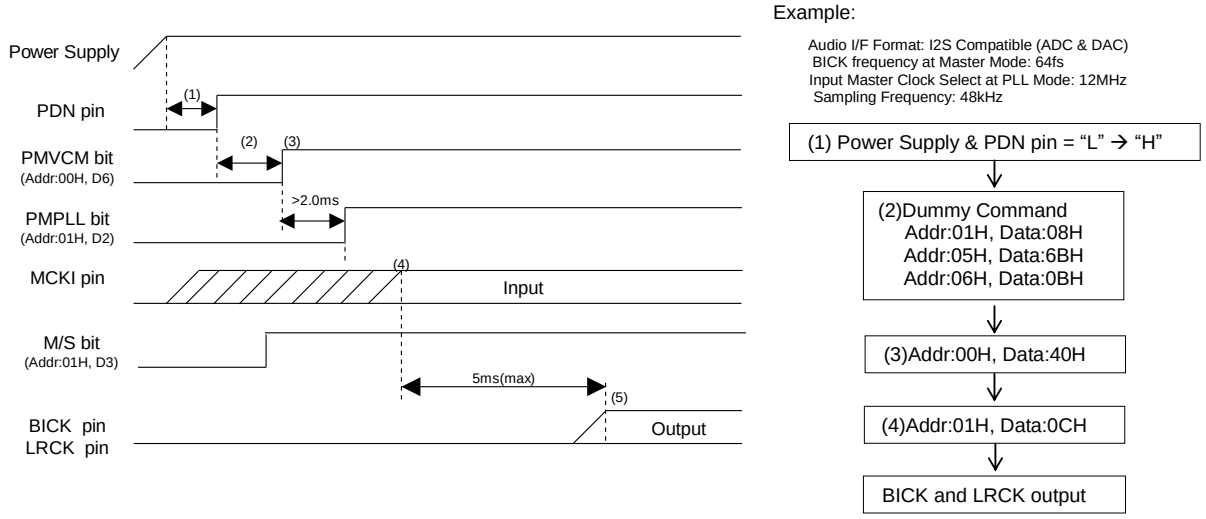


Figure 59. Clock Set Up Sequence (1)

<Sequence>

(1) After Power Up: PDN pin "L" → "H"
"L" time of 200ns or more is needed to reset the AK4951A.

(2) After Dummy Command (Addr:00H, Data:00H) input, DIF1-0, PLL3-0, FS3-0, BCKO and M/S bits must be set during this period.

(3) Power Up VCOM and Regulator: PMVCM bit = "0" → "1"
VCOM and Regulator must first be powered-up before the other block operates. Power up time is 2.0ms (max) when the capacitance of an external capacitor for the VCOM and the REGFIL pin is 2.2μF each.

(4) PLL starts after PMPLL bit changes from "0" to "1" and MCKI is supplied from an external source, and PLL lock time is 5ms (max)

(5) The AK4951A starts to output the LRCK and BICK clocks after the PLL became stable. Then normal operation starts.

2. PLL Slave Mode (BICK pin)

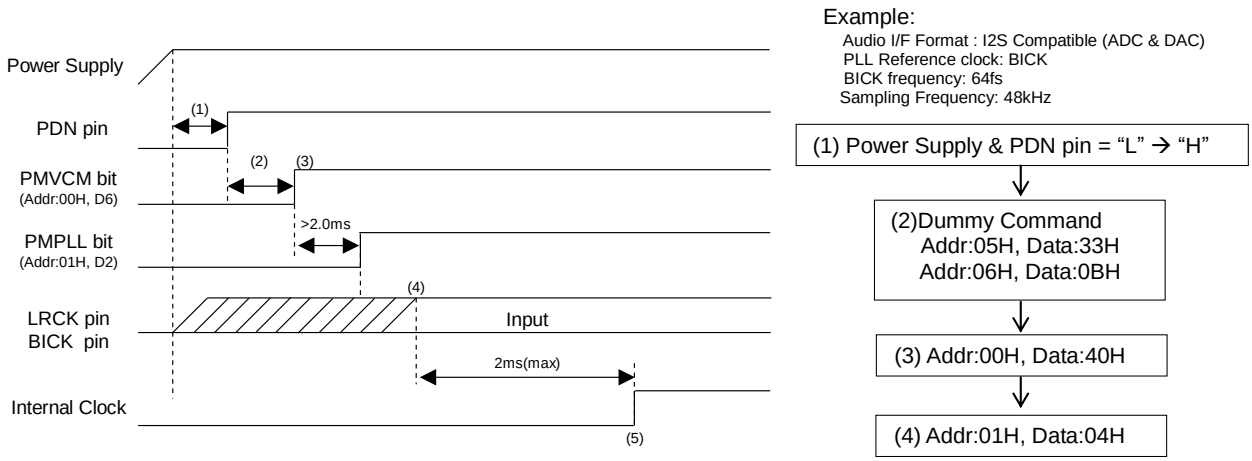


Figure 60. Clock Set Up Sequence (2)

<Sequence>

(1) After Power Up: PDN pin "L" → "H"
"L" time of 200ns or more is needed to reset the AK4951A.

(2) After Dummy Command (Addr:00H, Data:00H) input, DIF1-0, PLL3-0, and FS3-0 bits must be set during this period.

(3) Power Up VCOM and Regulator: PMVCM bit = "0" → "1"
VCOM and Regulator must first be powered-up before the other block operates. Power up time is 2.0ms (max) when the capacitance of an external capacitor for the VCOM and the REGFIL pin is 2.2μF each.

(4) PLL starts after the PMPLL bit changes from "0" to "1" and PLL reference clock (BICK pin) is supplied. PLL lock time is 2ms (max) when BICK is a PLL reference clock.

(5) Normal operation starts after that the PLL is locked.

3. EXT Slave Mode

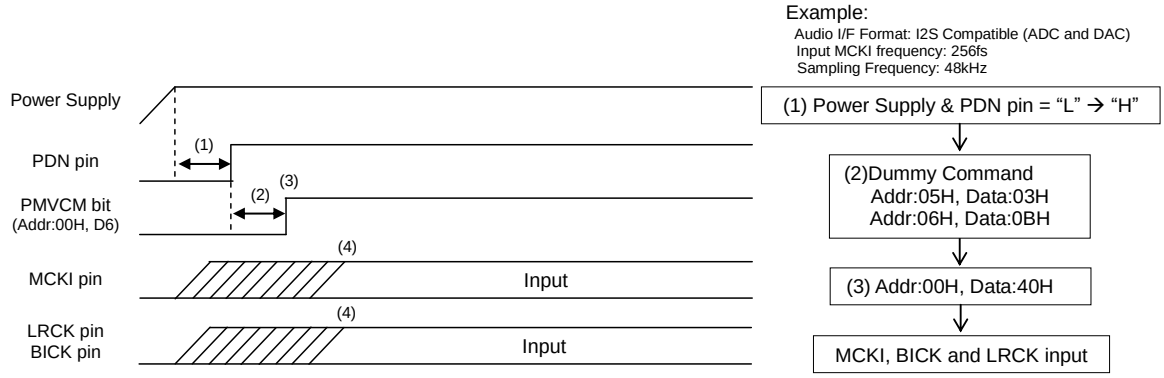


Figure 61. Clock Set Up Sequence (3)

<Sequence>

(1) After Power Up: PDN pin "L" → "H"
"L" time of 200ns or more is needed to reset the AK4951A.

(2) After Dummy Command (Addr:00H, Data:00H) input, DIF1-0, CM1-0 and FS3-0 bits must be set during this period.

(3) Power Up VCOM and Regulator: PMVCM bit = "0" → "1"
VCOM and Regulator must first be powered-up before the other block operates. Power up time is 2.0ms (max) when the capacitance of an external capacitor for the VCOM and the REGFIL pin is 2.2μF each.

(4) Normal operation starts after the MCKI, LRCK and BICK are supplied.

4. EXT Master Mode

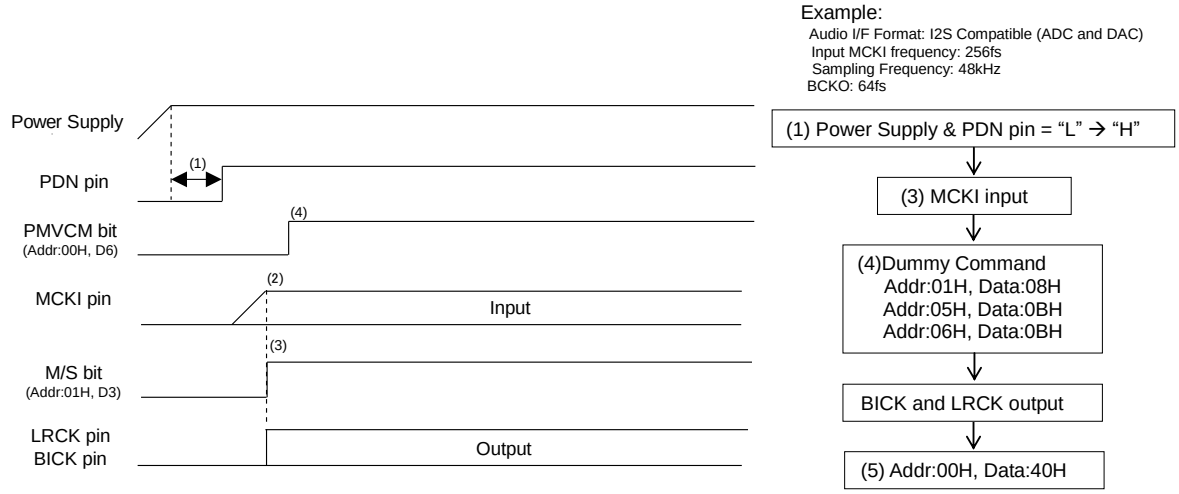


Figure 62. Clock Set Up Sequence (4)

<Sequence>

(1) After Power Up: PDN pin "L" → "H"
"L" time of 200ns or more is needed to reset the AK4951A.

(2) MCKI is supplied.

(3) After Dummy Command (Addr:00H, Data:00H) input, DIF1-0, CM1-0, BCKO and FS3-0 bits are set. M/S bit should be set to "1". Then LRCK and BICK are output.

(4) Power Up VCOM and Regulator: PMVCM bit = "0" → "1"
VCOM and Regulator must first be powered-up before the other block operates. Power up time is 2.0ms (max) when both capacitances of an external capacitor for the VCOM and REGFIL pins are 2.2μF each.

■ Microphone Input Recording (Stereo)

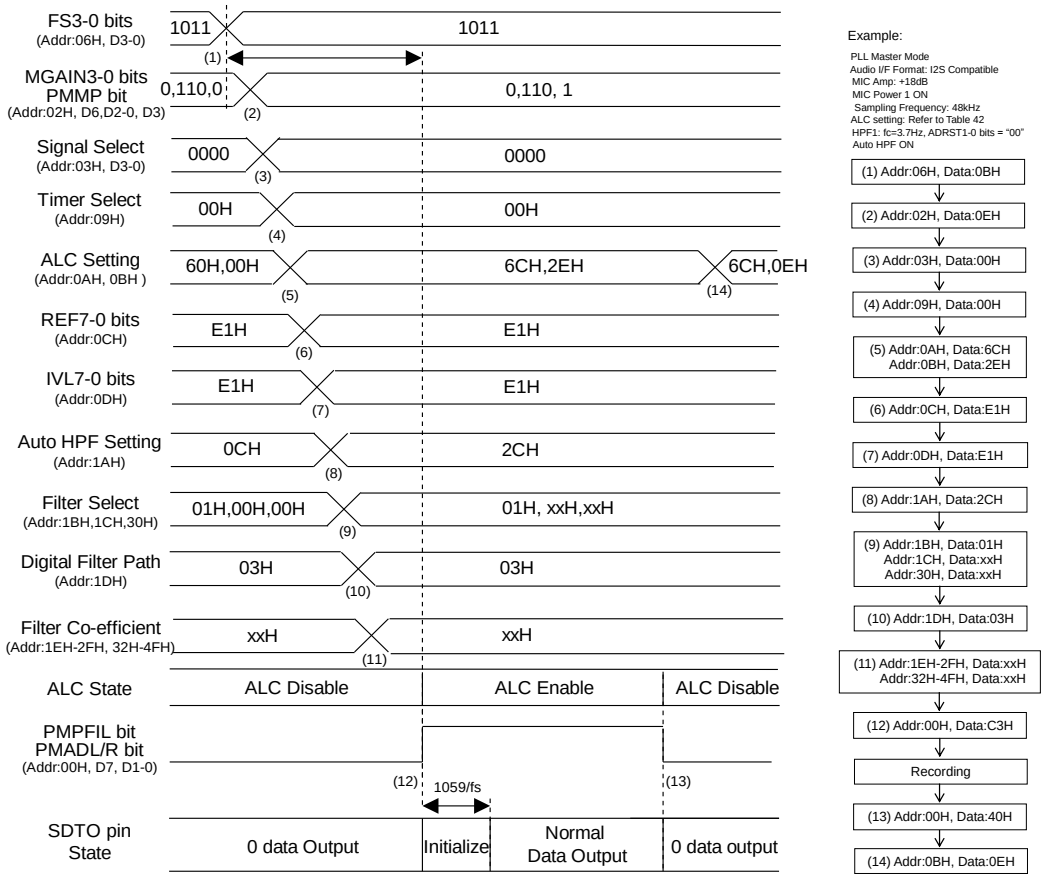


Figure 63. Microphone Input Recording Sequence

<Sequence>

This sequence is an example of ALC setting at fs= 48kHz. For changing the parameter of ALC, please refer to Table 43. At first, clocks should be supplied according to "Clock Set Up" sequence.

(1) Set up a sampling frequency (FS3-0 bits). When the AK4951A is in PLL mode, Microphone, ADC and Programmable Filter of (12) must be powered-up in consideration of PLL lock time after a sampling frequency is changed.
(2) Set up Microphone Amp and Microphone Power. (Addr = 02H)
(3) Set up Input Signal. (Addr = 03H)
(4) Set up FRN, FRATT and ADRST1-0 bits (Addr = 09H)
(5) Set up ALC mode. (Addr = 0AH, 0BH)
(6) Set up REF value at ALC (Addr = 0CH)
(7) Set up IVOL value at ALC operation start (Addr = 0DH)
(8) Set up Auto HPF (Addr = 1AH)
(9) Programmable Filter ON/OFF Setting (Addr: 1BH, 1CH, 30H)
(10) Set up Programmable Filter Path: PFSDO bit = ADCPF bit = "1" (Addr = 1DH)
(11) Set up Coefficient Programmable Filter (Addr: 1EH ~ 2FH, 32H ~ 4FH)
(12) Power Up Microphone Amp, ADC and Programmable Filter: PMADL = PMADR =PMPFIL bits = "0" → "1"
The initialization cycle time of ADC is 1059/fs=22ms @ fs=48kHz, ADRST1-0 bit = "00". ADC outputs "0" data during the initialization cycle. After the ALC bit is set to "1", the ALC operation starts from IVOL value of (7).
(13) Power Down Microphone Amp, ADC and Programmable Filter: PMADL = PMADR = PMPFIL bits = "1" → "0"
(14) ALC Disable: ALC bit = "1" → "0"

■ Digital Microphone Input (Stereo)

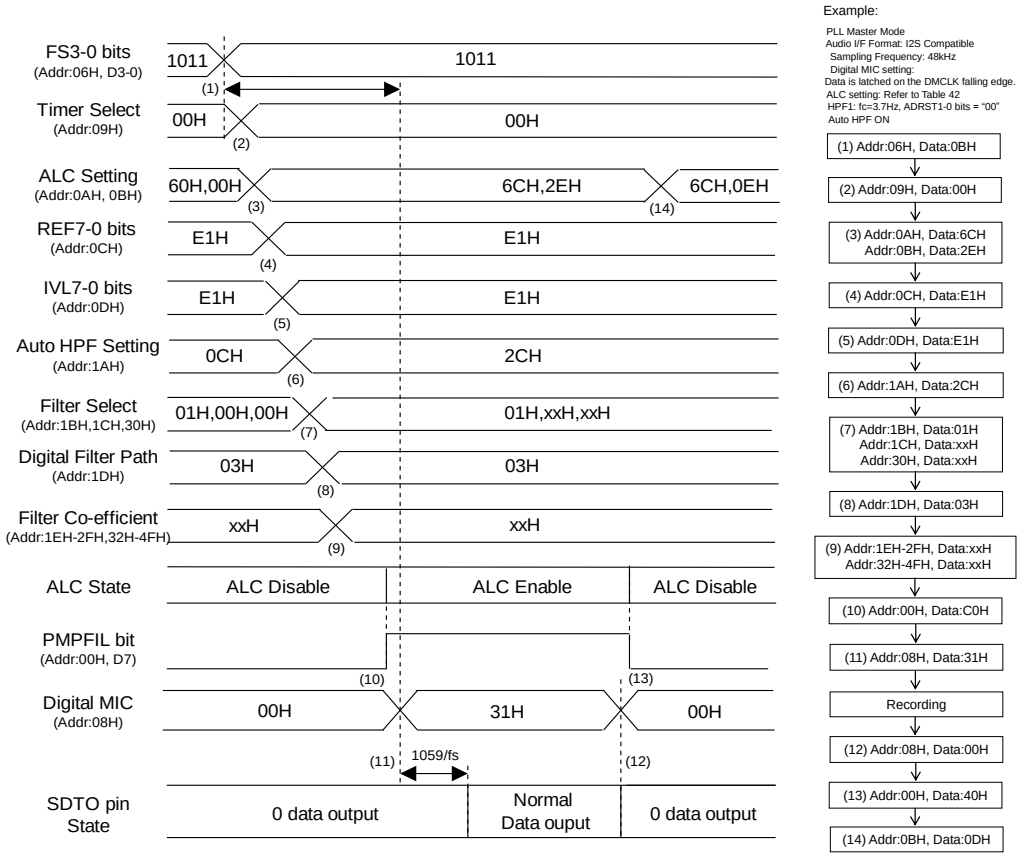


Figure 64. Digital Microphone Input Recording Sequence

<Sequence>

This sequence is an example of ALC setting at fs=48kHz. For changing the parameter of ALC, please refer to Table 43. At first, clocks should be supplied according to "Clock Set Up" sequence.

(1) Set up a sampling frequency (FS3-0 bits). When the AK4951A is PLL mode, Digital Microphone of (11) and Programmable Filter of (10) must be powered-up in consideration of PLL lock time after a sampling frequency is changed.
(2) Set up FRN, FRATT and ADRST1-0 bits (Addr = 09H)
(3) Set up ALC mode. (Addr = 0AH, 0BH)
(4) Set up REF value for ALC (Addr = 0CH)
(5) Set up IVOL value at ALC operation start (Addr = 0DH)
(6) Set up Auto HPF. (Addr =1AH)
(7) Set up Programmable Filter ON/OFF (Addr = 1BH, 1CH, 30H)
(8) Set up Programmable Filter Path: PFSDO bit = ADCPF bit = "1" (Addr = 1DH)
(9) Set up Coefficient of Programmable Filter (Addr:1EH ~ 2FH, 32H ~ 4FH)
(10) Power Up Programmable Filter: PMPFIL bit = "0" → "1"
(11) Set Up & Power Up Digital Microphone: DMIC = PMDMR = PMDML bits = "0" → "1"
The initialization cycle time of ADC is 1059/fs=22ms@ fs=48kHz, ADRST1-0 bit = "00". ADC outputs "0" data during initialization cycle. After the ALC bit is set to "1", the ALC operation starts from IVOL value of (5).
(12) Power Down Digital Microphone: PMDMR =PMDML bits = "1" → "0"
(13) Power Down Programmable Filter: PMPFIL bit = "1" → "0"
(14) ALC Disable: ALC bit = "1" → "0"

■ Headphone Amplifier Output

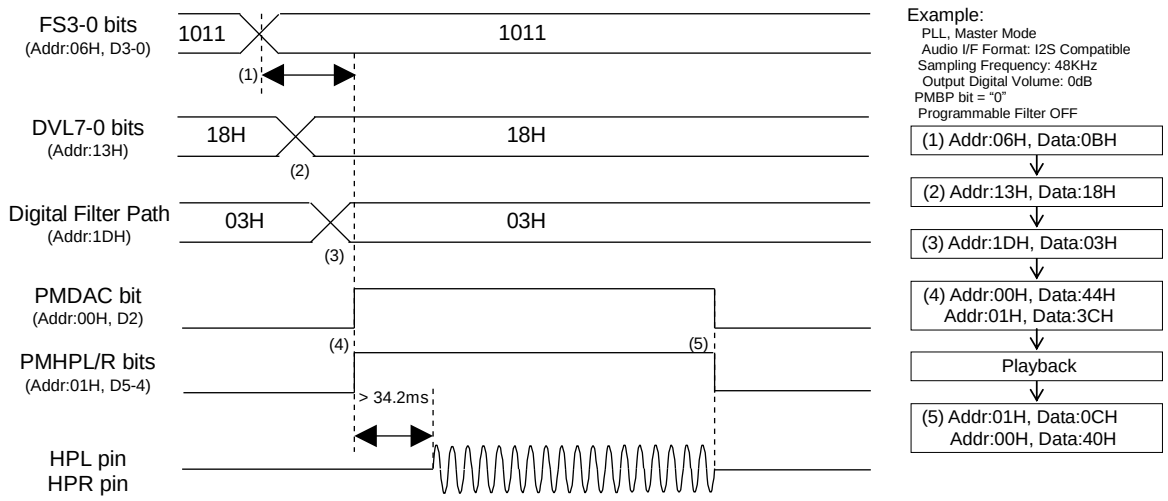


Figure 65. Headphone-Amp Output Sequence

<Sequence>

At first, clocks should be supplied according to "Clock Set Up" sequence.

(1) Set up the sampling frequency (FS3-0 bits). When the AK4951A is PLL mode, the Headphone Amplifier and DAC of (4) must be powered-up in consideration of PLL lock time after the sampling frequency is changed.
(2) Set up the digital output volume (Addr = 13H)
(3) Set up Programmable Filter Path: PFDAC1-0, ADCPF and PFSDO bits (Addr = 1DH)
(4) Power up DAC and Headphone Amplifier: PMDAC = PMHPL = PMHPR bits = "0" → "1"
When PMHPL = PMHPR bits = "1", the charge pump circuit is powered-up. The power-up time of Headphone Amplifier block is 34.2ms (max).
(5) Power down DAC and Headphone Amplifier: PMDAC = PMHPL = PMHPR bits = "1" → "0"

■ Beep Signal Output from Headphone Amplifier

1. Power down DAC → Headphone Amplifier

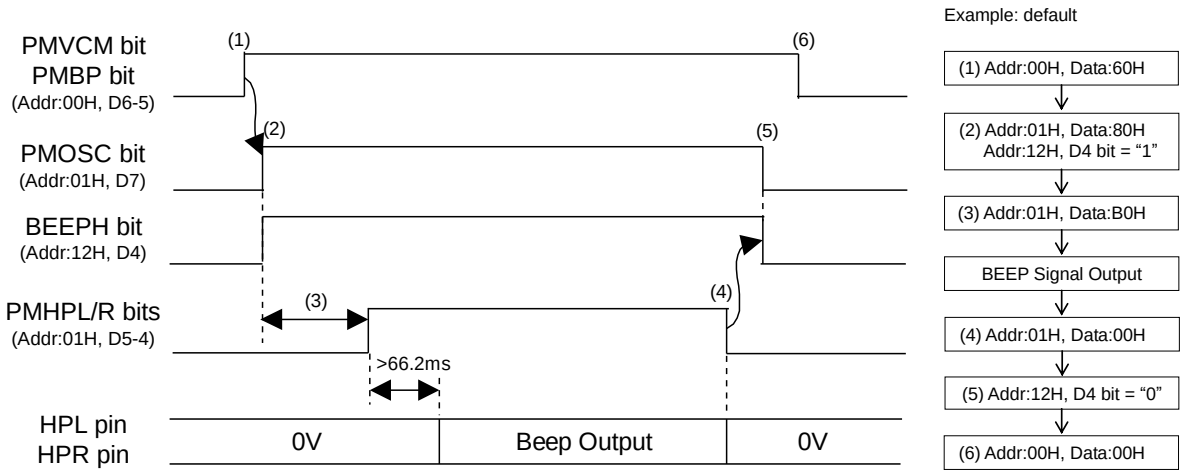


Figure 66. "BEEP-Amp → Headphone-Amp" Output Sequence

<Sequence>
Clock input is not necessary when the AK4951A is operating only on the path of "BEEP-Amp → Headphone-Amp".

(1) Power up VCOM and BEEP Amplifier: PMVCM = PMBP bit = "0" → "1"
Beep Amplifier is powered-up after rise-up VCOM. Power up time for VCOM is 2ms (max).
(2) Power up Oscillator: "0" → "1"
Set up the path of BEEP-Amp → Headphone-Amp: BEEPH bit= "0" → "1"
(3) Power up Headphone Amplifier: PMHPL bit or PMHPR bit = "0" → "1"
Period (3) should be set according to the time constant of a capacitor and a resistor that are connected to the BEEP pin. Pop noise may occur if the Headphone-Amp output is enabled before the BEEP-Amp input is stabilized. The BEEP-Amp is powered up after VCOM voltage rise. The maximum rise-up time of VCOM is 2msec.
e.g. R=86kΩ(max), C=0.1μF: Recommended Wait Time (max.): 2msec + 10τ = 88ms or more
The power-up time of Headphone Amplifier block is 66.2ms (max).
(4) Power down Headphone Amplifier: PMHPL = PMHPR bits = "1" → "0"
(5) Power down Oscillator: PMOSC bit = "1" → "0"
Disable the path of BEEP → Headphone-Amp: BEEPH bit = "1" → "0"
(6) Power down VCOM and BEEP Amplifier: PMVCM = PMBP bits = "1" → "0"

2. Power up DAC → Headphone Amplifier

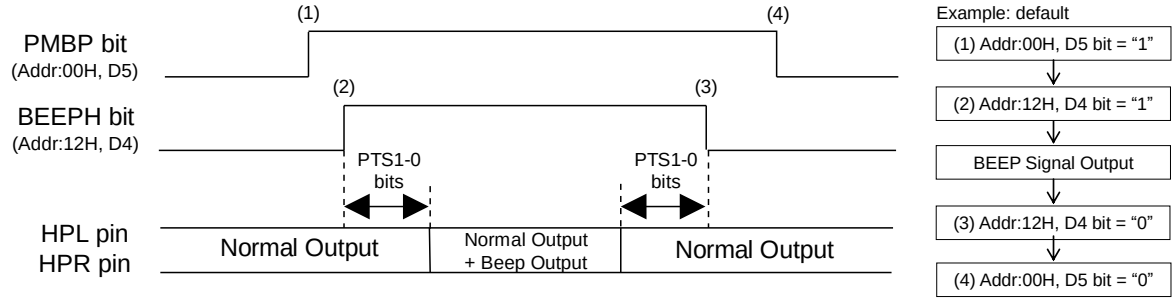


Figure 67. "BEEP-Amp → Headphone-Amp" Output Sequence

<Example>

At first, clocks should be supplied according to "Clock Set Up" sequence, and Headphone Amplifier output should be started according to "Headphone Amplifier Output" sequence.

(1) Power up BEEP Amplifier: PMBP bit = "0" → "1"
(2) BEEP output: BEEPH bit= "0" → "1"
After the transition time set by PTS1-0 bits, BEEP output starts.
(3) BEEP stop: BEEPH bit= "1" → "0"
(4) Power down BEEP Amplifier: PMBP bit = "1" → "0"

■ Speaker Amplifier Output

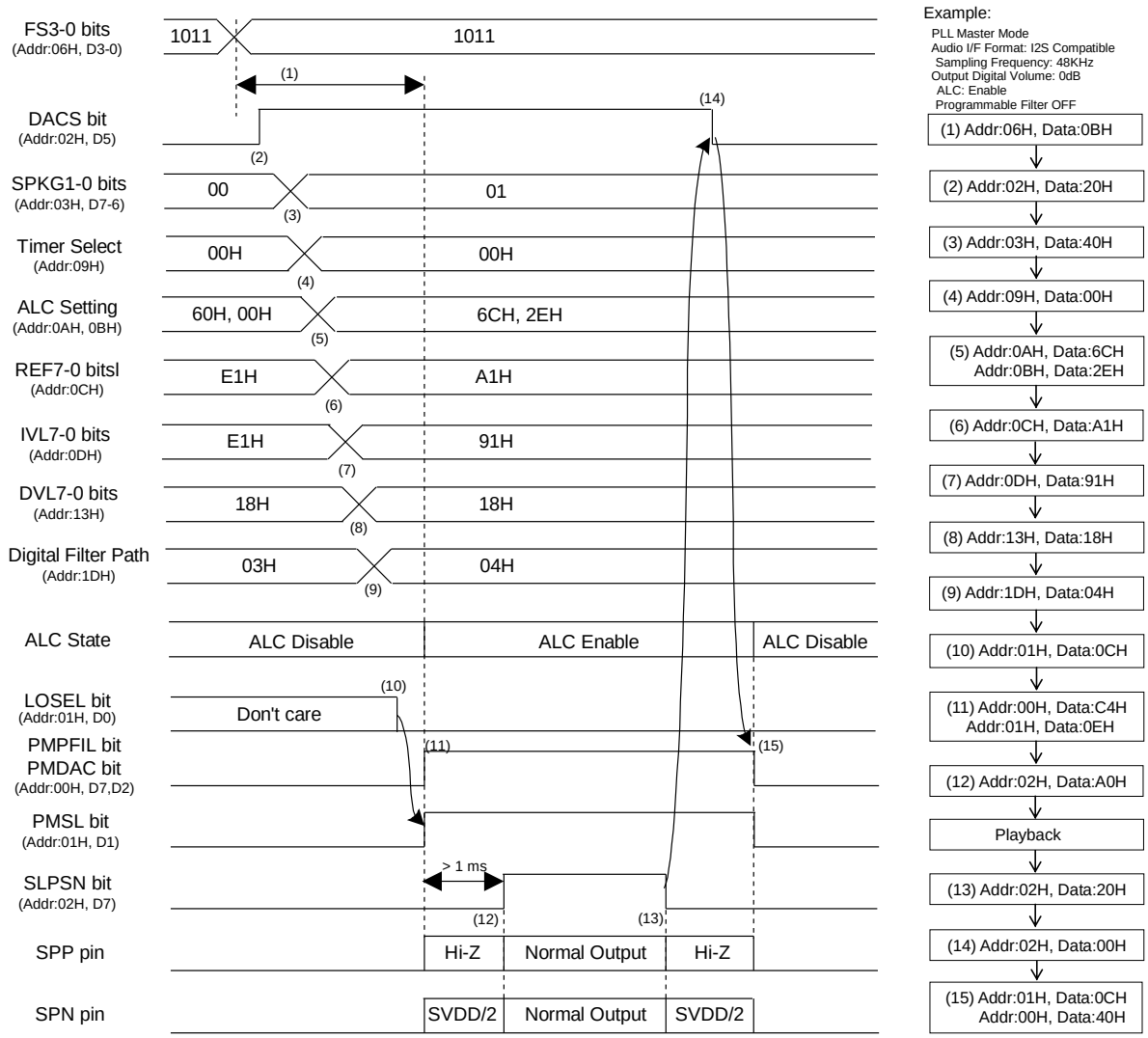


Figure 68. Speaker-Amp Output Sequence

<Sequence>

At first, clocks must be supplied according to “Clock Set Up” sequence.

(1) Set up a sampling frequency (FS3-0 bits). When the AK4951A is in PLL mode, DAC, Programmable Filter and Speaker-Amp of (11) must be powered-up in consideration of PLL lock time after a sampling frequency is changed.
(2) Set up the path of DAC → SPK-Amp: DACS bit = “0” → “1”
(3) SPK-Amp gain setting: SPKG1-0 bits = “00” → “01”
(4) Set up FRN, FRATT and ADRST1-0 bits (Addr = 09H)
(5) Set up ALC mode (Addr = 0AH, 0BH)
(6) Set up REF value of ALC (Addr = 0CH)
(7) Set up IVOL value of ALC operation start (Addr = 0DH)
(8) Set up the output digital volume. (Addr = 13H)
(9) Set up Programmable Filter Path: PFDAC1-0 bits=“01”, PFSDO=ADCPF bits=“0” (Addr = 1DH)
(10) Enter Speaker-Amp Output Mode: LOSEL bit = “0”
(11) Power up DAC, Programmable Filter and Speaker-Amp: PMDAC=PMPFIL=PMSL bits=“0”→“1”
(12) Exit the power-save mode of Speaker-Amp: SLPSN bit = “0” → “1”
(13) Enter Speaker-Amp Power Save Mode: SLPSN bit = “1” → “0”
(14) Disable the path of DAC → SPK-Amp: DACS bit = “1” → “0”
(15) Power down DAC, Programmable Filter and speaker: PMDAC=PMPFIL=PMSL bits= “1”→“0”

■ Beep Signal Output from Speaker Amplifier

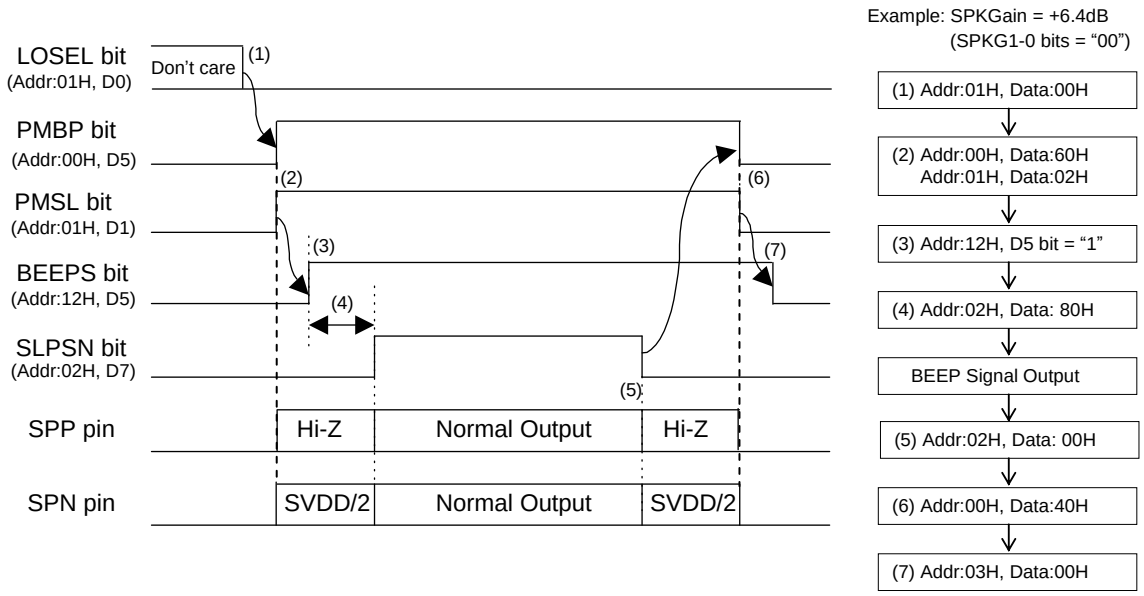


Figure 69. "BEEP-Amp → Speaker-Amp" Output Sequence

<Sequence>
Clock input is not necessary when the AK4951A is operating only on the path of "BEEP-Amp" → "SPK-Amp".

(1) Enter Speaker-Amp Output Mode: LOSEL bit = "0"
(2) Power up VCOM, MIN-Amp and Speaker: PMVCM = PMBP = PMSL bits = "0" → "1"
(3) Set up the path of BEEP → SPK-Amp: BEEPS bit = "0" → "1"
(4) Exit the power save mode of Speaker-Amp: SLPSN bit = "0" → "1"
Period (3) should be set according to the time constant of a capacitor and a resistor that are connected to the BEEP pin. Pop noise may occur if the SPK-Amp output is enabled before the BEEP-Amp input is stabilized. The BEEP Amp is powered up after VCOM voltage rise. The maximum rise-up time of VCOM is 2msec.
(5) Enter Speaker-Amp Power-save mode: SLPSN bit = "1" → "0"
(6) Power Down BEEP-Amp and Speaker: PMBP = PMSL bits = "1" → "0"
(7) Disable the path of BEEP → SPK-Amp: BEEPS bit = "1" → "0"

■ Stop of Clock

When ADC, DAC or Programmable Filter is powered-up, the clocks must be supplied.

1. PLL Master Mode

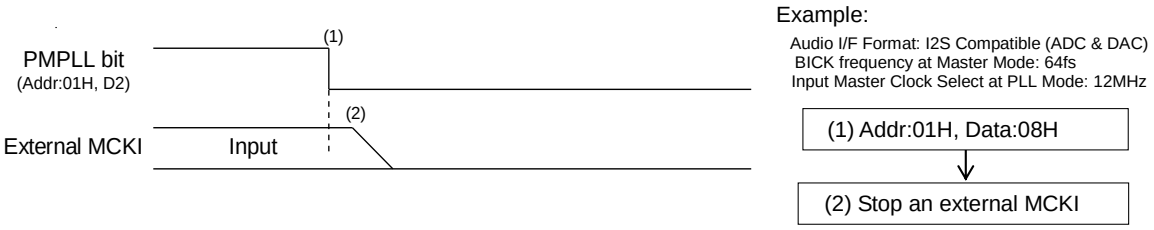


Figure 70. Clock Stopping Sequence (1)

<Sequence>
(1) Power down PLL: PMPLL bit = “1” → “0”
(2) Stop an external master clock.

2. PLL Slave Mode (BICK pin)

Figure 71. Clock Stopping Sequence (2)

<Sequence>
(1) Power down PLL: PMPLL bit = “1” → “0”
(2) Stop an external master clock.

3. EXT Slave Mode

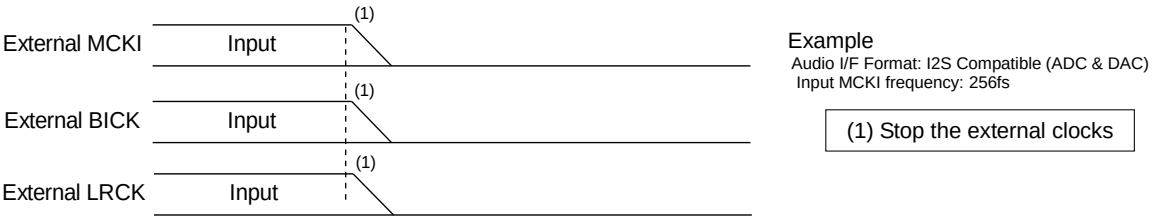


Figure 72. Clock Stopping Sequence (3)

<Sequence>
(1) Stop the external MCKI, BICK and LRCK clocks.

4. EXT Master Mode

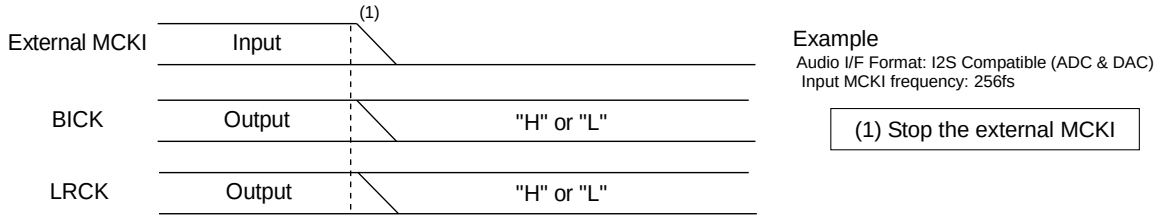


Figure 73. Clock Stopping Sequence (4)

<Sequence>
(1) Stop an external master clock. BICK and LRCK are fixed to “H” or “L”.

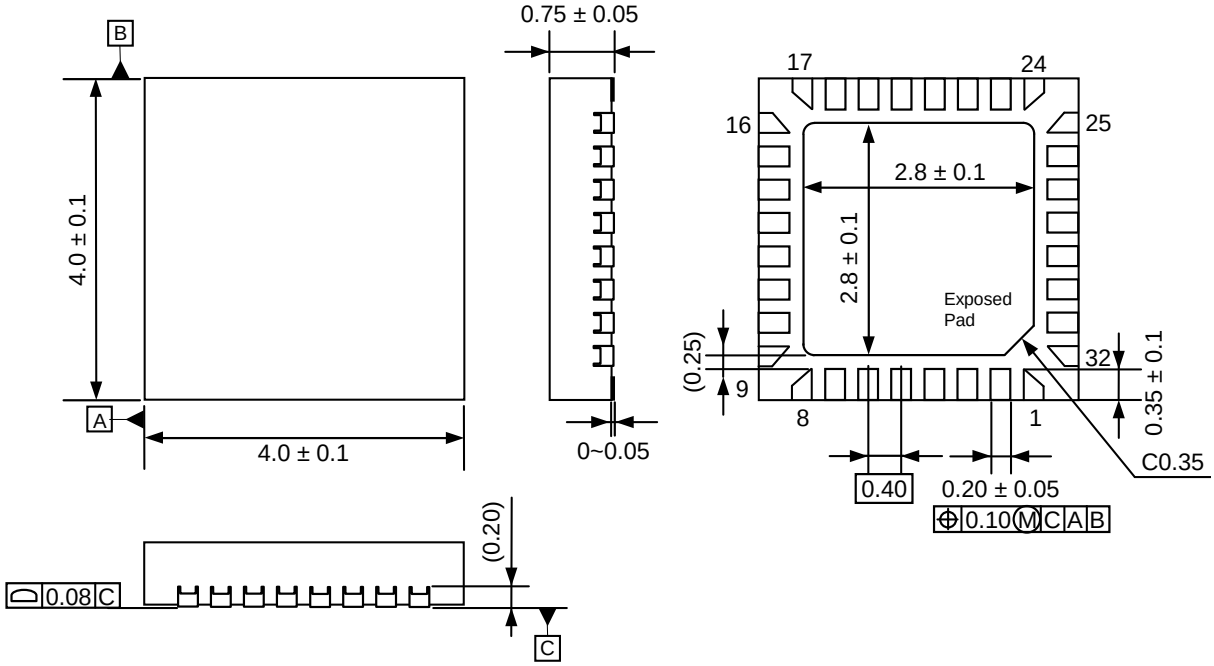
■ Power Down

Power supply current cannot be shut down by stopping clocks and setting PMVCM bit = “0”. Power supply current can be shut down (typ. 1μA) by stopping clocks and setting the PDN pin = “L”. When the PDN pin = “L”, all registers are initialized.

12. Package

■ Outline Dimensions

32-pin QFN (Unit: mm)

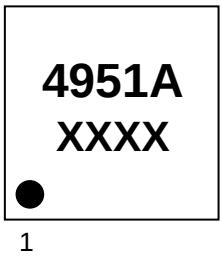


Note. The exposed pad on the bottom surface of the package must be connected to the ground.

■ Material & Lead finish

Package molding compound: Epoxy Resin, Halogen (Br and Cl) free
Lead frame material: Cu Alloy
Pin surface treatment: Solder (Pb free) plate

■ Marking



XXXX: Date code (4 digits)
Pin #1 indication

13. Ordering Guide

AK4951AEN	−40 ~ +85°C	32-pin QFN (0.4mm pitch)
AKD4951AEN	Evaluation board for AK4951AEN	

14. Revision History

Date (Y/M/D)	Revision	Reason	Page	Contents
15/03/18	00	First Edition		

IMPORTANT NOTICE

0. Asahi Kasei Microdevices Corporation (“AKM”) reserves the right to make changes to the information contained in this document without notice. When you consider any use or application of AKM product stipulated in this document (“Product”), please make inquiries the sales office of AKM or authorized distributors as to current status of the Products.
1. All information included in this document are provided only to illustrate the operation and application examples of AKM Products. AKM neither makes warranties or representations with respect to the accuracy or completeness of the information contained in this document nor grants any license to any intellectual property rights or any other rights of AKM or any third party with respect to the information in this document. You are fully responsible for use of such information contained in this document in your product design or applications. AKM ASSUMES NO LIABILITY FOR ANY LOSSES INCURRED BY YOU OR THIRD PARTIES ARISING FROM THE USE OF SUCH INFORMATION IN YOUR PRODUCT DESIGN OR APPLICATIONS.
2. The Product is neither intended nor warranted for use in equipment or systems that require extraordinarily high levels of quality and/or reliability and/or a malfunction or failure of which may cause loss of human life, bodily injury, serious property damage or serious public impact, including but not limited to, equipment used in nuclear facilities, equipment used in the aerospace industry, medical equipment, equipment used for automobiles, trains, ships and other transportation, traffic signaling equipment, equipment used to control combustions or explosions, safety devices, elevators and escalators, devices related to electric power, and equipment used in finance-related fields. Do not use Product for the above use unless specifically agreed by AKM in writing.
3. Though AKM works continually to improve the Product’s quality and reliability, you are responsible for complying with safety standards and for providing adequate designs and safeguards for your hardware, software and systems which minimize risk and avoid situations in which a malfunction or failure of the Product could cause loss of human life, bodily injury or damage to property, including data loss or corruption.
4. Do not use or otherwise make available the Product or related technology or any information contained in this document for any military purposes, including without limitation, for the design, development, use, stockpiling or manufacturing of nuclear, chemical, or biological weapons or missile technology products (mass destruction weapons). When exporting the Products or related technology or any information contained in this document, you should comply with the applicable export control laws and regulations and follow the procedures required by such laws and regulations. The Products and related technology may not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations.
5. Please contact AKM sales representative for details as to environmental matters such as the RoHS compatibility of the Product. Please use the Product in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. AKM assumes no liability for damages or losses occurring as a result of noncompliance with applicable laws and regulations.
6. Resale of the Product with provisions different from the statement and/or technical features set forth in this document shall immediately void any warranty granted by AKM for the Product and shall not create or extend in any manner whatsoever, any liability of AKM.
7. This document may not be reproduced or duplicated, in any form, in whole or in part, without prior written consent of AKM.