# N571P032

# Data Sheet

## 32-BIT VOICE PROCESSOR

## (NuVoice™)

*Release Date: January, 2015*
*Version 1.4*

# 1. General Description

N571P032 is a basic version of *NuVoice*, makes a cost-effective member of N572F065, N572F072/P072 series. CPU is Cortex™-M0, the same core as that of the whole series, but running in a lower frequency at 23MHz. The system resource is 32KB OTP and 4KB SRAM. Integrating analog peripherals, like pre-amplifier, ADC, hardware mixer, and DAC with PA, this chip saves a lot of system design effort and cost.

For N571, the major application is recording and long duration in this version. Regarding voice change or other algorithms running in N572, N571 could run the algorithms of simplified and single features by modification based on requirements of MIPS and SRAM.

Following is a brief table of all Part No. of N571 and N572 Series:

| Part No. | N571P032 | N572F072 | N572P072 | N572F065 |
|---|---|---|---|---|
| Program ROM | 32KB OTP | 72KB Flash | 64KB OTP + 8KB Flash | 64KB Flash |
| SRAM | 4KB | 8KB | 8KB | 8KB |
| CPU freq | 23MHz | 48MHz | 48MHz | 48MHz |
| SPI interface | Master/Slave 23MHz, 1 set | Master/Slave mode 12MHz, 1 set<br>Master mode 36MHz (3.3V), 1 set | | Master mode 12MHz, 2 sets |
| GPIO | 24 | 32 | 32 | 32 |
| USB | N/A | N/A | N/A | FS/12Mbps |

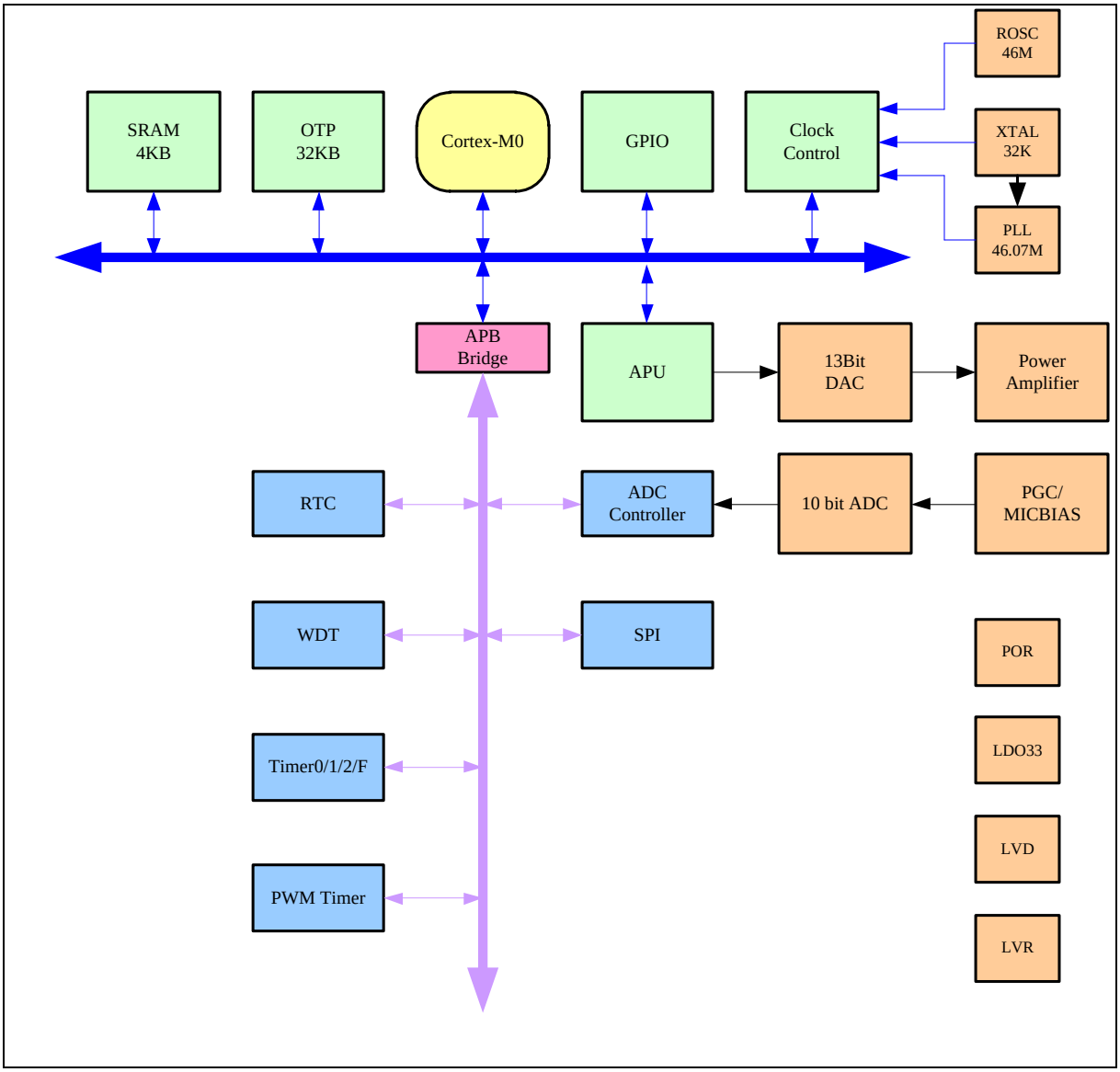
# 2. Features

- **Core**
  - ARM® Cortex™-M0 core runs up to 23MHz
  - Support low power sleep mode
  - Single-cycle 32-bit hardware multiplier
  - NVIC for the 16 interrupt inputs, each with 4-level of priority
  - Serial Wire Debug supports
- **Widely operating voltage range from 2.4V to 5.5V**
- **PROM Memory**
  - 32KB OTP
- **SRAM Memory**
  - 4KB embedded SRAM
- **Clock Control**
  - Support PLL, up to 46MHz from 32768Hz Crystal
  - External 32KHz crystal input for RTC function and system clock
  - Internal 46MHz RC oscillator
- **GPIO**
  - 24 GPIO
- **Timers**
  - 3 sets of the timer with 8-bit pre-scalar and 16-bit timer.

- Counter auto reload.
- IR carrier generator
- One fixed frequency timer

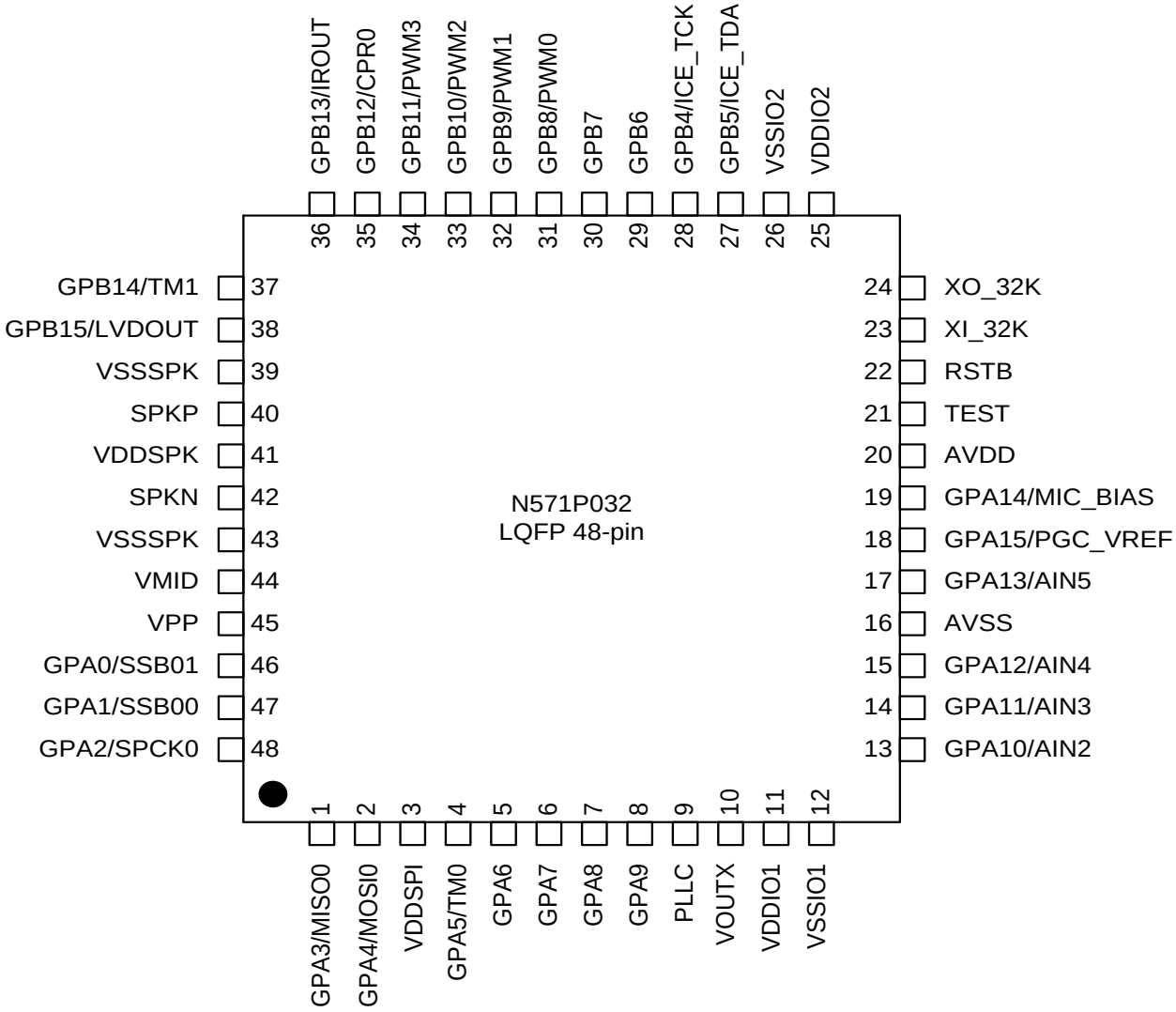
- **Watch Dog Timer**
  - Multiple clock sources
  - 8 selectable time out period (around 30ms~8s based on selecting 32K crystal oscillation as clock source)
  - Able to wake up power down/sleep
  - Interrupt or reset selectable on watchdog time-out
- **RTC**
  - Support time out interrupt
  - Support wake up function
- **PWM/Capture/Compare Timer**
- **SPI**
  - One sets of SPI device
  - Master mode up to 23MHz (3.3V)
  - Support master/slave mode
  - Two 32-bit buffers
- **ADC**
  - 10-bit with 220K conversion rate
  - 1 differential pair input for microphone input
  - Build in H/W DC remove filter
  - Build in up to 16 times up_sampling/filtering/decimation HW to get around additional 2 bits SNR
  - Build in Programmable Gain Control for microphone input
  - Additional 2 inputs for general ADC
  - Build in LDO for PGC/ADC bias
- **APU**
  - 13-bit DAC+PA
  - H/W mixer with 2 channel PCM inputs
  - Build in H/W 4 times PCM repeater and image cancellation filter to remove “metal sound” liked noise
  - Embedded power amplifier
  - 7-level volume control
- **Voltage Detector**
  - with 2 levels: 3.0V/2.7V
- **Voltage Output**
  - Built-in 3.3V regulator power supply Voutx (LDO33) support chip core power and driving external spi-flash
- **Low Voltage Reset 2.2V typical**
- **Operating Temperature: 0℃~70℃**
- **Package**
  - All Green package (RoHS)
  - LQFP 48-pin
  - COB

# 3. Functional Block Diagram



# 4. Pin Configuration

## 4.1 Pin Diagram




## 4.2 Pad Description

| Name | Type | Power | Description |
|---|---|---|---|
| 1. GPIO | | | |
| GPA0 ~ GPA15 | I/O | | Bidirectional general purpose I/O ports. Most of these pins have alternate function, refer to section 0 for detail. |

| | | | |
|---|---|---|---|
| GPB6 ~ GPB15 | I/O | | Bidirectional general purpose I/O ports. Most of these pins have alternate function, refer to section 0 for detail. |
| 2. Oscillator | | | |
| XI_32K | I | VDDIO2 | 32KHz crystal input |
| XO_32K | O | VDDIO2 | 32KHz crystal output |
| PLLC (VCP) | A | LDO33 | Capacitor connection for built-in PLL |
| 3. PGC and ADC | | | |
| AVDD | P | - | 3.0V LDO output for driving ADC and PGC |
| AVSS | P | - | Analog ground |
| MIC_BIAS | A | - | Microphone bias output, can be GPA14 by multi-function-pin setting |
| PGCVREF | A | - | AVDD/2 for PGC. A 4.7uF (or higher) capacitor for low pass filter to filter power noise is needed. can be GPA15 by multi-function-pin setting |
| 4. Speaker Driver | | | |
| SPKP | O | VDDSPK | Speaker positive output pin. |
| SPKN | O | VDDSPK | Speaker negative output pin. |
| VDDSPK*2 | P | - | Analog power supply for DAC/PA, double bond in LQFP48. |
| VSSSPK*2 | P | - | Analog ground for DAC/PA. |
| VMID | A | - | Connect a capacitor to VSSSPK. |
| 5. Power | | | |
| VDDIO2 (VDDIOB) | P | - | Power supply for I/O port |
| VSSIO2 (VSSIOB) | P | - | Ground pin, connect to 0V. |
| VDDIO1 (VDDIOA) | P | - | Power supply for I/O port LVR, LVD and Voutx(LDO33) |
| VSSIO1 (VSSIOA) | P | - | Ground pin, connect to 0V. |
| VDDSPI | P | - | Power supply for GPA0~GPA4 (shared with SPI interface). |
| Voutx (LDO33) | P | - | 3.3V LDO output for driving outside device, internal logic and POR |
| VPP | P | - | Power supply for OTP programming. |
| 6. SWD | | | |
| ICE_TCK | I | VDDIO2 | Serial Wired Debugger Clock, can be GPB4 pin by multi-function-pin setting |
| ICE_TDA | I/O | VDDIO2 | Serial Wired Debugger Data, can be GPB5 pin by multi-function-pin |

| | | | |
|---|---|---|---|
| | | | setting |
| 7. Other | | | |
| RSTB | I | VDDIO2 | Reset input pin, low active. Internal pull-high. |
| TEST | I | VDDIO2 | Test Pin |

## 4.3 Alternate Function List of GPIO

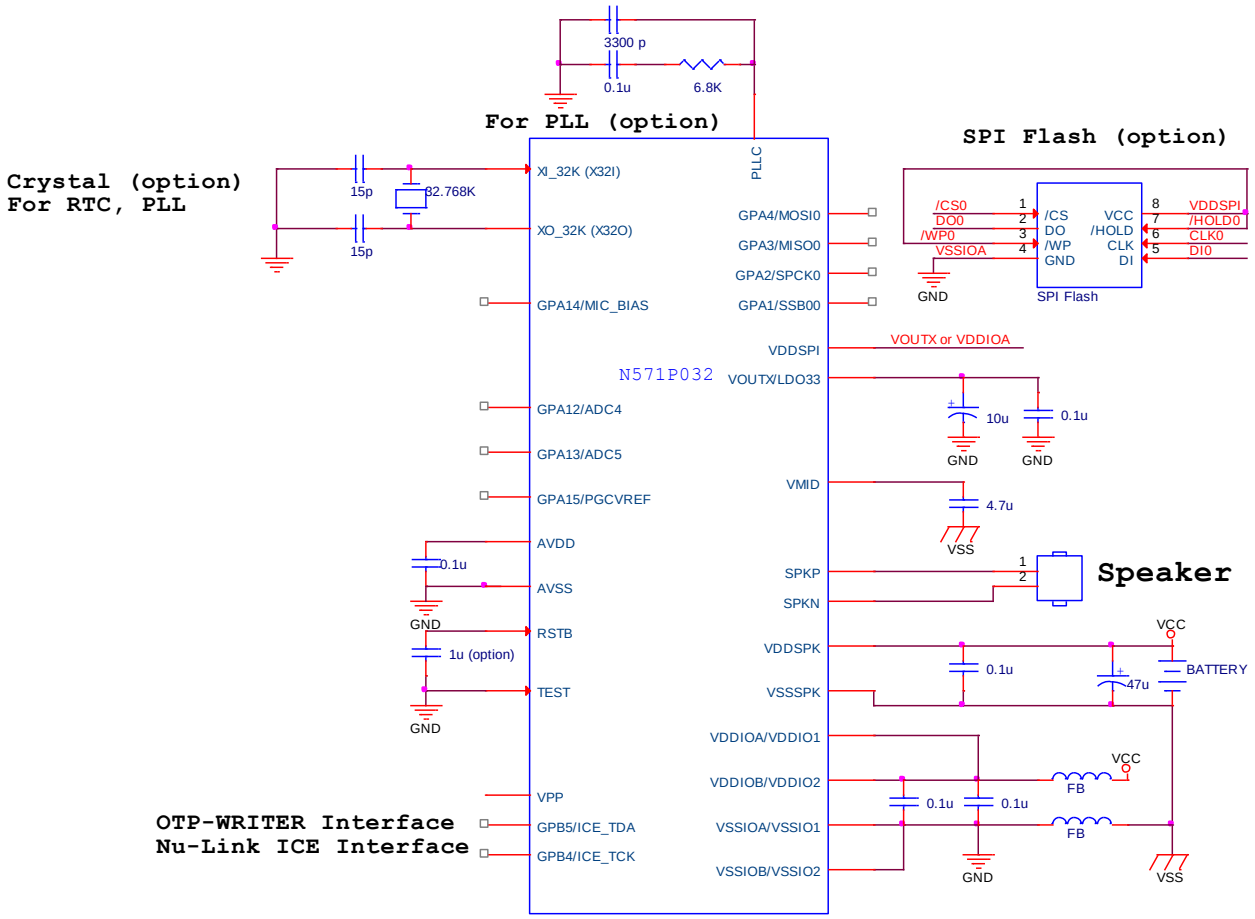
| GPIO | Power | Alternate | I/O of Alternate | Function Description |
|---|---|---|---|---|
| GPA0 | VDDSPI | SSB01 | O | SPI0 2nd chip select output pin |
| GPA1 | VDDSPI | SSB00 | I/O | SPI0 1st chip select output/input pin |
| GPA2 | VDDSPI | SPCK0 | I/O | SPI0 serial clock output/input pin |
| GPA3 | VDDSPI | MISO0 | I/O | SPI0 master data input, slave data output pin |
| GPA4 | VDDSPI | MOSI0 | I/O | SPI0 master data output, slave data input pin |
| GPA5 | VDDIO1 | TM0 | I | Timer0 counter external input |
| GPA6 | VDDIO1 | | | |
| GPA7 | VDDIO1 | | | |
| GPA8 | VDDIO1 | | | |
| GPA9 | VDDIO1 | | | |
| GPA10 | VDDIO1 | AIN2 | A | ADC analog input 2 |
| GPA11 | VDDIO1 | AIN3 | A | ADC analog input 3 |
| GPA12 | VDDIO1 | AIN4 | A | Mic. IN+ |
| GPA13 | VDDIO1 | AIN5 | A | Mic. IN- |
| GPA14 | VDDIO1 | MIC_BIAS | A | MIC Bias |
| GPA15 | VDDIO1 | PGC_VREF | A | PGC Reference Voltage |
| GPB4 | VDDIO2 | ICE_TCK | I | Serial Wired Debugger Clock |
| GPB5 | VDDIO2 | ICE_TDA | I/O | Serial Wired Debugger Data |
| GPB6 | VDDIO2 | - | | |
| GPB7 | VDDIO2 | - | | |
| GPB8 | VDDIO2 | PWM0/HCLK | O | PWM output pin 0 |
| GPB9 | VDDIO2 | PWM1 | O | PWM output pin 1 |
| GPB10 | VDDIO2 | PWM2 | O | PWM output pin 2 |
| GPB11 | VDDIO2 | PWM3 | O | PWM output pin 3 |
| GPB12 | VDDIO2 | CPR0 | I | Capture input |
| GPB13 | VDDIO2 | IROUT | O | IR carrier output |
| GPB14 | VDDIO2 | TM1 | I | Timer1 counter external clock input |
| GPB15 | VDDIO2 | LVDOUT | O | LVD output |

# 5. Typical Application Circuit

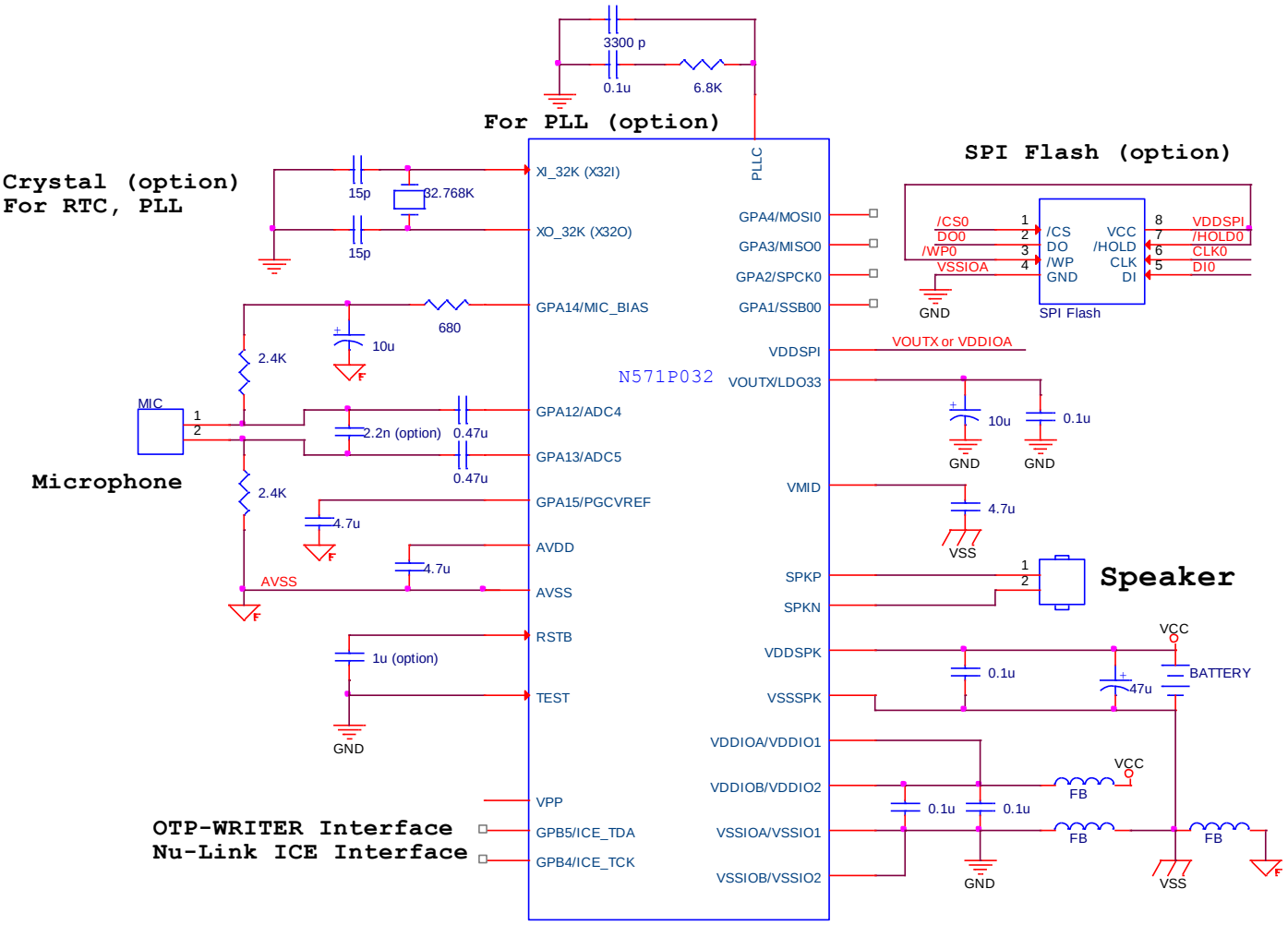
The followings are for general reference.

1. **Crystal is optional**, it is for RTC timer or for the reference clock of internal PLL. XI_32K and XO_32K are no connection for the application without crystal oscillator.
2. **PLL is optional**, it works with crystal oscillation to support higher accuracy system clock. PLLC is no connection for the application does not use PLL.
3. **Do not make VDDSPI spare**, it has to connect to LDO33 (Voutx) or connect to VDDIO based on application's request even if GPA0~4 (share with SPI interface) are spare.
4. **Bypass cap is must for LDO33 (Voutx)** to support chip core power even if the application does not use LDO33 to drive external device.
5. **Bypass cap is must for AVDD**, the power output pad of internal 3V LDO specific for ADC/PGC part, it can use a smaller cap if the application does not use ADC/PGC.
6. **For 2-battery (2*1.5V) and 3-battery (3*1.5V)**, the application circuits can be the same, but connecting VDDSPI to VDDIO can gain higher voltage for 2-battery application with SPI-Flash.

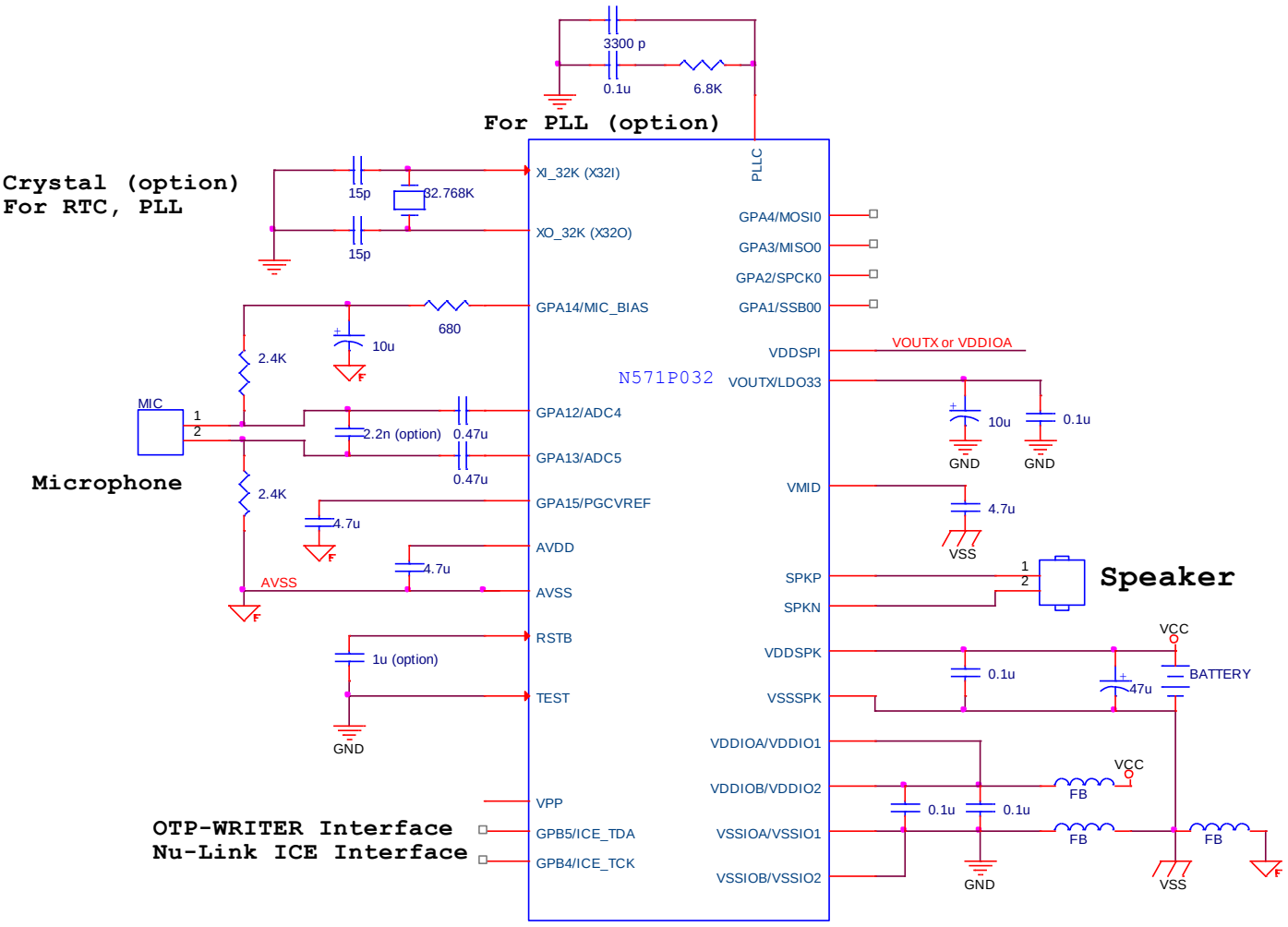
## 5.1 Playback



## 5.2 Recording and Playback



## 5.3 Application without SPI-Flash



# 6. Supported Codec

Following table shows the supported codec and suggested sample rate and corresponding bit rate. The Bit Rate of NuOne, NuLite, and NuSound could be configurable. For example, using 8K sample rate, the bit rate could be 8Kbps (1bit per sample) or 12Kbps (1.5 bit per sample) or 16Kbps (2 bit per sample). Details please refer to document in SDS.

| Codec | Sample Rate (Hz) | Bit Rate (bps) | For | Availability |
|---|---|---|---|---|
| NuOne | 16K | 16K | Speech, Music | Codec |
| NuLite | 8K | 12K | Speech, Music | Codec |
| NuSound | 16K | 32K | Speech, Music | Decoder |
| MD4 | 16K | 68.8K | Speech, Music | Decoder |
| IMAADPCM | 16K | 64K | Speech, Music | Codec |
| LP8 | 16K | 128K | Speech, Music | Codec |
| NuVox53/63 | 8K | 5.3K/6.3K | Speech | Decoder |

# 7. Electrical Characteristics

## 7.1 Absolute Maximum Ratings

| SYMBOL | PARAMETER | MIN | MAX | UNIT |
|---|---|---|---|---|
| DC Power Supply | VDD–VSS | -0.3 | +7.0 | V |
| Input Voltage | VIN | VSS-0.3 | VDD+0.3 | V |
| CPU Frequency | $1/t_{CLk}$ | 0 | 23 | MHz |
| Operating Temperature | TA | 0 | 70 | °C |
| Storage Temperature | TST | -55 | +150 | °C |
| Maximum Current into $V_{DD}$ | | - | 120 | mA |
| Maximum Current out of $V_{SS}$ | | | 120 | mA |
| Maximum Current sunk by an I/O pin | | | 35 | mA |
| Maximum Current sourced by an I/O pin | | | 35 | mA |
| Maximum Current sunk by total I/O pins | | | 100 | mA |
| Maximum Current sourced by total I/O pins | | | 100 | mA |

## 7.2 DC Electrical Characteristics

VDD-VSS=4.5V, TA=25°C, unless otherwise specified.

| PARAMETER | SYM | SPECIFICATION | | | | TEST CONDITIONS |
|---|---|---|---|---|---|---|
| | | MIN. | TYP. | MAX. | UNIT | |
| Operation voltage | $V_{DD}$ | 2.4 | | 5.5 | V | |
| Power Ground | $V_{SS}$ $AV_{SS}$ | -0.3 | | | V | |
| Analog Operating Voltage | $AV_{DD}$ | 0 | | $V_{DD}$ | V | |
| Analog Reference Voltage | Vref | 0 | | $AV_{DD}$ | V | |
| Operating Current at Normal Run Mode | $I_{DD1}$ | | 14 | | mA | $V_{DD}$=5.5V@46MHz, enable all IPs |
| | $I_{DD3}$ | | 14 | | mA | $V_{DD}$=3V@46MHz, enable all IPs |
| Operating Current at Idle Mode | $I_{IDLE2}$ | | 8.5 | | mA | $V_{DD}$=5.5V@46MHz, disable all IPs |
| | $I_{IDLE4}$ | | 8.5 | | mA | $V_{DD}$=3V@46MHz, disable all IPs |
| Operating Current at Power-down Mode | $I_{PWD1}$ | | | 6 | μA | $V_{DD}$ = 5.5V, No load, disable all IPs |
| | $I_{PWD2}$ | | | 5 | μA | $V_{DD}$ = 3.3V, No load, disable all IPs |
| Input Current GPA/GPB (Quasi-bidirection Mode) | $I_{IN1}$ | -60 | -65- | -70 | μA | $V_{DD}$ = 5.5V, $V_{IN}$ = 0V |
| Input Current GPA/GPB | $I_{IN1}$ | 0.1 | 0.5 | 1 | μA | $V_{DD}$ = 5.5V, $V_{IN}$=$V_{DD}$ |

| | | | | | | |
|---|---|---|---|---|---|---|
| (Quasi-bidirection Mode) | | | | | | |
| Input Current at RSTB [1] | $I_{IN2}$ | -60 | -80 | -100 | μA | $V_{DD}$ = 5.5V, $V_{IN}$ = 0.45V |
| Input Leakage Current GPA/GPB | $I_{LK}$ | -2 | - | +2 | μA | $V_{DD}$ = 5.5V, 0<$V_{IN}$<$V_{DD}$ |
| Input negative going Low Transfer Voltage GPIO (Schmitt trigger input) | $V_{IL1}$ | -0.5 | - | 1.35 | V | $V_{DD}$ = 4.5V |
| | | -0.5 | - | 0.9 | | $V_{DD}$ = 3.0V |
| Input positive going High Transfer Voltage GPIO (Schmitt trigger input) | $V_{IH1}$ | 3.15 | - | 5 | V | $V_{DD}$ = 4.5V |
| | | 2.1 | - | 3.5 | | $V_{DD}$ = 3.0V |
| Source Current GPA/GPB (Quasi-bidirectional Mode) | $I_{SR11}$ | -35 | -36 | -38 | μA | $V_{DD}$ = 4.5V, $V_S$ = 2.4V |
| | $I_{SR12}$ | -5 | -7 | -9 | | $V_{DD}$ = 2.7V, $V_S$ = 2.2V |
| Source Current GPA/GPB (Push-pull Mode) | $I_{SR21}$ | -28 | -29 | -30 | mA | $V_{DD}$ = 4.5V, $V_S$ = 3.0V |
| | $I_{SR22}$ | -6 | -7 | -8 | | $V_{DD}$ = 2.7V, $V_S$ = 2.2V |
| Sink Current GPA/GPB (Quasi-bidirectional and Push-pull Mode) | $I_{SK1}$ | 10 | 11 | 12 | mA | $V_{DD}$ = 4.5V, $V_S$ = 0.45V |
| | $I_{SK2}$ | 6 | 7.5 | 9 | | $V_{DD}$ = 2.7V, $V_S$ = 0.45V |

**Notes:** 1. RSTB pin is a Schmitt trigger input.

## 7.3 AC Electrical Characteristics

The following data are measured under VDD-VSS=4.5V, TA=25°C, unless otherwise specified.

### 7.3.1 Internal 46MHz RC Oscillator

| PARAMETER | CONDITION | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|
| Supply Voltage VDD | | 2.4 | 3.3 | 3.6 | V |
| Center Frequency | | | 46.0 | | MHz |
| Calibrated Internal Oscillator Frequency | +25°C; VDD = 3.3V | -2 | | +2 | % |
| | 0°C ~+70°C; $V_{DD}$=2.7V~3.6V | -5 | | +5 | % |

## 7.4 Analog Characteristics

The following data are measured under VDD-VSS=4.5V, TA=25°C, unless otherwise specified.

### 7.4.1 10-bit SAR ADC

| PARAMETER | SYM. | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|
| Resolution | - | - | - | 10 | Bit |
| Differential nonlinearity error | DNL | - | ±1 | - | LSB |
| Integral nonlinearity error | INL | - | ±1 | - | LSB |
| Offset error | EO | - | ±1 | - | LSB |
| Gain error (Transfer gain) | EG | - | 1 | - | - |
| Monotonic | - | Guaranteed | | | - |
| ADC clock frequency | FADC | 0.5 | - | 2.64 | MHz |
| Sample & Conversion time | TADC | 12 | | - | Clock |
| Sample rate | FS | - | - | 220 | Ksps |
| Supply voltage | VDD | 2.7 | | 5.5 | V |
| | AVDD | 2.7 | 3.3 | 3.6 | V |
| Supply current (Avg.) | IDD | - | 0.7 | - | mA |
| Reference voltage | VREFP | - | AVDD | - | V |

### 7.4.2 Programmable Gain Control (for Voice Recorder)

| Parameter | Sym. | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Operation Voltage | VDDA | AVDD | 2.7 | 3.3 | 3.6 | V |
| Operation Current | IDD | | | 1.5 | | mA |
| Preamp Gain | PreG | | 0 | | 20 | dB |
| Post Gain | PostG | | 14 | | 34 | dB |
| Offset Bit | OS | 6-bit Control | -64 | | 64 | mV |
| THD+N | THD+N | Gain=40dB, | | -50 | | dB |

### 7.4.3 Voutx (3.3V LDO) for External Driving

| Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Input Voltage | | 3.3 | - | 5.5 | V |
| Output Voltage | | -10% | 3.3 | +10% | V |
| $I_{load}$ | VDD = 4.5V | | 50 | | mA |

### 7.4.4 Low Voltage Reset

| PARAMETER | CONDITION | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|
| Threshold voltage | Temperature=25°C | 2.1 | 2.2 | 2.5 | V |

### 7.4.5 Voltage Detector

| PARAMETER | CONDITION | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|
| Detected Voltage | LVD_VL = 0 | 2.43 | 2.7 | 3.0 | V |
| | LVD_VL = 1 | 2.7 | 3.0 | 3.3 | V |

### 7.4.6 Power Amplifier

| PARAMETER | CONDITION | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|
| Operation voltage | VDDSPK | 2.4 | 4.5 | 5.5 | V |
| Output Power | VDDSPK=4.5V, 8Ω BTL load, 0dB gain | | 450 | | mW |
| Total Harmonic Distortion | VDDSPK=4.5V, 8Ω BTL load, 0dB gain, 400mW | | -41 | | dB |
| Power Amplifier Gain | | -18 | | 0 | dB |
| Power Amplifier Quiescent Current | DAC fine-tuned, VDDSPK=4.5V | | 11 | | mA |
| Power Down Current | DAC fine-tuned, VDDSPK=4.5V | | | 0.1 | μA |
| Operation Current | VDDSPK=4.5V, 400mW | | 250 | | mA |

# 8. Ordering Information

| PART NUMBER | PACKAGE | SPECIAL FEATURE | PB FREE + HALOGEN FREE (GREEN) | RELEASE DATE |
|---|---|---|---|---|
| N571P032 | **NA (Die Form)** | **OTP** | **Yes** | **Dec, 2012** |
| N571P032G | **LQFP 48pin 7mmx7mm** | **OTP** | **Yes** | **Dec, 2012** |
| | | | | |

# 9. Revision History

| VERSION | DATE | PAGE/CHAH. | DESCRIPTIONS |
|---|---|---|---|
| 1.0 | Oct., 2012 | | Preliminary draft |
| 1.1 | Nov., 2012 | | With ver-A AC/DC characteristics |
| 1.2 | Jan., 2013 | | Update Operating Temperature, $V_{IL1,}$ $V_{IH1,}$ |
| 1.3 | Apr., 2013 | | Update DC parameter<br>Remove 'Preliminary' |
| 1.4 | Jan., 2015 | | Update Application Circuit.<br>Update Electrical Characteristic: Power-Down current, Voltage Detector, Program Gain Control Offset/THD+N, Voutx (LDO33).<br>Change Software and Development Environment to Supported Codec and remove the others.. |

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