# W55P241

## *Table of Contents-*

## 1. GENERAL DESCRIPTION

The W55P241 is a general purpose programmable I/O device usable with many different microprocessors through SPI interface. The W55P241 contains three 8-bit ports (BP0, BP1 and BP2). There are 24 I/O pins which may be individually programmed for 4 separate command groups. The W55P241 features logical operating capability AND/OR/XOR for each bit of internal configuration register to speed up access. These I/O pins can drive LED directly with high-current applications. A dedicated counter is in charge of 256-level output functions.

## 2. FEATURES

- Wide range of operating voltage:
  - ➢ 2.2~5.5V
- SPI interface in mode 0
  - ➢ 4 SPI pins for communication
    - − /CS as chip select pin (low active)
    - − CLK for data synchronization (up to 10MHz)
    - − DI for W55P241 to receive commands and data
    - − DO for the microcontroller to receive data
- 1 wakeup pin for the microcontroller
- 24 I/O pins
  - ➢ 24 bi-directional I/O pins with 25mA of sink current
  - ➢ Status of each pin independently controlled
    - o Input
      - ▪ Floating
      - ▪ Pull high
      - ▪ Pull low
      - ▪ Dynamic pull low
      - ▪ Dynamic pull high
    - o Output
      - ▪ CMOS high/low
      - ▪ Inverted CMOS high/low
      - ▪ Inverted open-drain NMOS output
      - ▪ Open-drain PMOS output
  - ➢ Any pin can be selected to wake up the chip
  - ➢ Logic AND/OR/XOR to execute high-speed operations for each of these I/O control register bits
- Built-in 8 LED outputs with 256-level brightness control in the BP0 port
  - ➢ Internal ring oscillator @ 8MHz
  - ➢ 4 clock sources
    - o Clock/512, /256, /64, /16

- Reset management
  - ➢ Power-on reset
  - ➢ S/W reset
- Standby current <1uA
- Connection of up to 2 W55P241 devices
- Available package form:
  - o COB
  - o LQFP48
  - o QFN32 (no support BP07, BP17, BP26, BP27)

## 3. PIN DESCRIPTION

| PIN NAME | TYPE | FUNCTION |
|---|---|---|
| BP00~BP07 | I/O | General input/output pins. When used as output pins, they can be open-drain or CMOS-type and can sink 25mA for high-current applications. When used as input pins, they have a pull-high option and can generate an interrupt request to release the IC from STOP mode.<br><br>The default is input floating in the BP0 port. The BP0 port provides 8 LED outputs with 256-level brightness control. |
| BP10~BP17 | I/O | General input/output pins. When used as output pins, they can be open–drain or CMOS type and can sink 25mA for high-current applications. When used as input pins, they have a pull-high option and can generate an interrupt request to release the IC from STOP mode.<br><br>The default is input floating in the BP1 port. |
| BP20~BP27 | I/O | General input/output pins. When used as output pins, they can be open–drain or CMOS type and can sink 25mA for high-current applications. When used as input pins, they have a pull-high option and can generate an interrupt request to release the IC from STOP mode.<br><br>The default is input floating in the BP2 port. |
| /CS | I | SPI chip select (low active) |
| CLK | I | SPI clock |
| DI | I | SPI data input (MOSI) |
| DO | O | SPI data output (MISO) |
| DIS | I | Device ID setting(default is floating) |
| WAKEUP | O | Host wakeup |
| VDD | P | Positive power supply for logical device |
| VSS | P | Negative power supply for logical device |
| VDDIO1 | P | Positive power supply for IO |
| VSSIO1 | P | Negative power supply for IO |
| VDDIO2 | P | Positive power supply for IO |
| VSSIO2 | P | Negative power supply for IO |

## 4. BLOCK DIAGRAM

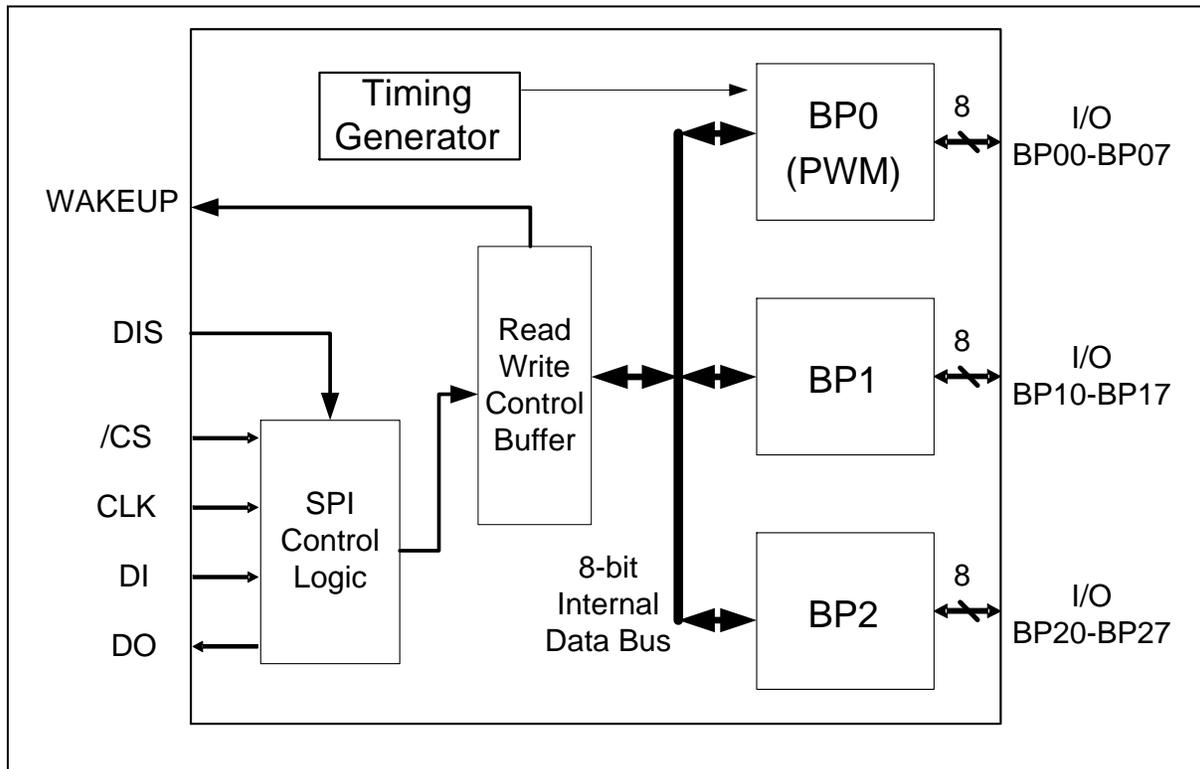

Figure 1 W55P241 Block Diagram

## 5. FUNCTIONAL DESCRIPTION

The W55P241 provides up to three bi-directional ports. Each bi-directional port has 8 pins (BP00~07, BP10~17, or BP20~27) and each bi-directional pin can be configured as an output pin or input pin independently. One dedicated wakeup pin forcibly releases the microcontroller from the standby mode. When selected as an input pin, the state change on each pin can trigger interrupt request, if the corresponding interrupt enabling bit is set. These three bi-directional ports, when programmed as an output port, can sink at least 25-mA current in order to drive LED directly. With an embedded 256-level output circuit, motor speed control and LED brightness are available in BP00~BP07.

### 5.1 SPI

SPI is a direct and simple interface that uses 4 pads (/CS, CLK, DI and DO) for data exchange between master and slave. W55P241 operates in the slave mode and up to 2 W55P241 devices can function simultaneously. The master identifies the slaves which are differentiated by the DIS pad. Because W55P241 operates in mode 0 only, the CLK idle state is always "0", "receive data" is always latched at the rising edge of CLK, and "transmit data" is always changed (if at all) at the falling edge of CLK. To control one SFR of W55P241, 16 bits of serial data must be transmitted from the master. 16 bits of serial data consist of 1 command byte and 1 data byte. Basically, 4 groups of commands are defined and the IO port group suffices to generate all possible IO statuses. Users may use 3 other speedup groups to minimize microcontroller load.

### 5.1.1 Physical Connection

The uC master may connect up to 2 slave devices as shown in the following figure. The W55P241 always operates in the slave mode. The master can be a microcontroller with 4 I/O pads or a dedicated SPI H/W. Each time the master wants to talk to one of the slaves, bit6 of command byte must be correctly specified. Slaves are identified by the DIS pad status. The master communicates with the slave via 4 SPI pads. In addition to bit6 of command byte, /CS must be asserted (low active) for W55P241 to receive the command. The W55P241 CLK runs on up to 10MHz. DI (master data output, slave data input) and DO (master data input, slave data output) exchange data between the microcontroller and the W55P241. To wake up the microcontroller, the WAKEUP or DO pad may connect to its one additional wakeup-enabled pad.
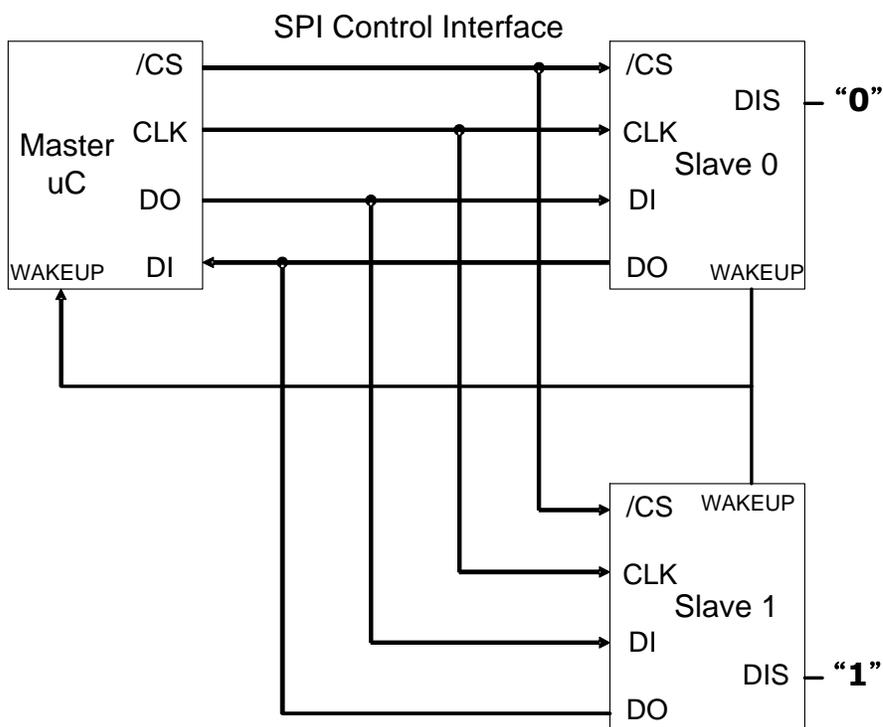


Figure 2 Connection of Master and Slave

### 5.1.2 Mode 0

Generally, the master's dedicated SPI H/W (hardware) may support up to 4 SPI operation modes, which are determined by the CLK's idle state and phase (rising edge and falling edge). In the W55P241, only mode 0 is supported. For both master and slave, data is transmitted on the falling edge of CLK and data is received (sampled) on the rising edge of CLK. CLK keeps "0" before the 1st rising edge and after the last falling edge.
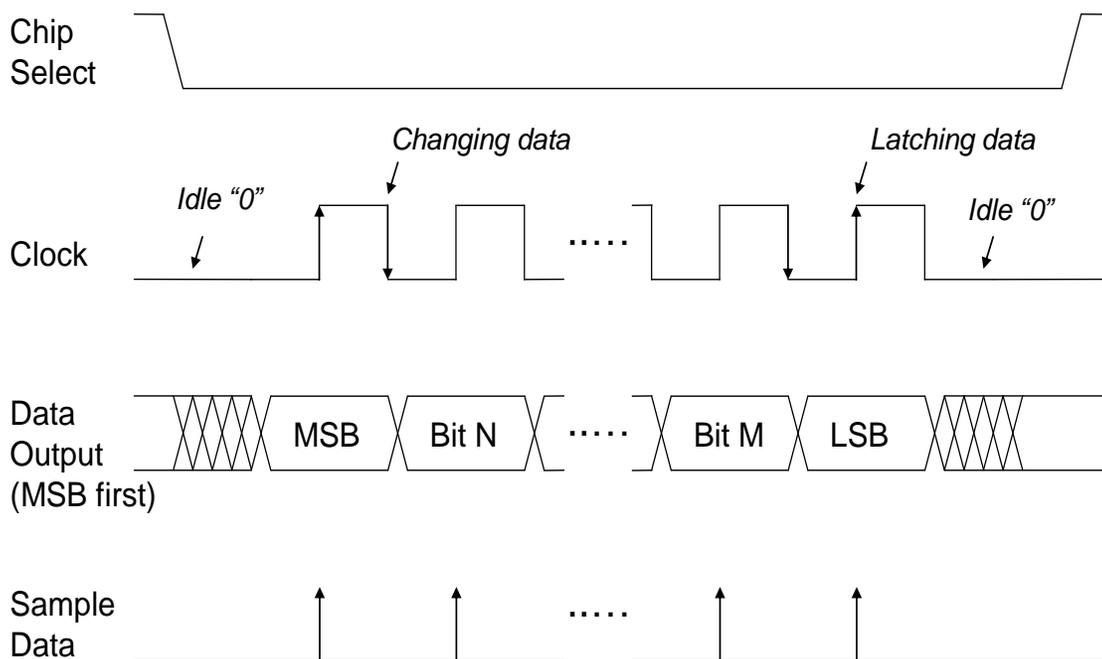
Figure 3 SPI mode 0 (MSB first)

### 5.1.3  Command Protocol

One SPI transfer consists of one command byte and one data byte. Because the 1$^{st}$ 8 bits of "transmit data" are regarded as command byte after the falling edge of /CS, it is not possible that /CS remains "0' during two successive SPI transfers. The last 8 bits of "transmit data" in one SPI transfer are regarded as data bytes. For both command byte and data byte to be identified by the W55P241, MSB (Most Significant Bit) is transferred first. When the microcontroller writes data to W55P241, DO remains in high impedance state during the whole SPI transfer. When the microcontroller reads data from the W55P241, DO remains in high impedance state until the data byte is generated.

/CS — Write command

CLK

DI — "1" C6 C5 C4 C3 C2 C1 C0 W7 W6 W5 W4 W3 W2 W1 W0

DO — *HZ*

/CS — Read command

CLK

DI — "0" C6 C5 C4 C3 C2 C1 C0 X X X X X X X X

DO — *HZ* — R7 R6 R5 R4 R3 R2 R1 R0
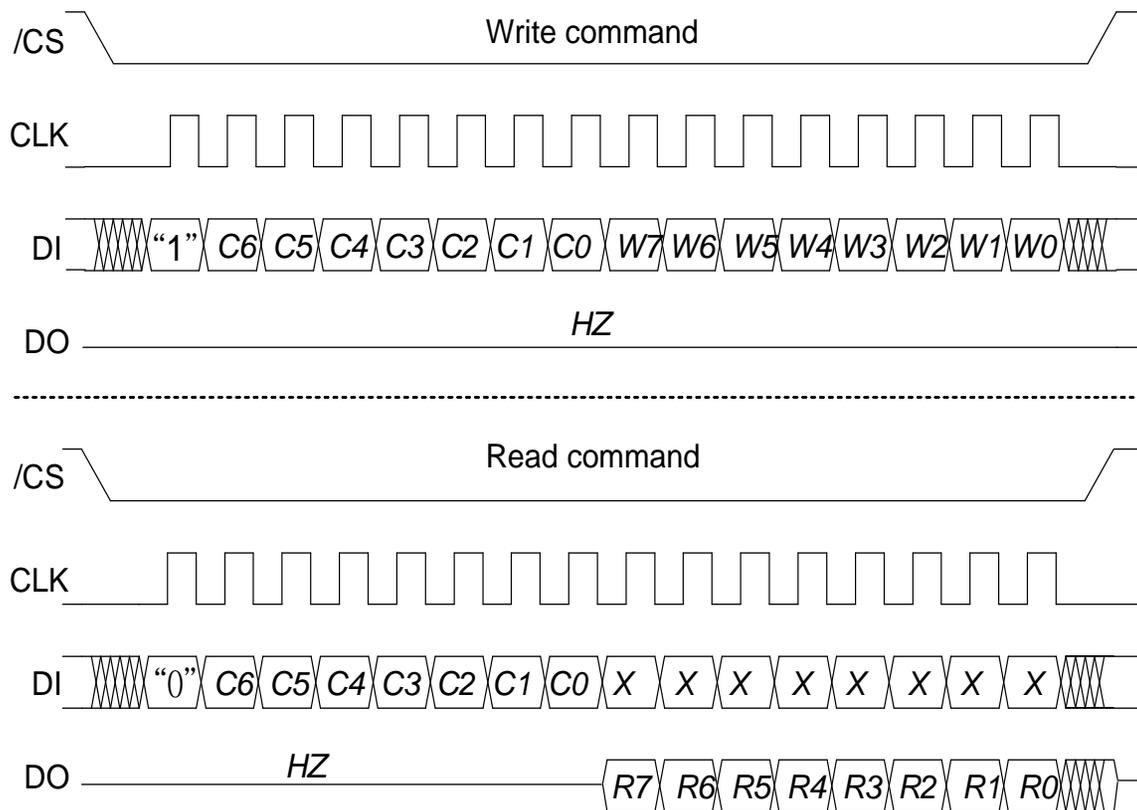
*Cn*: command bit. *Wn*: write data bit. *Rn*: read data bit.
*HZ*: high impedance. *X*: don't care. *7 -> 0*: MSB -> LSB.

Figure 4 Write command and read command

The command byte's Bit7 determines "write data to W55P241" or "read data from W55P241". The command byte's Bit6 selects slave device 0 or slave device 1. Bit5 and bit4 of command byte specify the command group while Bit3~bit0 of command byte control some Special Function Registers (SFR) in one specific group. The following table roughly lists all the commands.

| Command | Read/write | Device | Group | | Special Function Register | | | |
|---------|-----------|--------|-------|------|------|------|------|------|
| | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| Write | 1 | 0 or 1 | SFR of one specific group | | | | | |
| Read | 0 | 0 or 1 | SFR of one specific group | | | | | |
| Reset | 0xFF | | | | | | | |
| No response | Settings except write, read and reset commands | | | | | | | |

Table 1 Command list

## 5.2  BP0/BP1/BP2

Each bi-directional pin can be controlled independently and IO status (or function) is determined by Buffer bit, Direction bit and Attribute bit. In input mode, reading the Pin bit reveals the status of the corresponding I/O pin. The combinations are listed in the following table. For simplicity, B stands for Buffer, D stands for Direction, A stands for Attribute, and P stands for Pin.

| ATTRIBUTE | DIRECTION | BUFFER | IO status | Function |
|---|---|---|---|---|
| 0 | 0 | 0 | Floating(default) | Floating input |
| 0 | 0 | 1 | Pull low | Pull-low input |
| 1 | 0 | 1 | Pull high | Pull-high input |
| 0 | 1 | 0 | Output low | Buffer output |
| 0 | 1 | 1 | Output high | |
| 1 | 0 | 0 | Floating | Open-drain PMOS output |
| 1 | 1 | 0 | Output high | |
| 1 | 0 | 1 | Pull high | Wire AND (inverted) |
| 1 | 1 | 1 | Output low | |
| 0 | 1 | 0 | Output low | Open-drain NMOS output (inverted) |
| 0 | 0 | 0 | Floating | |
| 0 | 0 | 1 | Pull low | Wired OR |
| 0 | 1 | 1 | Output high | |
| 0 | 0 | 0 | Floating | Dynamic pull-low input |
| 0 | 0 | 1 | Pull low | |
| 1 | 0 | 0 | Floating | Dynamic pull-high input |
| 1 | 0 | 1 | Pull high | |
| 1 | 1 | 0 | Output high | Inverted buffer output |
| 1 | 1 | 1 | Output low | |

Table 2 Combination of IO status

### 5.2.1   Input with High Impedance

When Attribute bit = 0 or 1, Direction bit = 0 and Buffer bit = 0, the pad is in floating input mode. Value of the Pin bit depends on the corresponding pad.
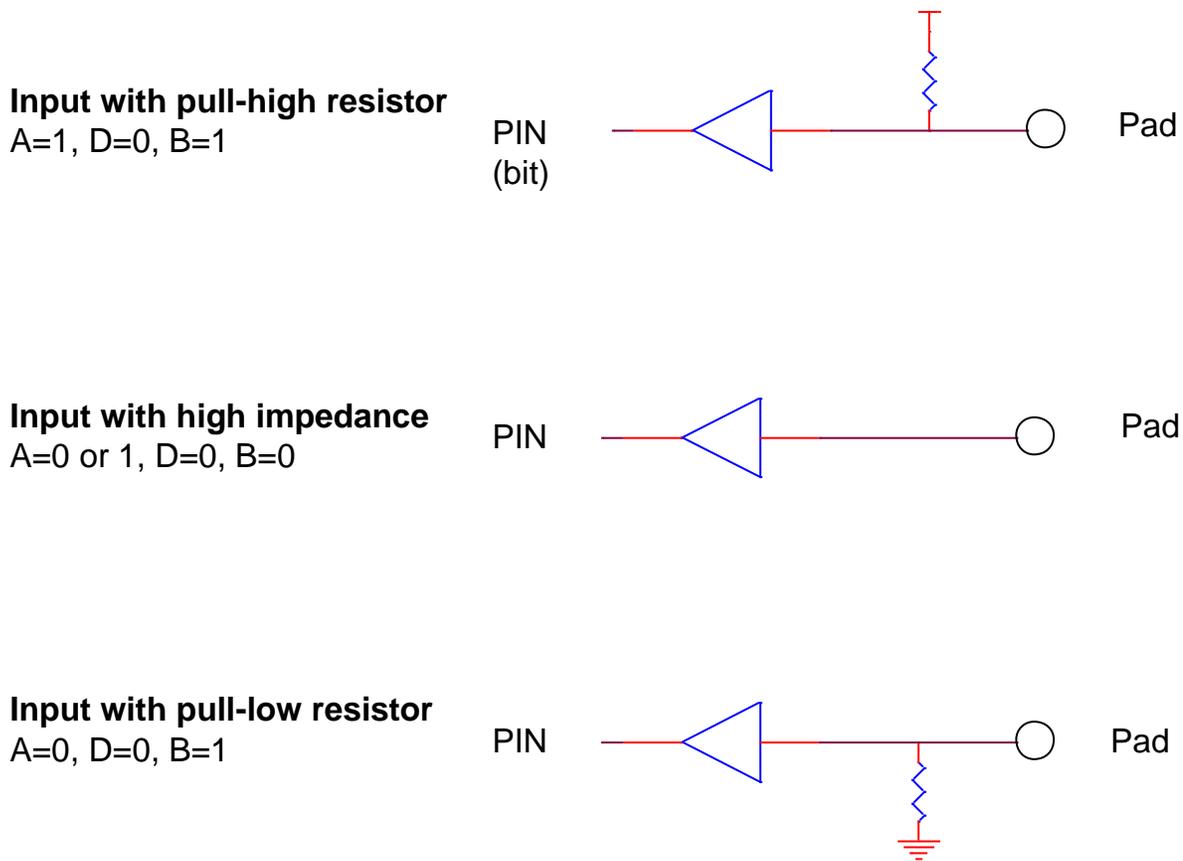
**Input with pull-high resistor**
A=1, D=0, B=1

PIN
(bit)

Pad

**Input with high impedance**
A=0 or 1, D=0, B=0

PIN

Pad

**Input with pull-low resistor**
A=0, D=0, B=1

PIN

Pad

Figure 5 Pure input

#### 5.2.2   Input With Pull-High Resistor

When Attribute bit = 1, Direction bit = 0 and Buffer bit = 1, the pad is in pull-high input mode. Pin bit is 1 when no external H/W is connected or the pad is forced to "1" by external H/W. Pin bit is 0 when the pad is forced to "0" by external H/W.

#### 5.2.3   Input With Pull-Low Resistor

When Attribute bit = 0, Direction bit = 0 and Buffer bit = 1, the pad is in pull-low input mode. Pin bit is 0 when no external H/W is connected or the pad is forced to "0" by external H/W. Pin bit is 1 when the pad is forced to 1 by external H/W.

#### 5.2.4   CMOS Output

When Attribute bit = 0 and Direction bit = 1, the pad is in CMOS output mode and the Buffer bit determines the state of the pad. If Buffer bit = 0, the pad will be set to "0". If Buffer bit = 1, the pad will be set to "1". Pin bit directly indicates pad status.
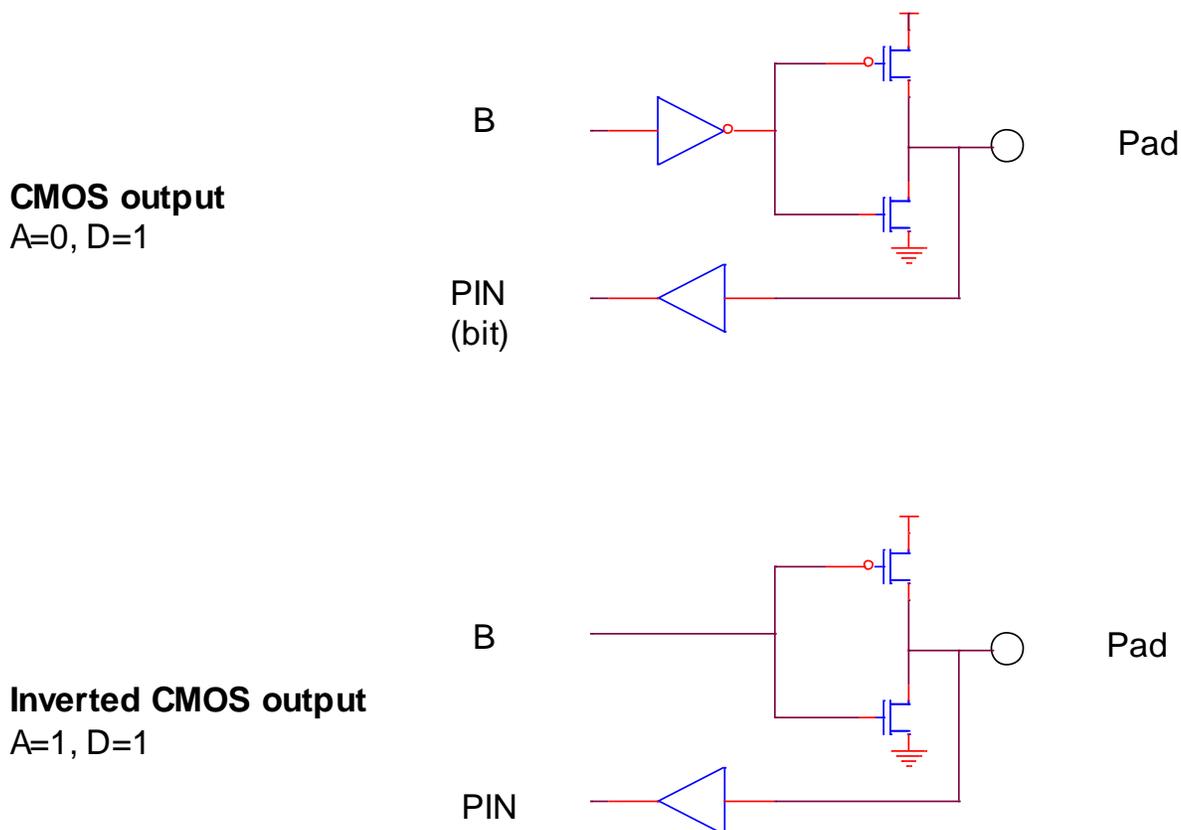
Figure 6 Normal and inverted CMOS output

### 5.2.5　Inverted CMOS Output

When Attribute bit = 1 and Direction bit = 1, the pad is in inverted CMOS output mode and the Buffer bit determines pad state. Unlike CMOS output mode, pad state is indirectly controlled by the Buffer bit in inverted CMOS output mode. If Buffer bit = 0, the pad will be set to "1." If Buffer bit = 1, the pad will be set to "0." Pin bit directly indicates pad status.

### 5.2.6　Inverted Open-Drain NMOS Output

When Attribute bit = 0 and Buffer bit = 0, the pad is in inverted open-drain NMOS output mode. If Direction bit is 0, the pad will be floating. In this case, the pad functions like floating input. If Direction bit is 1, the pad will be set to "0." Pin bit directly indicates pad status.

**Inverted open-drain NMOS output**
A=0, B=0
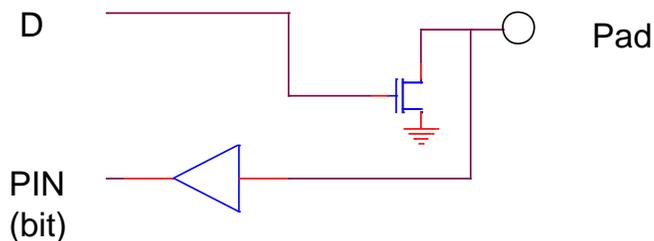
**Open-drain PMOS output**
A=1, B=0
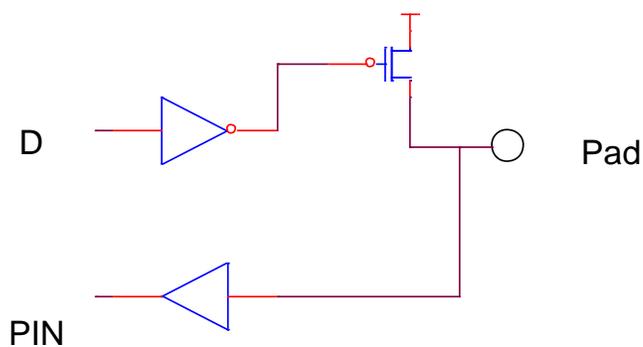
Figure 7 Inverted open-drain NMOS output and open-drain PMOS output

### 5.2.7 Open-Drain PMOS Output

When Attribute bit = 1 and Buffer bit = 0, the pad is in open-drain PMOS output mode. If Direction bit is 0, the pad will be floating. In this condition, the pad functions like floating input. If Direction bit is 1, the pad will be set to "1." Pin bit directly indicates pad status.

### 5.2.8 Dynamic Pull-Low Input

When Attribute bit = 0 and Direction bit = 0, the pad is in dynamic pull-low input mode. If Buffer bit = 0, the pad will be floating. In this case, the pad functions like floating input. If Buffer bit = 1, the pad will be internally pulled low. Pin bit directly indicates pad status.

**Dynamic pull-low input**
A=0, D=0
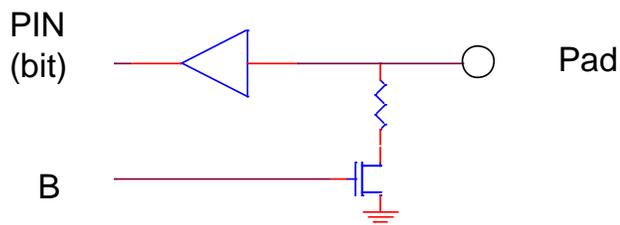
**Dynamic pull-high input**
A=1, D=0
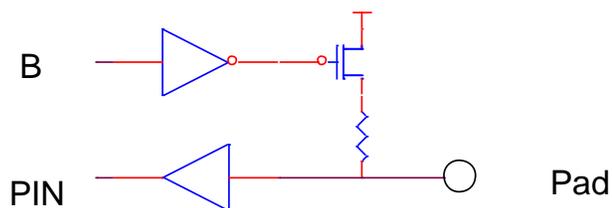
### 5.2.9 Dynamic Pull-High Input

When Attribute bit = 1 and Direction bit = 0, the pad is in dynamic pull-high input mode. If Buffer bit = 0, the pad will be floating. In this case, the pad functions like floating input. If Buffer bit = 1, the pad will be internally pulled high. Pin bit directly indicates status of the pad.

## 5.3 Speedup Groups

Although IO port alone suffices to generate all possible IO status, 3 other speedup groups aid to minimize microcontroller load. Accessing these speedup groups generates specific change of IO status such as OR, AND or XOR with some data in output mode.

## 5.4 Wakeup

In addition to 4 SPI pads for communication between master and slave, one specific W55P241 pad, WAKEUP, is able to wake up the microcontroller. By controlling WAKEN, KC0EN, KC1EN and KC2EN bits, the status change of any W55P241 I/O pad can wake up the microcontroller. Note that the

wakeup-enabled I/O pad must be in "input floating," "input pull high" or "input pull low" state. The supported wakeup modes are listed in the following table.

| WAKEN | KCnEN | ATTRIBUTE | DIRECTION | BUFFER | IO status | Wakeup |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | Floating(default) | |
| | | 0 | 0 | 1 | Pull low | |
| | | 0 | 1 | 0 | Output low | |
| | | 0 | 1 | 1 | Output high | |
| | | 1 | 0 | 0 | Floating | |
| | | 1 | 0 | 1 | Pull high | |
| | | 1 | 1 | 0 | Output high | |
| | | 1 | 1 | 1 | Output low | |
| | 1 | 0 | 0 | 0 | Floating | |
| | | 0 | 0 | 1 | Pull low | |
| | | 0 | 1 | 0 | Output low | |
| | | 0 | 1 | 1 | Output high | |
| | | 1 | 0 | 0 | Floating | |
| | | 1 | 0 | 1 | Pull high | |
| | | 1 | 1 | 0 | Output high | |
| | | 1 | 1 | 1 | Output low | |
| 1 | 0 | 0 | 0 | 0 | Floating | |
| | | 0 | 0 | 1 | Pull low | |
| | | 0 | 1 | 0 | Output low | |
| | | 0 | 1 | 1 | Output high | |
| | | 1 | 0 | 0 | Floating | |
| | | 1 | 0 | 1 | Pull high | |
| | | 1 | 1 | 0 | Output high | |
| | | 1 | 1 | 1 | Output low | |
| | 1 | 0 | 0 | 0 | Floating | Supported |
| | | 0 | 0 | 1 | Pull low | Supported |
| | | 0 | 1 | 0 | Output low | |
| | | 0 | 1 | 1 | Output high | |
| | | 1 | 0 | 0 | Floating | |
| | | 1 | 0 | 1 | Pull high | Supported |
| | | 1 | 1 | 0 | Output high | |
| | | 1 | 1 | 1 | Output low | |

Table 3 Supported wakeup mode

There are 2 ways to wake up the host (e.g. microcontroller). In way 1, DO suffices to wake up the

host and no dedicated WAKEUP pad is needed. By reading from WKCTL ($0F), the last data bit (bit0) is forced to "0" until the wakeup conditions match. After wakeup conditions match (any input pad with change of status), the rising edge on DI pad can wake up the host. Users can read data from WKCTL ($0F) to find the cause of wakeup port and then check BP0P ($0C), BP1P ($0D) or BP2P ($0E) for the dedicated pad. Note that after wakeup conditions match, the WAKEN bit (KC0EN, KC1EN and KC2EN bits are not affected) is automatically set to "0." WAKEN bit must be enabled again if wakeup is to be used later. Reading BP0P sets the P0C bit to "0." Reading BP1P sets the P1C bit to "0." Reading BP2P sets the P2C bit to "0." Only when P0C, P1C and P2C bits are all "0"s is the WKFLG bit set to "0."
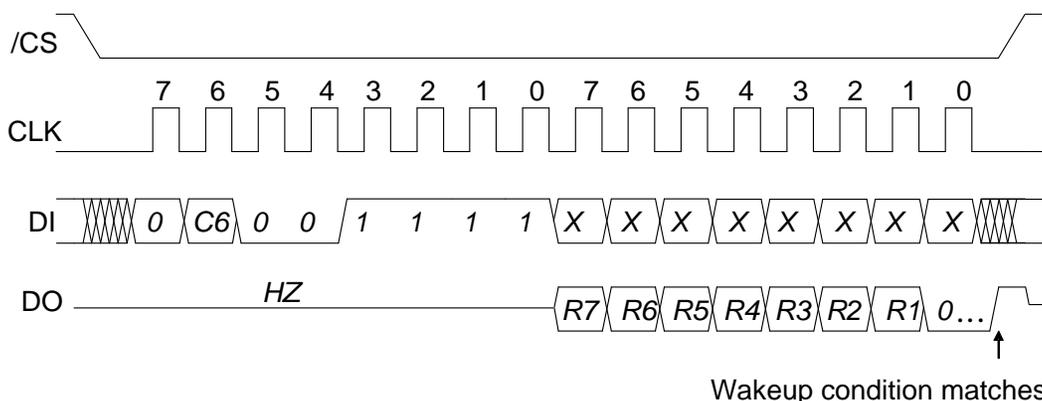


*Cn*: command bit. *Rn*: read data bit.
*HZ*: high impedance. *X* : don't care. *7 -> 0*: MSB -> LSB.

Figure 8 Wakeup method 1

In way 2, a dedicated WAKEUP pad (instead of the DO pad) wakes up the host. The WAKEUP pad keeps floating until wakeup conditions match. After wakeup conditions match, the WAKEUP pad is forced to "0." When the WKFLG bit is set to "0," the WAKEUP pad is not forced to "0" and remains floating until wakeup conditions match again. Because the WAKEUP pad is not pulled by any internal resistor, the host or the system board must have a pull-high resistor for wakeup to work smoothly.

## 5.5  256-Level Output

The W55P241 provides 8 256-level output controls in BP00~BP07 respectively. A dedicated counter is in charge of the 256-level output function. It is also used in motor control. The internal ring oscillator runs @ 8MHz and one PWM period consists of 256 PWM clocks whose frequencies are derived by dividing the original ring oscillator clock by 16, 64, 256 or 512. The basic PWM period can be selected by PWMCK. BP03, BP02, BP01 and BP00 have one identical PWM period while BP07, BP06, BP05 and BP04 may have another identical PWM period. Because the default statuses of BP0[7:0] are general

IO pads, PWMEN enables both internal ring oscillator and PWM output. Any bit of PWMEN can enable the internal ring oscillator. In addition to PWMEN, the corresponding BP0D bit must be set to 1 to generate PWM output. The duty ratio is determined by PWMn, where n = 0~7. When PWMn is larger than or equal to the internal counter, the PWM output will be "1" if the corresponding BP0A and BP0B bits are not equal. Therefore, PWM output must keep "1" for at least one PWM clock. The PWM output will be made inverse if the corresponding BP0A and BP0B bits are equal. Note that except for power-on reset, the internal PWM counter may not count from zero once it is enabled. Software reset initializes the status of I/O (input, floating), not the PWM counter's status. Note that in software reset, bit6 of command byte must be 1 whatever the DIS pad status.

*When the corresponding bits of BP0B and BP0A are not equal*

| Counter | 255 | 0 | 1 | …............ | 126 | 127 | 128 | …............ | 254 | 255 | 0 |

(1)
Comparator = 0

Output

(2)
Comparator = 127

Output

(3)
Comparator = 255

Output

"1"

"0"
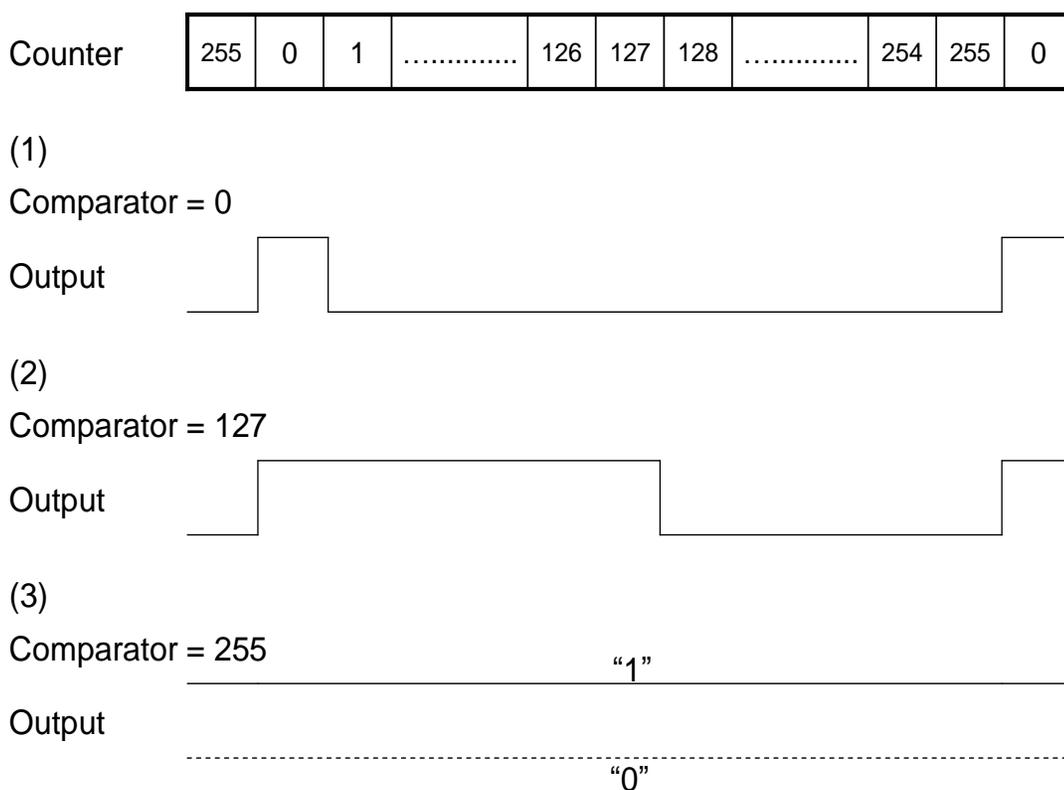
Figure 9 Normal PWM output (B0x bit is not equal to A0x bit)

**W55P241**

*When the corresponding bits of BP0B and BP0A are equal*



| Counter | 255 | 0 | 1 | ….......... | 126 | 127 | 128 | ….......... | 254 | 255 | 0 |

(1)
Comparator = 0

Output

(2)
Comparator = 127

Output

(3)
Comparator = 255
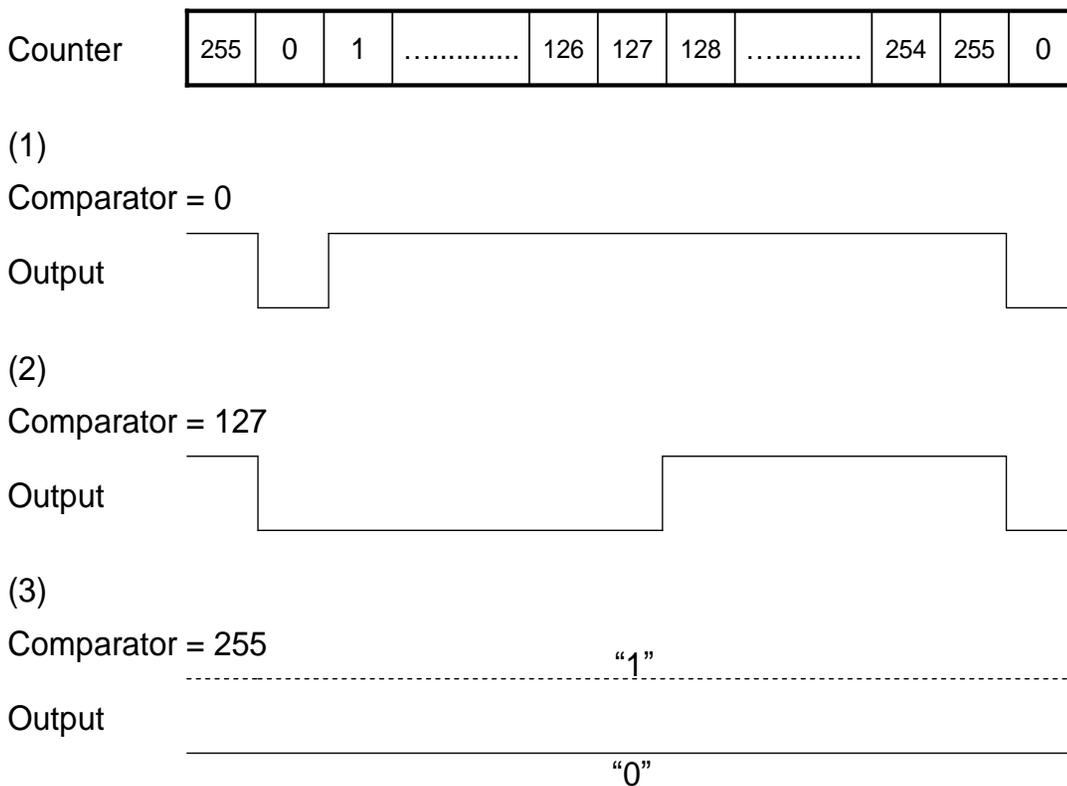
Output

Figure 10 Inverted PWM output (B0x bit is equal to A0x bit)

For the chip to enter standby mode, all PWM channels have to be disabled in addition to keeping /CS "1".

## 6. CONTROL AND STATUS REGISTERS

SFRs (Special Function Registers) are basically divided into 4 groups. Note that "$" stands for hexadecimal format.

### 6.1 I/O port

I/O port SFRs control I/O status.

| Address | Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Attribute | Default |
|---------|----------|-----|-----|-----|-----|-----|-----|-----|-----|-----------|-----------|
| $00 | BP0B | B07 | B06 | B05 | B04 | B03 | B02 | B01 | B00 | R/W | 0000_0000 |
| $01 | BP1B | B17 | B16 | B15 | B14 | B13 | B12 | B11 | B10 | R/W | 0000_0000 |

| $02 | BP2B | B27 | B26 | B25 | B24 | B23 | B22 | B21 | B20 | R/W | 0000_0000 |
|------|------|------|------|------|------|------|------|------|------|------|------|
| $03 | | | | | | | | | | | |
| $04 | BP0D | D07 | D06 | D05 | D04 | D03 | D02 | D01 | D00 | R/W | 0000_0000 |
| $05 | BP1D | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | R/W | 0000_0000 |
| $06 | BP2D | D27 | D26 | D25 | D24 | D23 | D22 | D21 | D20 | R/W | 0000_0000 |
| $07 | | | | | | | | | | | |
| $08 | BP0A | A07 | A06 | A05 | A04 | A03 | A02 | A01 | A00 | R/W | 0000_0000 |
| $09 | BP1A | A17 | A16 | A15 | A14 | A13 | A12 | A11 | A10 | R/W | 0000_0000 |
| $0A | BP2A | A27 | A26 | A25 | A24 | A23 | A22 | A21 | A20 | R/W | 0000_0000 |
| $0B | | | | | | | | | | | |
| $0C | BP0P | P07 | P06 | P05 | P04 | P03 | P02 | P01 | P00 | R/W | 0000_0000 |
| $0D | BP1P | P17 | P16 | P15 | P14 | P13 | P12 | P11 | P10 | R/W | 0000_0000 |
| $0E | BP2P | P27 | P26 | P25 | P24 | P23 | P22 | P21 | P20 | R/W | 0000_0000 |
| $0F | WKCTL | WAKEN | KC0EN | KC1EN | KC2EN | P0C | P1C | P2C | WKFLG | R | 0000_0000 |
| $0F | WKCTL | WAKEN | KC0EN | KC1EN | KC2EN | | | | | W | |

| | |
|------|------|
| **B0n** | BUFFER data of BP0: n = 0(LSB) ~ 7(MSB). |
| **B1n** | BUFFER data of BP1 |
| **B2n** | BUFFER data of BP2 |
| **D0n** | DIRECTION data of BP0 |
| **D1n** | DIRECTION data of BP1 |
| **D2n** | DIRECTION data of BP2 |
| **A0n** | ATTRIBUTE data of BP0 |
| **A1n** | ATTRIBUTE data of BP1 |
| **A2n** | ATTRIBUTE data of BP2 |
| **P0n** | PIN data of BP0 |
| **P1n** | PIN data of BP1 |
| **P2n** | PIN data of BP2. |
| **WAKEN** | Wakeup enabling bit. It is set to 0 when wakeup matches. 1: enable. 0: disable. |
| **KC0EN** | Wakeup enabling bit of BP0. 1: enable. 0: disable. |
| **KC1EN** | Wakeup enabling bit of BP1. 1: enable. 0: disable. |
| **KC2EN** | Wakeup enabling bit of BP2. 1: enable. 0: disable. |
| **P0C** | Change bit of BP0. It is set to 0 after reading BP0P. 1: change. 0: no change. |
| **P1C** | Change bit of BP1. It is set to 0 after reading BP1P. 1: change. 0: no change. |
| **P2C** | Change bit of BP2. It is set to 0 after reading BP2P. 1: change. 0: no change. |
| **WKFLG** | ORing of P0C, P1C and P2C bits. 1: WAKEUP pad is forced low. 0: floating. |

## 6.2  AND

AND group SFRs speed up AND operation of BUFFER, DIRECTION or ATTRIBUTE bit. BPmB = BPmB AND NBPmB. BMmD = BPmD AND NBPmD. BPmA = BPmA AND NBPmA. m = 0, 1, 2.

| Address | Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Attribute | Default |
|---------|----------|------|------|------|------|------|------|------|------|-----------|---------|
| $10 | NBP0B | NB07 | NB06 | NB05 | NB04 | NB03 | NB02 | NB01 | NB00 | W | |
| $11 | NBP1B | NB17 | NB16 | NB15 | NB14 | NB13 | NB12 | NB11 | NB10 | W | |
| $12 | NBP2B | NB27 | NB26 | NB25 | NB24 | NB23 | NB22 | NB21 | NB20 | W | |
| $13 | | | | | | | | | | | |
| $14 | NBP0D | ND07 | ND06 | ND05 | ND04 | ND03 | ND02 | ND01 | ND00 | W | |
| $15 | NBP1D | ND17 | ND16 | ND15 | ND14 | ND13 | ND12 | ND11 | ND10 | W | |
| $16 | NBP2D | ND27 | ND26 | ND25 | ND24 | ND23 | ND22 | ND21 | ND20 | W | |
| $17 | | | | | | | | | | | |
| $18 | NBP0A | NA07 | NA06 | NA05 | NA04 | NA03 | NA02 | NA01 | NA00 | W | |
| $19 | NBP1A | NA17 | NA16 | NA15 | NA14 | NA13 | NA12 | NA11 | NA10 | W | |
| $1A | NBP2A | NA27 | NA26 | NA25 | NA24 | NA23 | NA22 | NA21 | NA20 | W | |
| $1B | | | | | | | | | | | |
| $1C | PWM0 | P0D7 | P0D6 | P0D5 | P0D4 | P0D3 | P0D2 | P0D1 | P0D0 | W | |
| $1D | PWM1 | P1D7 | P1D6 | P1D5 | P1D4 | P1D3 | P1D2 | P1D1 | P1D0 | W | |
| $1E | PWM2 | P2D7 | P2D6 | P2D5 | P2D4 | P2D3 | P2D2 | P2D1 | P2D0 | W | |
| &1F | PWM3 | P3D7 | P3D6 | P3D5 | P3D4 | P3D3 | P3D2 | P3D1 | P3D0 | W | |

| | |
|------|------|
| **NB0n** | AND data of BP0B: n = 0(LSB) ~ 7(MSB) |
| **NB1n** | AND data of BP1B |
| **NB2n** | AND data of BP2B |
| **ND0n** | AND data of BP0D |
| **ND1n** | AND data of BP1D |
| **ND2n** | AND data of BP2D |
| **NA0n** | AND data of BP0A |
| **NA1n** | AND data of BP1A |
| **NA2n** | AND data of BP2A |
| **PmDn** | PWM channel m data[n]: m = 0 ~ 3. n = 0(LSB) ~ 7(MSB). |

## 6.3 OR

OR group SFRs speed up OR operation of BUFFER, DIRECTION or ATTRIBUTE bit. BPmB = BPmB OR OBPmB. BPmD = BPmD OR OBPmD. BPmA = BPmA OR OBPmA. m = 0, 1, 2.

| Address | Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Attribute | Default |
|---------|----------|------|------|------|------|------|------|------|------|-----------|---------|
| $20 | OBP0B | OB07 | OB06 | OB05 | OB04 | OB03 | OB02 | OB01 | OB00 | W | |
| $21 | OBP1B | OB17 | OB16 | OB15 | OB14 | OB13 | OB12 | OB11 | OB10 | W | |
| $22 | OBP2B | OB27 | OB26 | OB25 | OB24 | OB23 | OB22 | OB21 | OB20 | W | |
| $23 | | | | | | | | | | | |
| $24 | OBP0D | OD07 | OD06 | OD05 | OD04 | OD03 | OD02 | OD01 | OD00 | W | |
| $25 | OBP1D | OD17 | OD16 | OD15 | OD14 | OD13 | OD12 | OD11 | OD10 | W | |
| $26 | OBP2D | OD27 | OD26 | OD25 | OD24 | OD23 | OD22 | OD21 | OD20 | W | |
| $27 | | | | | | | | | | | |
| $28 | OBP0A | OA07 | OA06 | OA05 | OA04 | OA03 | OA02 | OA01 | OA00 | W | |
| $29 | OBP1A | OA17 | OA16 | OA15 | OA14 | OA13 | OA12 | OA11 | OA10 | W | |
| $2A | OBP2A | OA27 | OA26 | OA25 | OA24 | OA23 | OA22 | OA21 | OA20 | W | |
| $2B | | | | | | | | | | | |
| $2C | PWM4 | P4D7 | P4D6 | P4D5 | P4D4 | P4D3 | P4D2 | P4D1 | P4D0 | W | |
| $2D | PWM5 | P5D7 | P5D6 | P5D5 | P5D4 | P5D3 | P5D2 | P5D1 | P5D0 | W | |
| $2E | PWM6 | P6D7 | P6D6 | P6D5 | P6D4 | P6D3 | P6D2 | P6D1 | P6D0 | W | |
| &2F | PWM7 | P7D7 | P7D6 | P7D5 | P7D4 | P7D3 | P7D2 | P7D1 | P7D0 | W | |

| | |
|---|---|
| **OB0n** | OR data of BP0B: n = 0(LSB) ~ 7(MSB) |
| **OB1n** | OR data of BP1B |
| **OB2n** | OR data of BP2B |
| **OD0n** | OR data of BP0D |
| **OD1n** | OR data of BP1D |
| **OD2n** | OR data of BP2D |
| **OA0n** | OR data of BP0A |
| **OA1n** | OR data of BP1A |
| **OA2n** | OR data of BP2A |
| **PmDn** | PWM channel m data[n]: m = 4 ~ 7. n = 0(LSB) ~ 7(MSB). |

## 6.4  XOR

XOR group SFRs speed up XOR operation of BUFFER, DIRECTION or ATTRIBUTE bit. BPmB = BPmB XOR XBPmB. BPmD = BPmD XOR XBPmD. BPmA = BPmA XOR XBPmA. m = 0, 1, 2.

| Address | Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Attribute | Default |
|---------|----------|---|---|---|---|---|---|---|---|-----------|---------|
| $30 | XBP0B | XB07 | XB06 | XB05 | XB04 | XB03 | XB02 | XB01 | XB00 | W | |
| $31 | XBP1B | XB17 | XB16 | XB15 | XB14 | XB13 | XB12 | XB11 | XB10 | W | |
| $32 | XBP2B | XB27 | XB26 | XB25 | XB24 | XB23 | XB22 | XB21 | XB20 | W | |
| $33 | | | | | | | | | | | |
| $34 | XBP0D | XD07 | XD06 | XD05 | XD04 | XD03 | XD02 | XD01 | XD00 | W | |
| $35 | XBP1D | XD17 | XD16 | XD15 | XD14 | XD13 | XD12 | XD11 | XD10 | W | |
| $36 | XBP2D | XD27 | XD26 | XD25 | XD24 | XD23 | XD22 | XD21 | XD20 | W | |
| $37 | | | | | | | | | | | |
| $38 | XBP0A | XA07 | XA06 | XA05 | XA04 | XA03 | XA02 | XA01 | XA00 | W | |
| $39 | XBP1A | XA17 | XA16 | XA15 | XA14 | XA13 | XA12 | XA11 | XA10 | W | |
| $3A | XBP2A | XA27 | XA26 | XA25 | XA24 | XA23 | XA22 | XA21 | XA20 | W | |
| $3B | | | | | | | | | | | |
| $3C | PWMEN | EN7 | EN6 | EN5 | EN4 | EN3 | EN2 | EN1 | EN0 | R/W | |
| $3D | PWMCK | TEST | X | X | X | MOD3 | MOD2 | MOD1 | MOD0 | R/W | |
| $3E | | | | | | | | | | | |
| &3F | RESET | X | X | X | X | X | X | X | X | W | |

| | |
|---|---|
| **XB0n** | XOR data of BP0B: n = 0(LSB) ~ 7(MSB) |
| **XB1n** | XOR data of BP1B |
| **XB2n** | XOR data of BP2B |
| **XD0n** | XOR data of BP0D |
| **XD1n** | XOR data of BP1D |
| **XD2n** | XOR data of BP2D |
| **XA0n** | XOR data of BP0A |
| **XA1n** | XOR data of BP1A |
| **XA2n** | XOR data of BP2A |
| **ENn** | 1: enables PWM channel. 0: disable. n = 0 ~ 7. |
| **MOD[1:0]** | 00: BP0[3:0] clock is derived by dividing 8MHz clock by 16. |
| | 01: BP0[3:0] clock is derived by dividing 8MHz clock by 64. |
| | 10: BP0[3:0] clock is derived by dividing 8MHz clock by 256. |
| | 11: BP0[3:0] clock is derived by dividing 8MHz clock by 512. |
| **MOD[3:2]** | 00: BP0[7:4] clock is derived by dividing 8MHz clock by 16. |

01: BP0[7:4] clock is derived by dividing 8MHz clock by 64.

10: BP0[7:4] clock is derived by dividing 8MHz clock by 256.

11: BP0[7:4] clock is derived by dividing 8MHz clock by 512.

## 7. ELECTRICAL CHARACTERISTICS

### 7.1 Absolute maximum ratings

| PARAMETER | SYMBOL | CONDITIONS | RATED VALUE | UNIT |
|---|---|---|---|---|
| Power Supply | $V_{DD}$–$V_{SS}$ | - | -0.3 to +7.0 | V |
| Input Voltage | $V_{IN}$ | All Inputs | $V_{SS}$ -0.3 to $V_{DD}$ +0.3 | V |
| Storage Temp. | $T_{STG}$ | - | -55 to +150 | °C |
| Operating Temp. | $T_{OPR}$ | - | 0 to +70 | °C |

Note: Exposure to conditions beyond those listed under the Absolute Maximum Ratings table may adversely affect the life and reliability of the device.

### 7.2 DC Characteristics

($V_{DD}$ – $V_{SS}$ = 4.5V, $T_A$ = 25° C, No Load unless otherwise specified)

| PARAMETER | SYM. | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| Operating voltage | $V_{DD}$ | | 2.2 | - | 5.5 | V |
| Operating current | $I_{OP1}$ | $V_{DD}$=5.5V, CLK @10MHz | - | | 800 | uA |
| Standby current (STOP) | $I_{DD1}$ | $V_{DD}$=5.5V, /CS=$V_{DD}$ | - | 1 | 2 | $\mu A$ |
| Input low voltage | $V_{IL}$ | All Input Pins | $V_{SS}$ | - | 0.3 $V_{DD}$ | V |
| Input high voltage | $V_{IH}$ | All Input Pins | 0.7 $V_{DD}$ | - | $V_{DD}$ | V |
| Input pull-high resistor | $I_{IN1}$ | VDD=3.0V | 360 | 450 | 540 | $K\Omega$ |
| Input pull-low resistor | $I_{IN2}$ | VDD=3.0V | 360 | 450 | 540 | $K\Omega$ |
| Output current | $I_{OL}$ | $V_{DD}$ = 3V, $V_{OUT}$ = 0.4V | 8 | 12 | - | mA |
| | $I_{OH}$ | $V_{DD}$ = 3V, $V_{OUT}$ = 2.6V | -4 | -6 | - | mA |
| | $I_{OL}$ | $V_{DD}$ = 4.5V, $V_{OUT}$ = 1.0V | - | 25 | - | mA |
| | $I_{OH}$ | $V_{DD}$ = 4.5V, $V_{OUT}$ = 2.6V | - | -12 | - | mA |

### 7.3 AC Characteristics

($V_{DD}$ – $V_{SS}$ = 3.0V, $T_A$ = 25°C ; unless otherwise specified)

| PARAMETER | SYM. | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| CLK Clock frequency | $f_{CLK}$ | | - | - | 10 | MHz |
| Input rise time | $t_R$ | | - | - | 5 | nS |
| Input fall time | $t_F$ | | - | - | 5 | nS |
| CLK high time | $t_{WH}$ | | 45 | - | - | nS |
| CLK low time | $t_{WL}$ | | 45 | - | - | nS |
| /CS high time | $t_{CS}$ | | 100 | - | - | nS |
| /CS setup time | $t_{CSS}$ | | 50 | - | - | nS |
| /CS hold time | $t_{CSH}$ | | 50 | - | - | nS |
| Data in setup time | $t_{SU}$ | | 5 | - | - | nS |

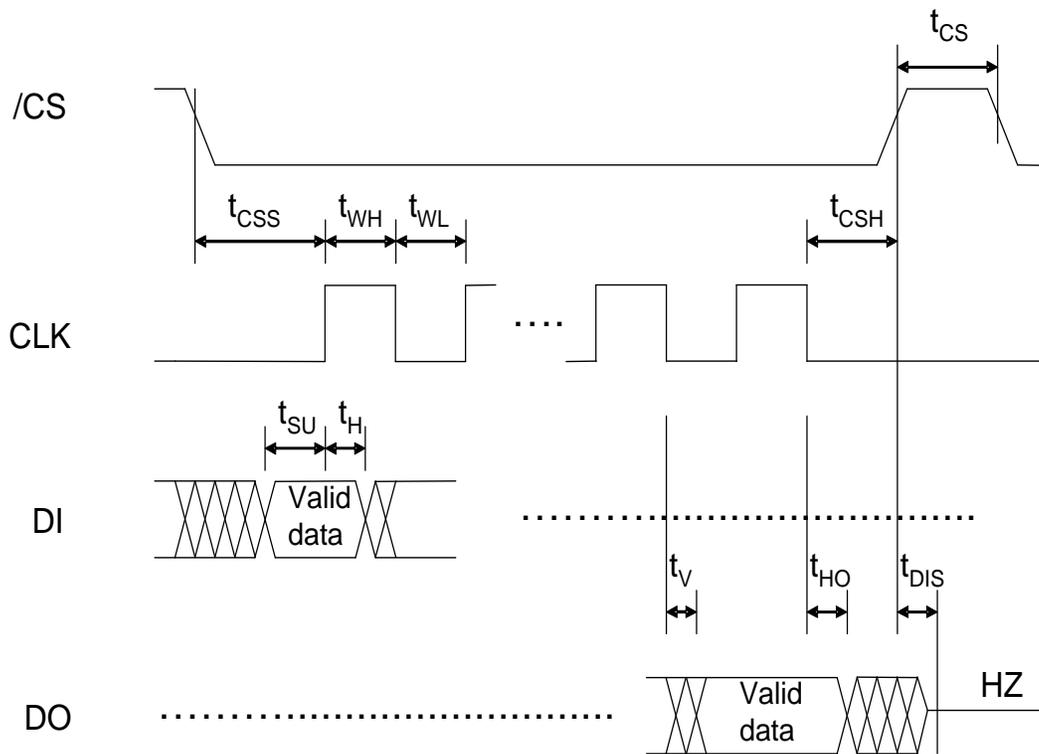| Data in hold time | $t_H$ | | 5 | - | - | nS |
|---|---|---|---|---|---|---|
| Output valid time | $t_V$ | | - | - | 45 | nS |
| Output hold time | $t_{HO}$ | | 0 | - | - | nS |
| Output disable time | $t_{DIS}$ | | - | - | 100 | nS |

Figure 11 SPI Timing

## 8. TYPICAL APPLICATION CIRCUIT
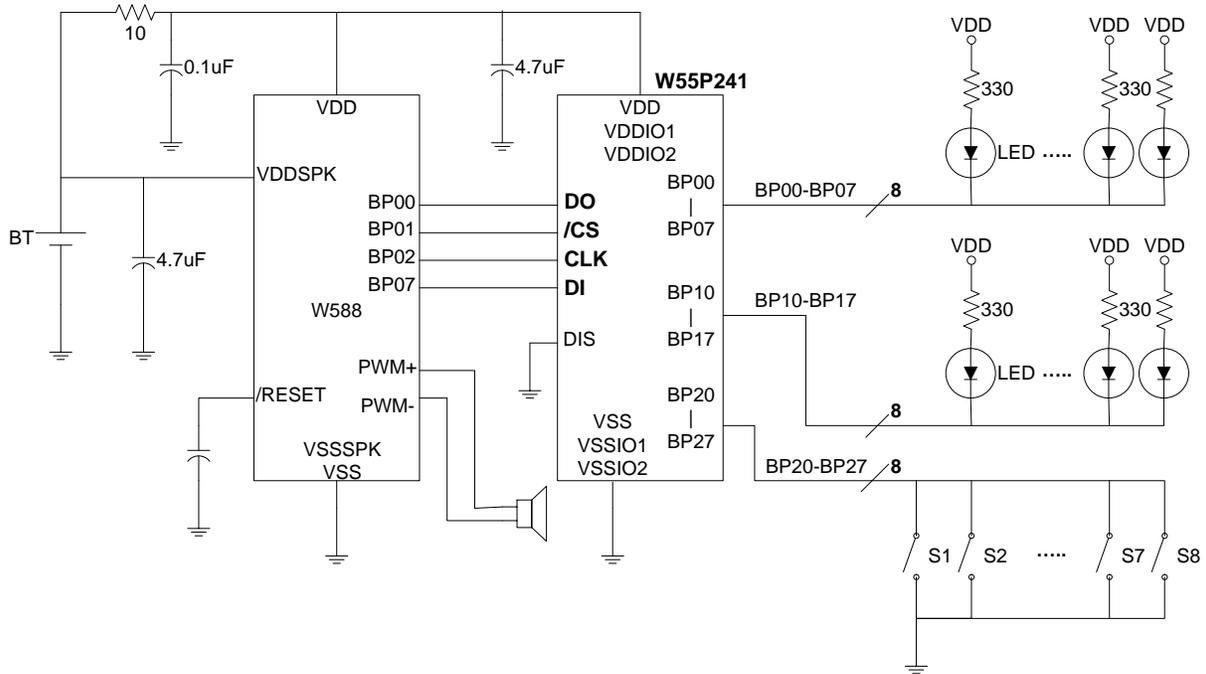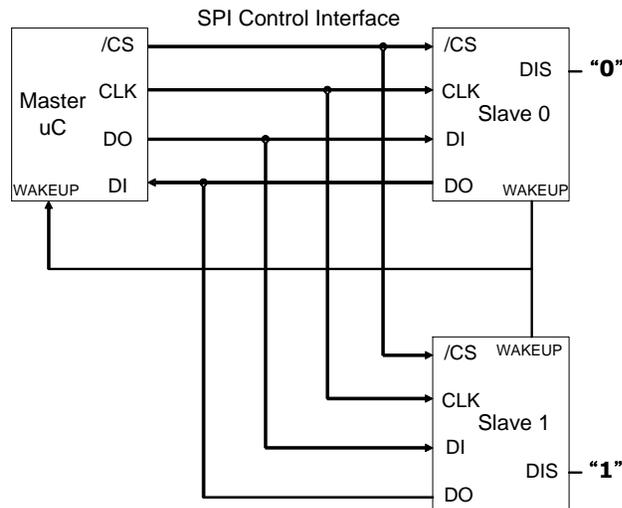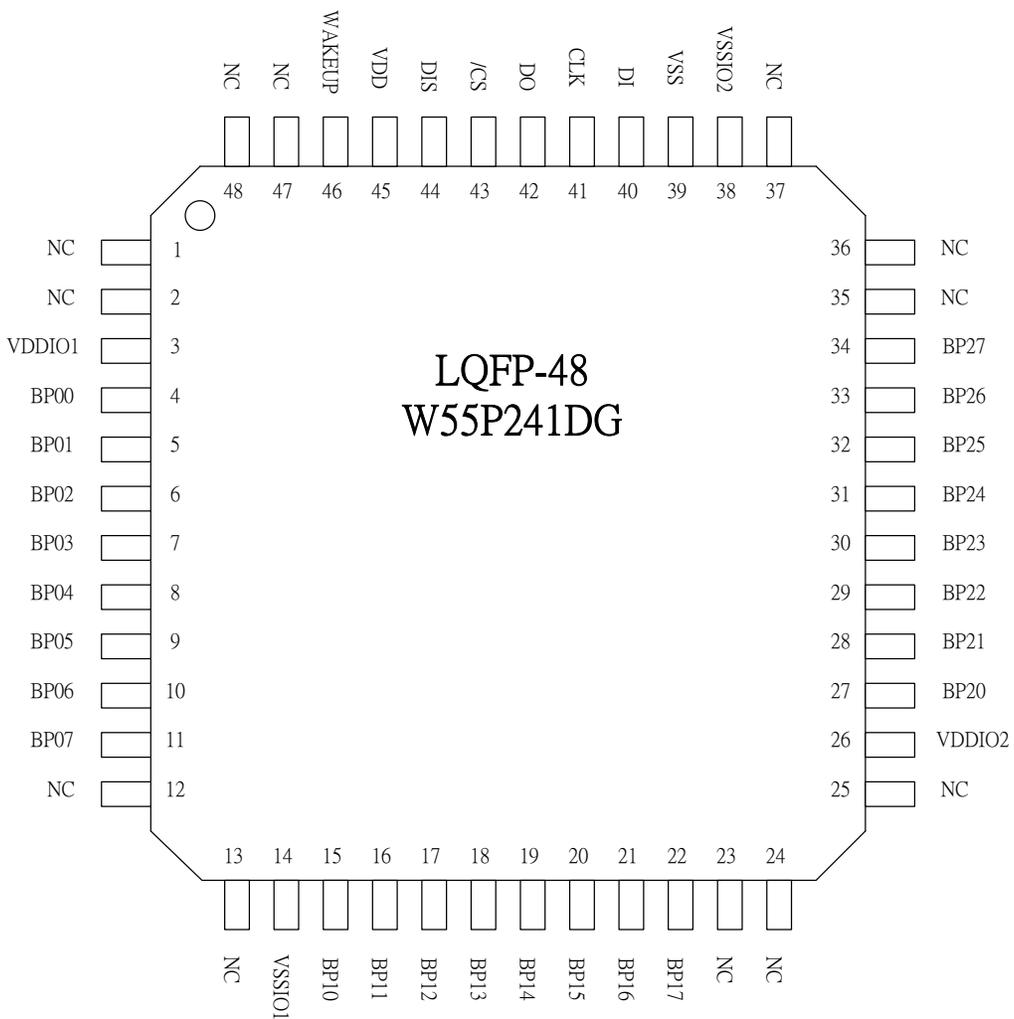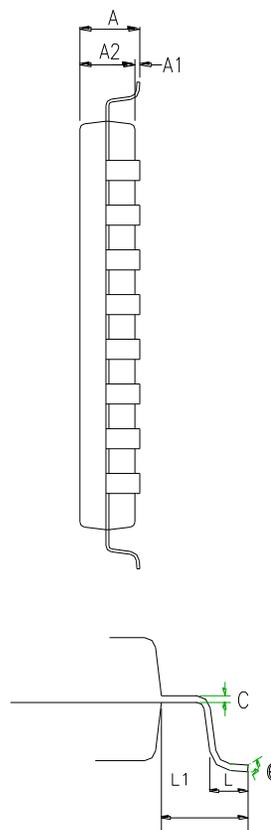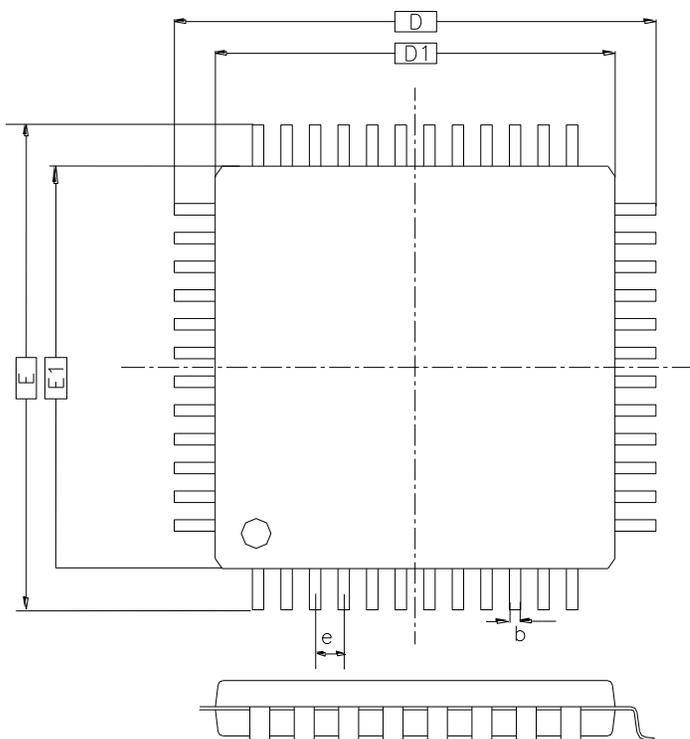


Figure 12 Application circuit



Figure 13 Connection of Master and Slave

## 9. PACKAGE INFORMATION

### LQFP48 Pin assignment



LQFP-48
W55P241DG

Top pins (left to right, 48–37): NC, NC, WAKEUP, VDD, DIS, /CS, DO, CLK, DI, VSS, VSSIO2, NC

Left pins (top to bottom, 1–12): NC, NC, VDDIO1, BP00, BP01, BP02, BP03, BP04, BP05, BP06, BP07, NC

Right pins (top to bottom, 36–25): NC, NC, BP27, BP26, BP25, BP24, BP23, BP22, BP21, BP20, VDDIO2, NC

Bottom pins (left to right, 13–24): NC, VSSIO1, BP10, BP11, BP12, BP13, BP14, BP15, BP16, BP17, NC, NC

## LQFP48 Package dimension



COTROL DIMENSIONS ARE IN MILLIMETERS.

| SYMBOL | MILLIMETER | | | INCH | | |
|---|---|---|---|---|---|---|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | — | — | 1.60 | — | — | 0.063 |
| A1 | 0.05 | 0.10 | 0.15 | 0.002 | 0.004 | 0.006 |
| A2 | 1.35 | 1.40 | 1.45 | 0.053 | 0.055 | 0.057 |
| D1 | 6.90 | 7.00 | 7.10 | 0.272 | 0.276 | 0.260 |
| E1 | 6.90 | 7.00 | 7.10 | 0.272 | 0.276 | 0.260 |
| e | 0.35 | 0.50 | 0.65 | 0.014 | 0.020 | 0.260 |
| D | 8.9 | 9.00 | 9.10 | 0.350 | 0.354 | 0.358 |
| E | 8.9 | 9.00 | 9.10 | 0.350 | 0.354 | 0.358 |
| L | 0.45 | 0.60 | 0.75 | 0.018 | 0.024 | 0.030 |
| L1 | — | 1.00 | — | — | 0.039 | — |
| C | 0.09 | — | 0.20 | 0.0035 | — | 0.0079 |
| θ | 0° | — | 7° | 0° | — | 7° |
| b | 0.17 | 0.22 | 0.27 | 0.007 | 0.0087 | 0.011 |

**QFN32 Pin assignment**
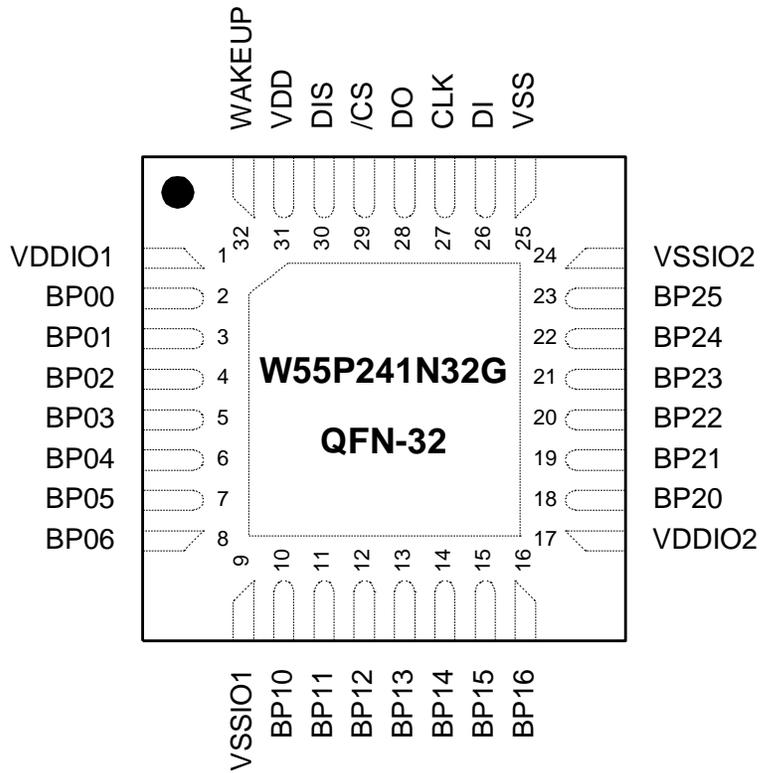


Note: No support BP07, BP17, BP26 and BP27

**QFN32 Package dimension**
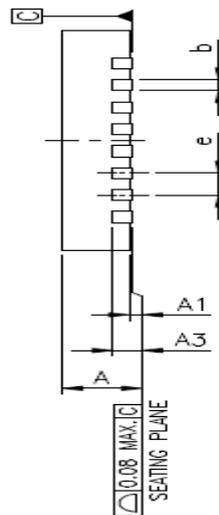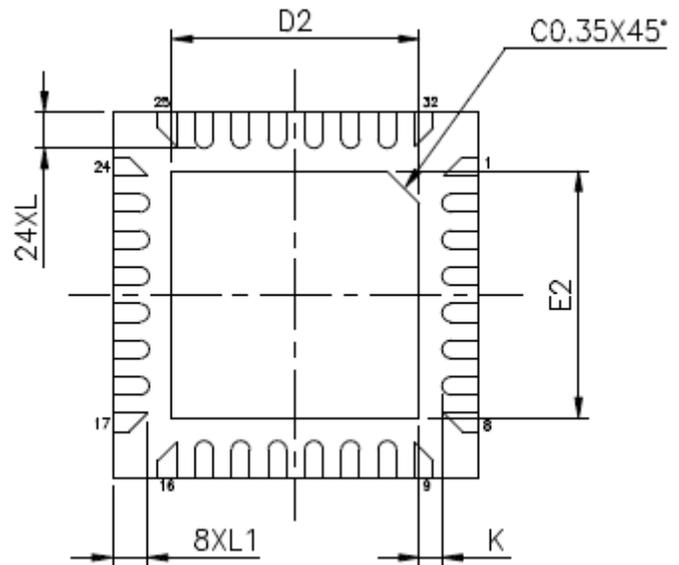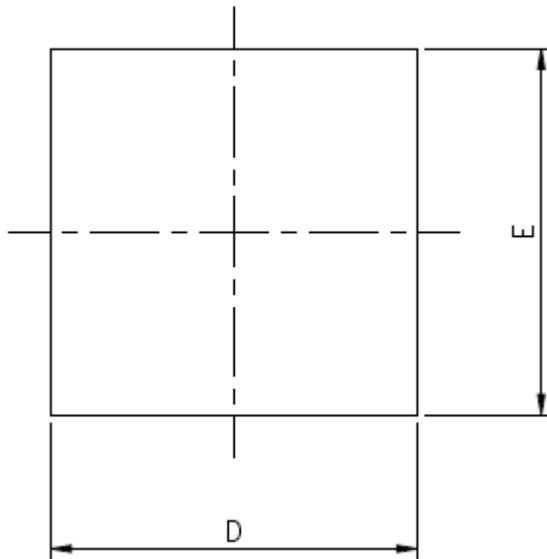


| | Symbol | Min | Nom | Max |
|---|---|---|---|---|
| Total Thickness | A | 0.7 | 0.75 | 0.8 |
| Stand Off | A1 | 0.0 | 0.02 | 0.05 |
| L/F Thickness | A3 | | 0.2 REF. | |
| Lead Width | b | 0.15 | 0.20 | 0.25 |
| Body Size | D | | 4.00 BSC | |
| | E | | 4.00 BSC | |
| Lead Pitch | e | | 0.40 BSC | |
| Lead Length | L | 0.35 | 0.4 | 0.45 |
| | K | 0.2 | -- | -- |

| Symbol | L/F SIZE | Dimension in mm | | |
|---|---|---|---|---|
| | | MIN. | NOR. | MAX. |
| D2 | 114X114 mm | 2.6 | 2.7 | 2.75 |
| E2 | | 2.6 | 2.7 | 2.75 |

**10. DEMO BOARD**



| PIN NAME | PIN Number | PIN NAME | PIN Number |
|----------|-----------|----------|-----------|
| /CS | 2 | BP14 | 22 |
| DIS | 3 | BP15 | 23 |
| VDD | 4 | BP16 | 24 |
| WAKEUP | 5 | BP17 | 25 |
| VDDIO1 | 6 | VDDIO2 | 26 |
| BP00 | 7 | BP20 | 27 |
| BP01 | 8 | BP21 | 28 |
| BP02 | 9 | BP22 | 29 |
| BP03 | 10 | BP23 | 30 |
| BP04 | 11 | BP24 | 31 |
| BP05 | 12 | BP25 | 32 |
| BP06 | 13 | BP26 | 33 |
| BP07 | 14 | BP27 | 34 |
| VSSIO1 | 15 | VSSIO2 | 35 |
| BP10 | 16 | VSS | 36 |
| BP11 | 17 | DI | 37 |
| BP12 | 18 | CLK | 38 |
| BP13 | 19 | DO | 39 |

## 11. ORDERING INFORMATION

    A.  Dies: W55P241

    B.  Package of LQFP48: W55P241DG

    C.  Package of QFN32: W55P241N32G

## 12. REVISION HISTORY

| REVISION | DATE | MODIFICATIONS | |
|---|---|---|---|
| A1.0 | Feb.  2008 | ➢ | Preliminary release. |
| A1.1 | May 2008 | ➢ | Change part # from W55IO241 to W55P241 |
| | | ➢ | Add Section 5 Function Description |
| | | ➢ | Add Section 6 Control and Status Registers |
| | | ➢ | Add application circuit |
| A2.0 | Aug. 2008 | ➢ | Add Section 9 Demo board Pin List |
| | | ➢ | Add Figure13 |
| A3.0 | Oct. 2008 | ➢ | Remove Section 9 Demo Board Pin List |
| | | ➢ | Add Section 9 LQFP Package Information |
| | | ➢ | Add Section 11 Ordering Information |
| | | ➢ | Change port name to BP0 ~ BP2 |
| A4.0 | Nov. 2008 | ➢ | Fix grammar |
| A5.0 | Apr. 2009 | ➢ | Add Section 10 Demo Board Information |
| A6.0 | May 2009 | ➢ | Fix Package information |
| A7.0 | Nov. 2012 | ➢ | Add QFN32 package information |

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