## 1. GENERAL DESCRIPTION

The N551C161 is an 16-Mbit Mask ROM with interface with Nuvoton PowerSpeech, BandDirector and ViewTalk series products to extend the memory size for long duration applications.

2. FEATURES

➢ Wide range of operation voltage: 2.4 ~ 5.5V @ normal read mode
➢ ROM size: 16-Mbit
➢ SPI ROM interface
➢ Normal read access time: 500 nS
➢ Operating current: 2.5mA (max.)
➢ Available package form:
   ■ COB is essential

3. BLOCK DIAGRAM
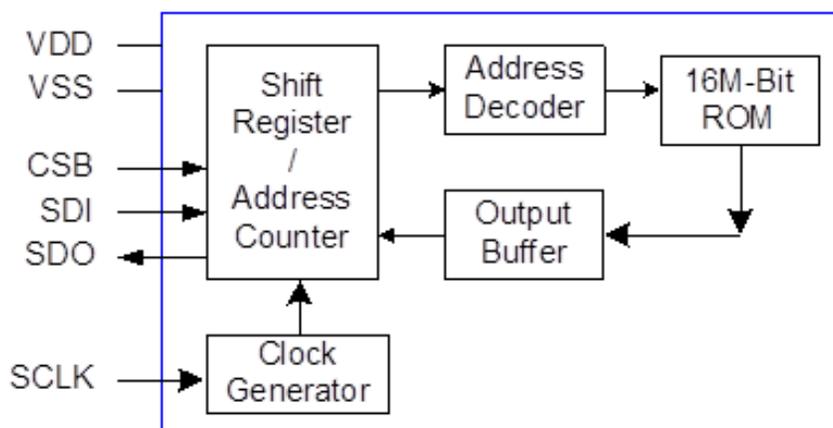
4. PIN DESCRIPTION

SYMBOL	I/O	FUNCTION
SDI	I	Command/address input
SDO	O	Data output
SCLK	I	Clock input
CSB	I	Chip select input, low active. When CSB is High, chip is in standby mode and SDO pin is at high impedance
VSS	I	Microcontroller Negative power supply (-).
VDD	I	Microcontroller Positive power supply (+).

5. ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	CONDITIONS	RATED VALUE	UNIT
Power Supply	$V_{DD} - V_{SS}$	-	-0.3 ~ +7.0	V
Input Voltage	V_{IN}	All Inputs	V_{SS}-0.3 ~ V_{DD}+0.3	V
Storage Temp.	T_{STG}	-	-55 ~ +150	°C
Operating Temp.	T_{OPR}	-	0 ~ +70	°C

NOTE: Operating the device under conditions beyond those indicated above may cause permanent damage or affect device reliability

6. ELECTRICAL CHARACTERISTICS

DC Parameters

(VDD–VSS = 4.5V±10%, TA = 25° C; unless otherwise specified)

PARAMETER	SYM.	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Operating voltage	VDD		2.4		5.5	V
Operation current	Iop2	SPI interface mode, data output rate 2MHz			2.5	mA
Standby current	Isb	VDD=5.5V			4	μA
Output high current	Ioh	Vout=4.0V		-5		mA
Output low current	Iol	Vout=0.5V		5		mA
Input Low Voltage	V_{IL}	All input pins	-0.3	-	0.8	V
Input High Voltage	V_{IH}	All input pins	2.0	-	VDD	V

AC Parameters

(VDD−VSS = 4.5V±10%, TA = 25° C; unless otherwise specified)

PARAMETER	SYM.	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Serial clock period	Tsck	Data Read	500			nS
		Fast Data Read	250			nS
Select lead time	Tssb		100			nS
Data input setup time	Tsui		20			nS
Data input hold time	Thdi		20			nS
Data output valid time	Tvdo				85	nS

SPI Mode Interface
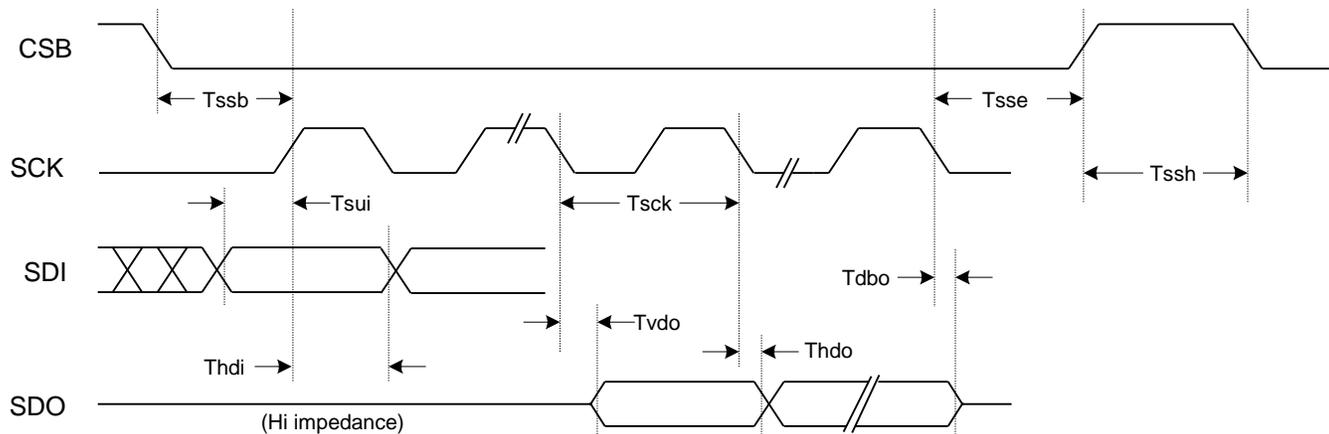
7. APPLICATION CIRCUIT
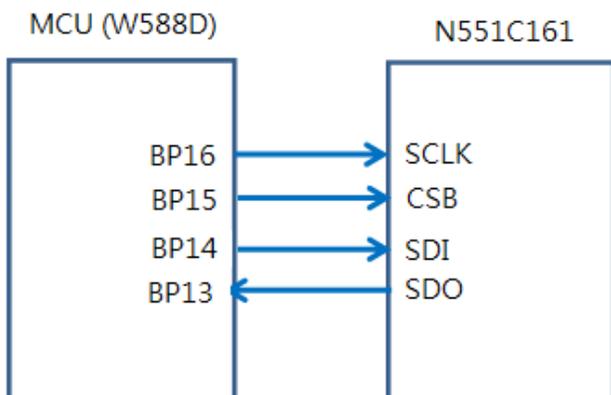
8. REVISION HISTORY

Version	Date	Substantial Changes	Page
A1.0	Sep. 2012	Initial Release	All
A2.0	Jul. 2012	Revise interface of application circuit	

Important Notice

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