

# N584Hxxx

## Data Sheet

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## 1. General Description

N584Hxxx is a 4-bit microcontroller-based speech synthesizer with PWM mode output to drive the speaker directly. The synthesizer contains one voice-channel and/or dual tone melody. It has *Ultra I/O™* to simplify the procedure of defining the output pattern, besides, it also includes 4-level Low Voltage Detection function. The N584Hxxx family contains several devices with different playback duration shown as below:

N584H	H009	H010	H019	H020	H029	H030	H039	H040
ROM (Kbit)	300	300	620	620	940	940	1260	1260
*Duration	12"	12"	24"	24"	37"	37"	49"	49"
I/O pins	4	8	4	8	4	8	4	8

N584H	H060	H070	H120	H160	H170	H210	H260	H300
ROM (Kbit)	1740	1900	3340	4070	4460	5740	7020	7980
*Duration	68"	74"	131"	159"	175"	225"	275"	312"
I/O pins	8	8	16	16	16	16	16	16

Note1: The duration time is based on 4-bit NM4 at 6 KHz sampling rate

## 2. Features

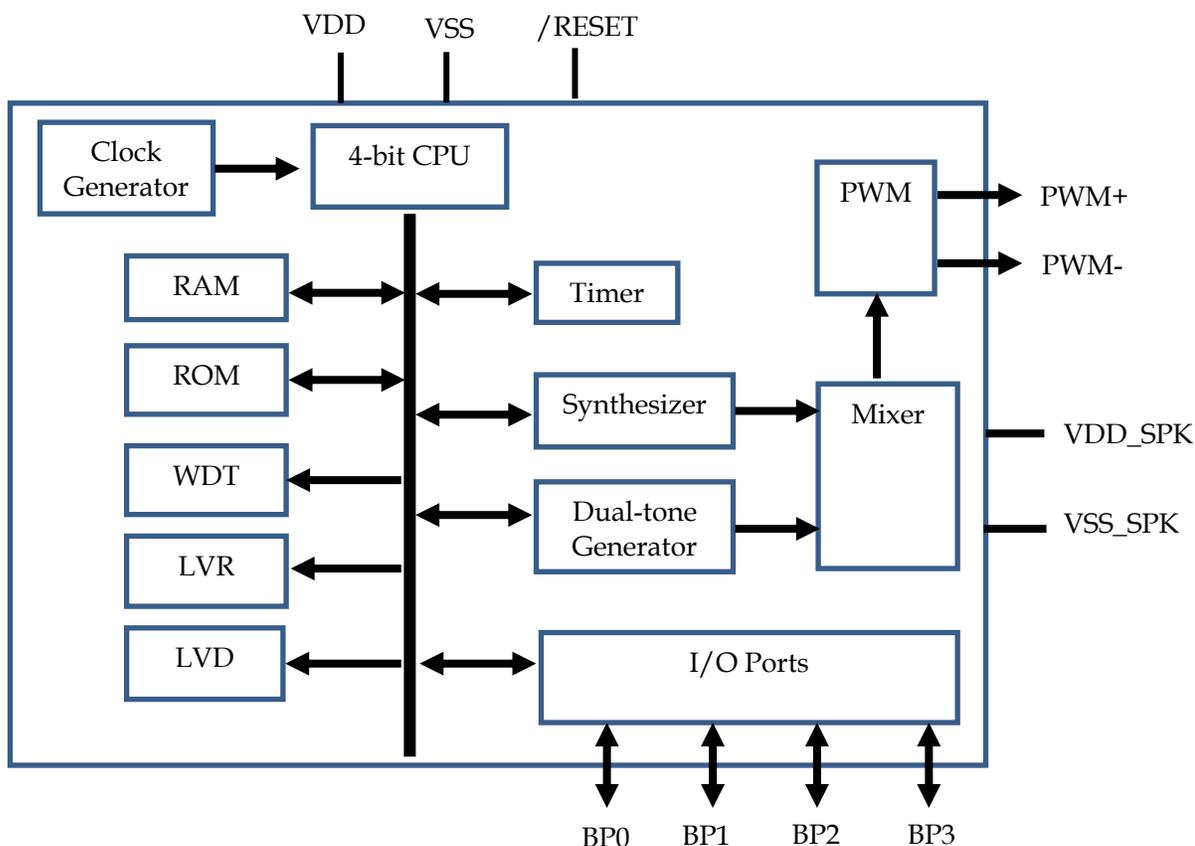
- Operating Voltage and CPU Frequency:
  - 1.8 ~ 5.5V (Fcpu = 4 MHz)
  - 2.0 ~ 5.5V (Fcpu = 8 MHz)
- Speech synthesis
  - 1-channel voice
  - Dual Tone Melody w/ 8 octaves (N584H120 ~ N584H300)
  - 4-bit NM4
- Build in internal oscillator (TRIM)
- Build in PWM Direct Drive circuit, with 4-level volume control
- Programmable sample rate
- Provides power management to save current consumption
  - 4 / 8 MHz system clock, with Ring type oscillator
  - STOP mode for stopping entire device's operation

- Provides 4 ~ 16 I/O
  - N584H009, H019, H029, H039: 4 I/O (BP0)
  - N584H010, H020, H030, H040, H060, H070: 8 I/O (BP0, BP1)
  - N584H120, H160, H170, H210, H260, H300: 16 I/O (BP0, BP1, BP2, BP3)
- High sink current capability
- Support capture timer to implement up to 8 capture sensor key
- Input can be set as active low (internal pull high) or active high (internal pull low)
- Provides 96\*4 ~ 224\*4 bits RAM
- Provides 64K\*10 of program data
- Provides IR carrier generator (38 KHz or 56 KHz)
- Provides Watch Dog Timer (WDT)
- Provides Low Voltage Reset (LVR: 1.7V, 1.9V)
- Provides Low Voltage Detection (LVD: 2.2V, 2.4V, 3.0V, 3.3V) with deviation +/-5%
- Shared ROM for voice and program storage
- Supports **PowerScript™** for developing codes easily
- Full-fledged development system
  - Source-level ICE debugger (**PowerScript™** format)
  - Event synchronization mechanism
  - User-friendly GUI environment
  - It has **Ultra I/O™** to simplify the defined output pattern

### 3. Pad Description

Pad Name	I/O	Function
BP00~BP03	I/O	Bi-directional I/O port0, defined as input or output. As input, it can be set as pull-high, pull-low or floating. As output, it is defined as CMOS. BP03 can also be defined as IR carrier output (by mask option).
BP10~BP13	I/O	Bi-directional I/O port1, defined as input or output. As input, it can be set as pull-high, pull-low or floating. As output, it is defined as CMOS.
BP20~BP23	I/O	Bi-directional I/O port2, defined as input or output. As input, it can be set as pull-high, pull-low or floating. As output, it is defined as CMOS.
BP30~BP33	I/O	Bi-directional I/O port3, defined as input or output. As input, it can be set as pull-high, pull-low or floating. As output, it is defined as CMOS.
VDD, VDD_IO	-	Power supply
VSS, VSS_IO	-	Ground
PWM+	O	PWM drive positive output
PWM-	O	PWM drive negative output
VDD_SPK	-	Power supply for PWM drive
VSS_SPK	-	Ground for PWM drive
/RESET	I	Chip reset input with Schmitt trigger, internal pull-high
TEST	-	Test PAD, no connection

### 4. Block Diagram



### 5. Electrical Characteristics

#### 5.1 Absolute Maximum Ratings

Item	Symbol	Conditions	Rated Value	Unit
Power Supply	VDD – VSS	-	-0.3 ~ +7.0	V
Input Voltage	VIN	All Inputs	VSS-0.3 ~ VDD+0.3	V
Storage Temp.	TSTG	-	-55 ~ +150	°C
Operating Temp.	TOPR	-	0 ~ +70	°C

NOTE:

Operating the device under conditions beyond those indicated above may cause permanent damage or affect device reliability.

## 5.2 DC Parameters

(VDD-VSS = 4.5V, VDD\_SPK-VSS\_SPK=4.5V, TA = 25° C; no load, unless otherwise specified)

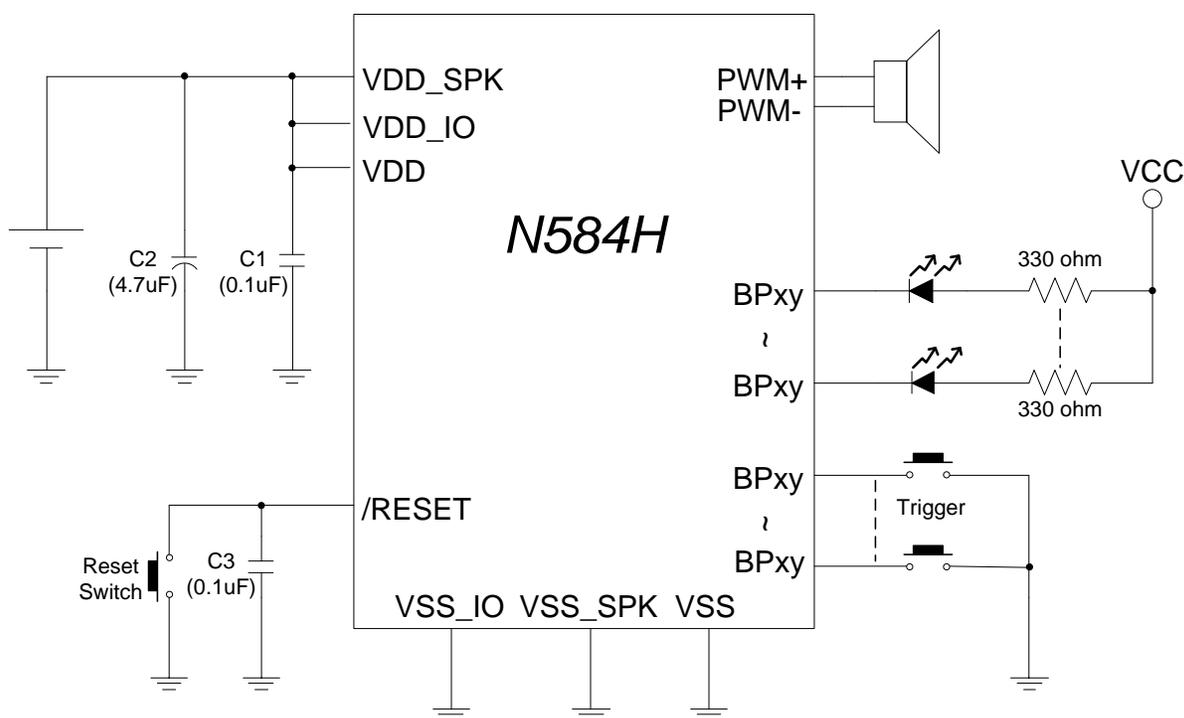
Parameter	Sym	Conditions	Min	Typ	Max	Unit
Operating voltage	VDD	Fcpu = 4 MHz Fcpu = 8 MHz	1.8 2.0		5.5 5.5	V
Operating current	I <sub>OP</sub>	Fcpu=8 MHz, VDD=4.5V		1.5		mA
		Fcpu=8 MHz, VDD=3.0V		1.0		
Standby current	I <sub>SB</sub>	VDD=4.5V			1	μA
		VDD=3.0V			1	
Output high current (BP0, BP1,BP2,BP3)	I <sub>OH</sub>	VDD=3.0V, Vout=2.6V	-4	-6		mA
		VDD=4.5V, Vout=2.6V		-30		
Output low current (BP0, BP1,BP2,BP3)	I <sub>OL</sub>	VDD=3.0V, Vout=0.4V	8	12		mA
		VDD=4.5V, Vout=1.0V		34		
PWM driver current	I <sub>pw</sub>	Rl=8Ω, connect to PWM+ and PWM-	200			mA
Pull-high resistor (BP0, BP1,BP2,BP3)	R <sub>PH</sub>	VDD=4.5V	90K 0.6M	150K 1M	210K 1.4M	Ω
Pull-low resistor (BP0, BP1,BP2,BP3)	R <sub>PL</sub>	VDD=4.5V	90K 0.6M	150K 1M	210K 1.4M	Ω
LVD detect voltage	VLVD	LVD_SEL[1:0] = 00	2.09	2.2	2.31	V
		LVD_SEL[1:0] = 01	2.28	2.4	2.52	
		LVD_SEL[1:0] = 10	2.85	3.0	3.15	
		LVD_SEL[1:0] = 11	3.13	3.3	3.47	

### 5.3 AC Parameters

(VDD-VSS = 4.5V, TA = 25° C; unless otherwise specified)

Parameter	Sym	Conditions	Min	Typ	Max	Unit
Main-clock Frequency	Fosc	8 MHz	7.95	8.19	8.44	MHz
Frequency deviation	$\frac{\Delta F}{F}$	Fosc=8 MHz, VDD=2.2 ~ 5.5V $\frac{Fosc(max) - Fosc(min)}{Fosc(min)}$		3	5	%

## 6. Typical Application Circuit



Notes:

1. In PCB layout, VSS\_IO, VSS\_SPK should be connected to VSS; and VDD\_IO, VDD\_SPK should be connected to VDD
2. The C1 capacitor 0.1uF is recommended to prevent the IC from hang-up as battery power bouncing. For power line layout in extended length, suggest C1 to be 1uF.

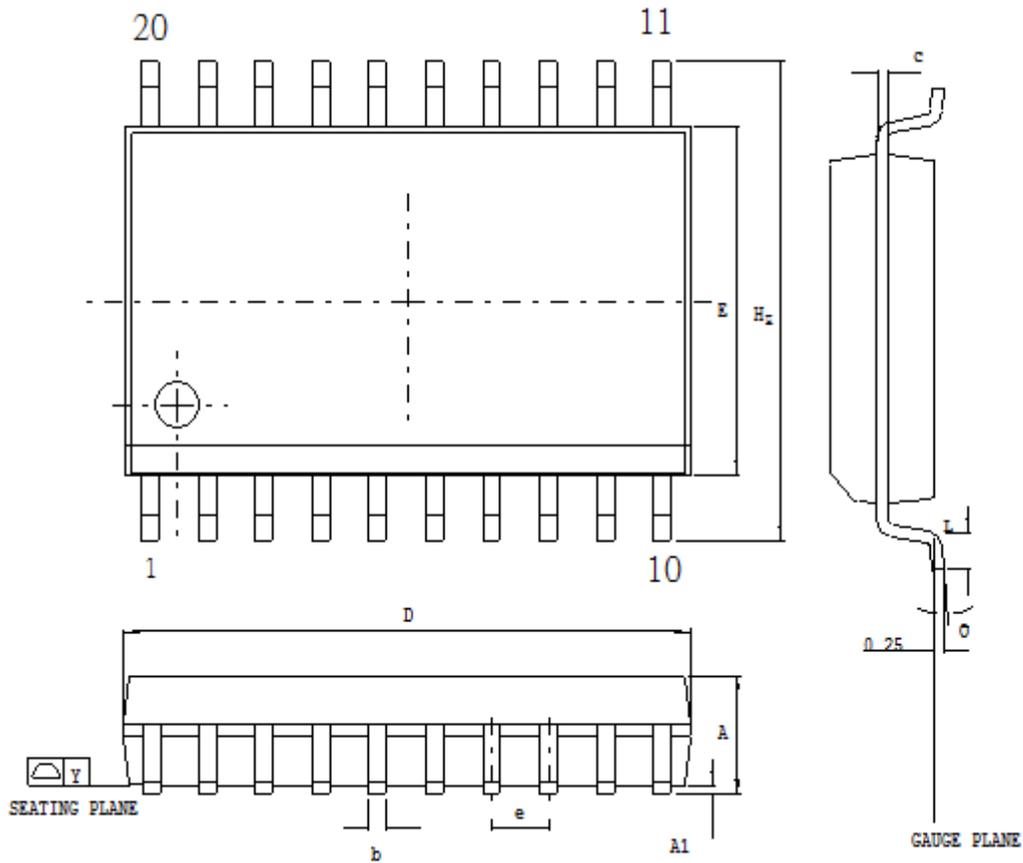
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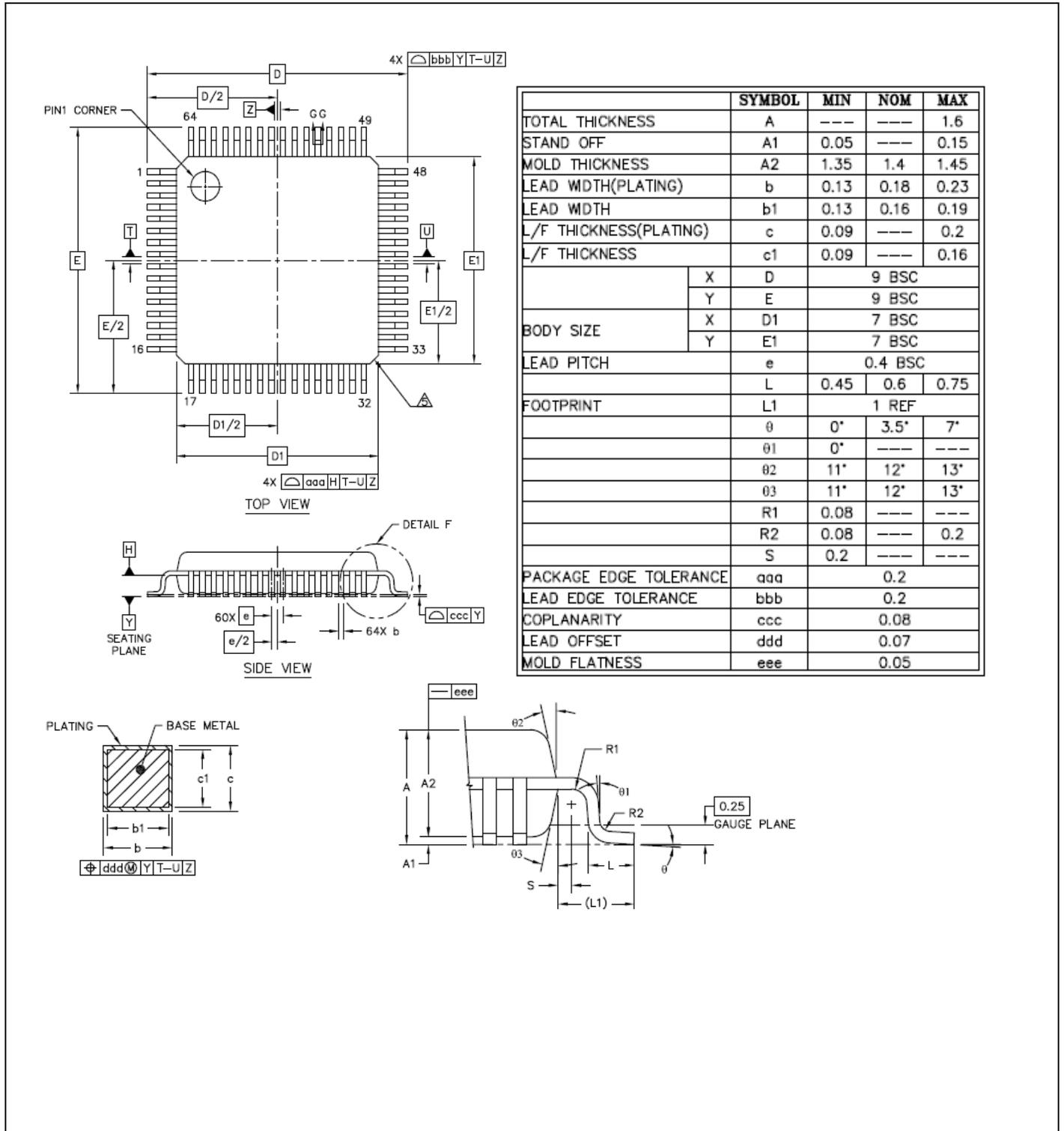
Package Dimension (SOP20, 300mil)



Control dimensions are in milimeters .

SYMBOL	DIMENSION IN MM		DIMENSION IN INCH	
	MIN.	MAX.	MIN.	MAX.
A	2.35	2.65	0.093	0.104
A1	0.10	0.30	0.004	0.012
b	0.33	0.51	0.013	0.020
c	0.23	0.32	0.009	0.013
E	7.40	7.60	0.291	0.299
D	12.60	13.00	0.496	0.512
e	1.27 BSC		0.050 BSC	
H±	10.00	10.65	0.394	0.419
Y	0.10		0.004	
L	0.40	1.27	0.016	0.050
Ø	0	8	0	8

Package Dimension (LQFP64, 7x7x1.4mm, footprint 2.0mm)



	SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS	A	---	---	1.6
STAND OFF	A1	0.05	---	0.15
MOLD THICKNESS	A2	1.35	1.4	1.45
LEAD WIDTH(PLATING)	b	0.13	0.18	0.23
LEAD WIDTH	b1	0.13	0.16	0.19
L/F THICKNESS(PLATING)	c	0.09	---	0.2
L/F THICKNESS	c1	0.09	---	0.16
	X D	9 BSC		
	Y E	9 BSC		
BODY SIZE	X D1	7 BSC		
	Y E1	7 BSC		
LEAD PITCH	e	0.4 BSC		
	L	0.45	0.6	0.75
FOOTPRINT	L1	1 REF		
	θ	0°	3.5°	7°
	θ1	0°	---	---
	θ2	11°	12°	13°
	θ3	11°	12°	13°
	R1	0.08	---	---
	R2	0.08	---	0.2
	S	0.2	---	---
PACKAGE EDGE TOLERANCE	aaa	0.2		
LEAD EDGE TOLERANCE	bbb	0.2		
COPLANARITY	ccc	0.08		
LEAD OFFSET	ddd	0.07		
MOLD FLATNESS	eee	0.05		

## 8. Revision History

Version	Date	Substantial Changes	Page
A0.1	Mar. 2015	First establishment	
A0.2	Apr. 2015	Add part numbers	ALL
A0.3	May 2015	Add VDD range at Fcpu = 4 MHz	2, 5
A0.4	Jul. 2015	Revise note of AP circuit on C1 value	8
A1.0	Nov. 2015	Remove 'PRELIMINARY', update DC characteristic, Application circuit	1, 6, 8
A2.0	Jul. 2016	Revise application circuit	9
A3.0	Dec. 2016	Add N584H160 Part No.	3
A4.0	Sep. 2017	Add package information	10-12

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