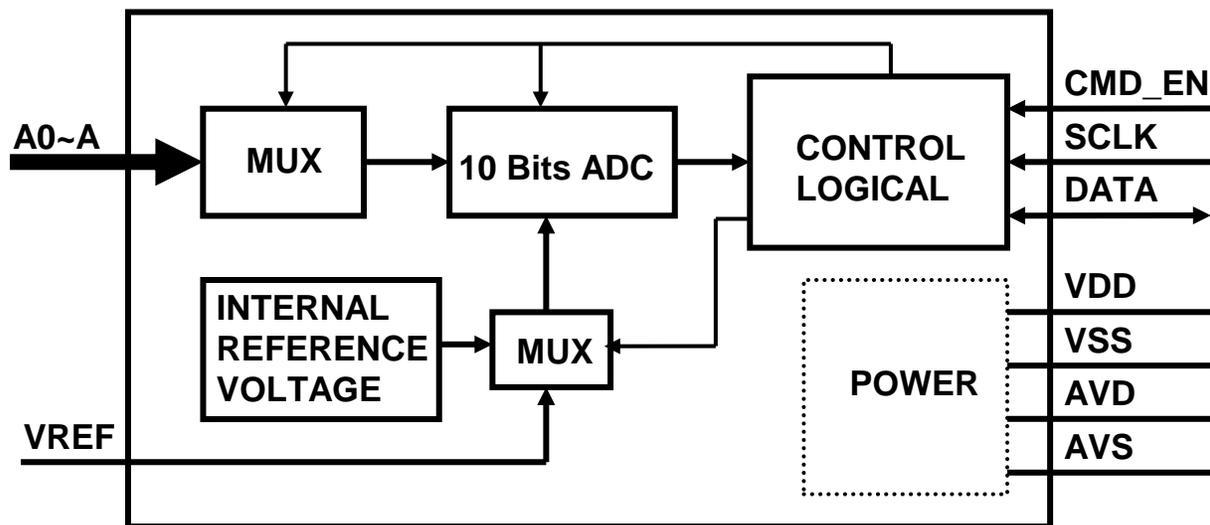# 1 General Description

W55AD808, a low cost 8-bit ADC with 8 input channels. Each channel can be defined as digital or analog input mode independently. In analog input mode, this channel can accept an analog input range from 0V ~ V_{REF} and convert it into a 10-bit digital data format (with 8-bit significant digits). W55AD808 provides a serial interface for host CPU to control it. Beside analog input mode, all input pins can be defined as digital input mode; host CPU can monitor them by the serial interface.

2 Features

- Operating voltage: 2.7V ~ 5.5V.
- Guarantee 8-bit A/D resolution.
- 8 analog input channels.
- Each channel can be independently programmed to a digital input mode.
- 50KHz conversion rate.
- 10-bit ADC with 8-bit significant digits.
- Operation current: 0.5mA ~ 1mA.
- Stand-by current: <0.5uA @ 4.5V.
- Auto entry power-down mode.
- Less external components.

3 Block Diagram

4 W55AD808 Pad Description

Symbol	Pad No.	I/O	Functional Description
A0	1	I	Digital or analog input path 0.
A1	2	I	Digital or analog input path 1.
A2	3	I	Digital or analog input path 2.
A3	4	I	Digital or analog input path 3.
A4	5	I	Digital or analog input path 4.
A5	6	I	Digital or analog input path 5.
A6	7	I	Digital or analog input path 6.
A7	8	I	Digital or analog input path 7.
VSS	9	Ground	Digital ground return path.
VDD	10	Power	Digital power path.
DATA	11	I/O	Data input or output for Serial interface communication.
SCLK	12	I	Shift clock for command input and data input or output.
CMD_EN	13	I	Command enable for serial communication.
AVDD	14	Power	Analog power path.
AVSS	15	Ground	Analog ground return path.
VREF	16	I	External reference voltage for analog to digital conversion.

5 Electronic Characteristics

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Operating voltage	V_{DD}		2.7	-	5.5	V
Operating current	I_{DD}	F_{SMP} = 18.5KHz	340	-	1900	μA
Standby current	I_{SB}	V_{DD}=2.7V~5.5V		0.1		μA
Conversion rate	F_{SMP}	V_{DD}=3.0V		50		KHz
Differential Non-linearity	DNL	V_{DD}=2.7V	-0.34	-	+0.14	LSB
		V_{DD}=3.0V	-0.32		+0.11	
		V_{DD}=3.9V	-0.28		+0.18	
		V_{DD}=4.5V	-0.26		+0.14	
		V_{DD}=5.0V	-0.18		+0.18	
		V_{DD}=5.25V	-0.22		+0.22	
Integral Non-linearity	INL	V_{DD}=2.7V	-3.53	-	+1.57	LSB
		V_{DD}=3.0V	-2.83		+1.12	
		V_{DD}=3.9V	-1.08		+0.18	
		V_{DD}=4.5V	-0.62		+0.17	

Parameter	Symbol	Test Condition	Measured Value			Unit
			Min.	Typ.	Max.	
		V_{DD}=5.0V	-0.33		+0.21	
		V_{DD}=5.25V	-0.26		+0.18	
No missing code	NMC	V_{DD}=2.7V~5.25V	8	-	-	Bits
Signal to noise and distortion	SINAD	V_{DD}=2.7V	-	38.78	-	dB
		V_{DD}=3.0V		40.77		
		V_{DD}=3.9V		48.15		
		V_{DD}=4.5V		51.31		
		V_{DD}=5.0V		53.12		
		V_{DD}=5.25V		53.44		
Output drive current of DATA ($V_{OP} = V_{DD} - 0.5V$)	I_{dv}	V_{DD}=2.7V	-	2.692	-	mA
		V_{DD}=3.0V		3.045		
		V_{DD}=3.9V		3.239		
		V_{DD}=5.0V		4.628		
Sink current of DATA ($V_{OP} = V_{SS} + 0.5V$)	I_{sk}	V_{DD}=2.7V	-	4.797	-	mA
		V_{DD}=3.0V		5.362		
		V_{DD}=3.9V		5.436		
		V_{DD}=5.0V		7.657		

6 Application Schematic
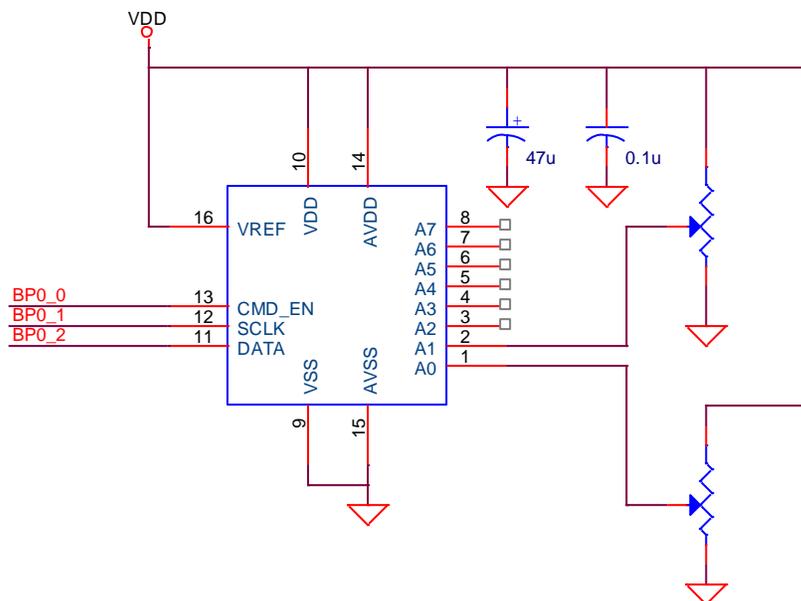
7 Revision History

Date	Revision	Notes
07/01/2004	A1.0	Preliminary version.
07/11/2004	A1.1	Update preliminary version.
07/13/2004	A2.0	Release version.
08/24/2005	A2.1	Add important notice.
10/30/2008	A3.0	Change document logo, from Winbond to Nuvoton
10/30/2012	A4.0	Revise max. VDD as 5.5V

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