RK292X Datasheet
Preliminary

Revision 1.1
Sep. 2012

Chapter 1 Introduction

RK292X is a low power, high performance processor solution for low-end tablet, Android Portable GPS and other digital multimedia applications, and integrates single-core Cortex-A9 with separately Neon and FPU coprocessor, and also with 128KB L2 Cache.

Many embedded powerful hardware engines provide optimized performance for high-end application. RK292X supports almost full-format video decoder by 1080p@60fps, also support H.264/MVC/VP8 encoder by 1080p@30fps, high-quality JPEG encoder/decoder and special image preprocessor and postprocessor.

Embedded 3D GPU makes RK292X completely compatible with OpenGL ES1.1 and 2.0, OpenVG1.1 etc. Special 2D hardware engine with MMU will maximize display performance.

RK292X has high-performance external memory interface (DDR3/LVDDR3) capable of sustaining demanding memory bandwidths, also provides a complete set of peripheral interface to support very flexible applications.

This document will provide guideline on how to use RK292X correctly and efficiently. In them, the chapter 1 and chapter 2 will introduce the features, block diagram, signal descriptions and system usage of RK292X, the chapter 3 through chapter 45 will describe the full function of each module in detail.

1.1 Features

1.1.1 Processor

- Single-core ARM Cortex-A9 processor is a high-performance, low-power, cached application processor
- Full implementation of the ARM architecture v7-A instruction set, ARM Neon Advanced SIMD (single instruction, multiple data) support for accelerated media and signal processing computation
- Superscalar, variable length, out-of-order pipeline with dynamic branch prediction, 8-stage pipeline
- Include VFPv3 hardware to support single and double-precision add, subtract, divide, multiply and accumulate, and square root operations
- Integrated timer and watchdog timer in CPU
- Integrated 32KB L1 instruction cache , 32KB L1 data cache, 4-wat set associative
- 128KB unified L2 Cache
- coresight debug solution
- One isolated voltage domain to support DVFS
- Maximum frequency can be up to 670MHz@1.08v,125C and 1.0GHz@1.2v,25C

1.1.2 Memory Organization

- Internal on-chip memory
  - 8KB internal SRAM
- External off-chip memory①
  - DDR3-800, 16bits data width, 2 ranks, 1GB(max) address space per rank
  - LVDDR3-800, 16bits data width, 2 ranks, 1GB(max) address space per rank
  - Async/Toggle/Sync Nand Flash(include LBA Nand), 8bits data width,4 banks

1.1.3 Internal Memory

- Internal BootRom
  - Support system boot from the following device :
    - 8bits Nand Flash
    - SPI interface
    - eMMC interface
  - Support system code download by the following interface:
    - USB OTG
    - UART2

1.1.4 External Memory or Storage device

- Dynamic Memory Interface (DDR3/LVDDR3)
  - Compatible with JEDEC standard DDR3/ LVDDR3 SDRAM
  - Data rates of up to 800Mbps(400MHz) for DDR3/LVDDR3
  - Support up to 2 ranks (chip selects), maximum 1GB address space per rank
  - 6 host ports with 64bits AXI bus interface for system access, AXI bus clock asynchronous with DDR clock
  - Programmable timing parameters support DDR3/LVDDR3 SDRAM from various vendor
  - Advanced command reordering and scheduling to maximize bus utilization
  - Low power modes, such as power-down and self-refresh for DDR3/ LVDDR3 SDRAM;
  - Compensation for board delays and variable latencies through programmable pipelines
  - Programmable output and ODT impedance with dynamic PVT compensation

- Nand Flash Interface
  - Support 8bits async/toggle/syncnand flash, up to 4 banks
  - Support LBA nand flash
  - 16bits, 24bits, 40bits, 60bits hardware ECC
  - For DDR nand flash, support DLL bypass and 1/4 or 1/8 clock adjust, maximum clock rate is 66.5MHz
  - For async/togglenand flash, support configurable interface timing , maximum data rate is 16bit/cycle
  - Embedded two 256x32bits buffers to support ping-pong operation
  - Embedded AHB master interface to do data transfer by DMA method
  - Also support data transfer by AHB slave interface together with external DMAC

- eMMC Interface
  - Compatible with standard iNAND interface
  - Support MMC4.41 protocol
  - Provide eMMC boot sequence to receive boot data from external eMMC device
  - Support combined single FIFO(32x32bits) for both transmit and receive operations
  - Support FIFO over-run and under-run prevention by stopping card clock automatically
  - Support CRC generation and error detection
  - Embedded clock frequency division control to provide programmable baud rate
  - Support block size from 1 to 65535Bytes
  - 8bits data bus width

- SD/MMC Interface
  - Compatible with SD3.0, MMC ver4.41
  - Support combined single FIFO(32x32bits) for both transmit and receive operations
  - Support FIFO over-run and under-run prevention by stopping card clock automatically
  - Support CRC generation and error detection
  - Embedded clock frequency division control to provide programmable baud rate
  - Support block size from 1 to 65535Bytes
    Data bus width is 4bits

1.1.5 System Component

- CRU (clock & reset unit)
  - Support clock gating control for individual components inside RK292X
  - Support global soft-reset control for whole SOC, also individual soft-reset for

every components
- Support flexible clock solution, including clock source, clock mux, clock frequency division
- One oscillator with 24MHz clock and 4 embedded PLLs

- Timer
  - on-chip 32bits Timers with interrupt-based operation
  - Provide two operation modes: free-running and user-defined count
  - Support timer work state checkable
  - 24MHz/PCLK clock input for operating domain, and PCLK input for bus interface domain.

- PWM
  - Three on-chip PWMs with interrupt-based operation
  - Programmable 4-bit pre-scalar from apb bus clock
  - Embedded 32-bit timer/counter facility
  - Support single-run or continuous-run PWM mode
  - Provides reference mode and output various duty-cycle waveform

- WatchDog
  - 32 bits watchdog counter width
  - Counter clock is from apb bus clock
  - Counter counts down from a preset value to 0 to indicate the occurrence of a timeout
  - WDT can perform two types of operations when timeout occurs:
    - Generate a system reset
    - First generate an interrupt and if this is not cleared by the service routine by the time a second timeout occurs then generate a system reset
  - Programmable reset pulse length
  - Totally 16 defined-ranges of main timeout period

- Bus Architecture
  - multi-layer AXI/AHB/APB composite bus architecture
  - Five embedded axi interconnect. For each interconnect with AXI/AHB/APB composite bus, clocks for AXI/AHB/APB domains are always synchronous, and different integer ratio is supported for them.

- Interrupt Controller
  - Support 3 PPI interrupt source and 96 SPI interrupt sources input from different components inside RK292X
  - Support 16 softwre-triggered interrupts
  - Input interrupt level is fixed , only high-level sensitive
  - Two interrupt output (nFIQ and nIRQ) to per Cortex-A9, both are low-level sensitive
  - Support different interrupt priority for each interrupt source, and they are always software-programmable

- DMAC
  - Micro-code programming based DMA
  - The specific instruction set provides flexibility for programming DMA transfers
  - Linked list DMA function is supported to complete scatter-gather transfer
  - Support internal instruction cache
  - Embedded DMA manager thread
  - Support data transfer types with memory-to-memory, memory-to-peripheral, peripheral-to-memory
  - Signals the occurrence of various DMA events using the interrupt output signals
  - Mapping relationship between each channel and different interrupt outputs is software-programmable

- One embedded DMA controller in peri system

1.1.6 Video CODEC

- Shared internal memory and bus interface for video decoder and encoder
- Video Decoder
  - Real-time video decoder of MPEG-1, MPEG-2, MPEG-4,H.263, H.264 , VC-1 , RV , VP6/VP8 , Sorenson Spark
  - Error detection and concealment support for all video formats
  - Output data structure after decoder is YCbCr 4:2:0 semi-planar to have more efficient bus usage, For H.264, YCbCr 4:0:0(monochrome) is also supported
  - Minimum image size is 48x48 for all video formats
  - H.264 up to HP level 4.2 : 1080p@60fps (1920x1088)[8]
  - MPEG-4 up to ASP level 5 : 1080p@60fps (1920x1088)
  - MPEG-2 up to MP : 1080p@60fps (1920x1088)
  - MPEG-1 up to MP : 1080p@60fps (1920x1088)
  - H.263 : 576p@60fps (720x576)
  - Sorenson Spark : 1080p@60fps (1920x1088)
  - VC-1 up to AP level 3 : 1080p@30fps (1920x1088)
  - RV8/RV9/RV10 : 1080p@60fps (1920x1088)
  - VP6/VP8 : 1080p@60fps (1920x1088)
  - For H.264, Image cropping not supported
  - For MPEG-4,GMC(global motion compensation) not supported
  - For VC-1, upscaling and range mapping are supported in image post-processor
  - For MPEG-4 SP/H.263/Sorenson spark, using a modified H.264 in-loop filter to implement deblocking filter in post-processor unit

- Video Encoder
  - Encoder only for H.264 (BP@level4.0, MP@level4.0,HP@level4.0) standard
  - Only support I and P slices, not B slices
  - Entropy encoding is CAVLC in BP and CABAC in MP
  - Support error resilience based on constrained intra prediction and slices
  - Maximum MV length is +/- 14 pixels in vertical direction and +/-30 pixels in horizontal direction
  - Motion vector pixel accuracy is up to 1/4 pixels in 720p resolution and 1/2 pixels in 1080p resolution
  - 12 intra prediction modes
  - Number of reference frames is 1
  - Maximum number of slice groups is 1
  - Input data format :
    - YCbCr 4:2:0 planar
    - YCbCr 4:2:0 semi-planar
    - YCbYCr 4:2:2
    - CbYCrY 4:2:2 interleaved
    - RGB444 and BGR444
    - RGB555 and BGR555
    - RGB565 and BGR565
    - RGB888 and BRG888
    - RGB101010 and BRG101010
  - Output data format : H.264 byte unit stream and H.264 NAL unit stream
  - Image size is from 96x96 to 1920x1088(Full HD)
  - Maximum frame rate is up to 30fps@1920x1080[8]
  - Bit rate supported is from 10Kbps to 20Mbps

1.1.7 JPEG CODEC

- JPEG decoder
  - Input JPEG file : YCbCr 4:0:0, 4:2:0, 4:2:2, 4:4:0, 4:1:1 and 4:4:4 sampling formats

- Output raw image : YCbCr 4:0:0, 4:2:0, 4:2:2, 4:4:0, 4:1:1 and 4:4:4 semi-planar
- Decoder size is from 48x48 to 8176x8176(66.8Mpixels)
- Maximum data rate④ is up to 76million pixels per second

- JPEG encoder
  - Input raw image :
    - YCbCr 4:2:0 planar
    - YCbCr 4:2:0 semi-planar
    - YCbYCr 4:2:2
    - CbYCrY 4:2:2 interleaved
    - RGB444 and BGR444
    - RGB555 and BGR555
    - RGB565 and BGR565
    - RGB888 and BRG888
    - RGB101010 and BRG101010
  - Output JPEG file : JFIF file format 1.02 or Non-progressive JPEG
  - Encoder image size up to 8192x8192(64million pixels) from 96x32
  - Maximum data rate④ up to 90million pixels per second

1.1.8 Image Enhancement

- Image pre-processor(embedded inside video encoder)
  - Only used together with HD video encoder inside RK292X , not support stand-alone mode
  - Provides RGB to YCbCr 4:2:0 color space conversion, compatible with BT.601 , BT.709 or user defined coefficients
  - Provides YCbCr4:2:2 to YCbCr4:2:0 color space conversion
  - Support cropping operation from 8192x8192 to any supported encoding size
  - Support rotation with 90 or 270 degrees

- Video stabilization(embedded inside video encoder)
  - Work in combined mode with HD video encoder inside RK30xx and stand-alone mode
  - Adaptive motion compensation filter
  - Support scene detection from video sequence, encodes key frame when scene change noticed

- Image post-processor(embedded inside video decoder)
  - Combined with HD video decoder and JPEG decoder, post-processor can read input data directly from decoder output to reduce bus bandwidth
  - Also work as a stand-alone mode, its input data is from a camera interface or other image data stored in external memory
  - Input data format :
    - any format generated by video decoder in combined mode
    - YCbCr 4:2:0 semi-planar
    - YCbCr 4:2:0 planar
    - YCbYCr 4:2:2
    - YCrYCb 4:2:2
    - CbYCrY 4:2:2
    - CrYCbY 4:2:2
  - Ouput data format:
    - YCbCr 4:2:0 semi-planar
    - YCbYCr 4:2:2
    - YCrYCb 4:2:2
    - CbYCrY 4:2:2
    - CrYCbY 4:2:2
    - Fully configurable ARGB channel lengths and locations inside 32bits, such as

ARGB8888, RGB565, ARGB4444 etc.

- Input image size:
  - Combined mode : from 48x48 to 8176x8176 (66.8Mpixels)
  - Stand-alone mode : width from 48 to 8176,height from 48 to 8176, and maximum size limited to 16.7Mpixels
  - Step size is 16 pixels
- Output image size: from 16x16 to 1920x1088 (horizontal step size 8,vertical step size 2)
- Support image up-scaling :
  - Bicubic polynomial interpolation with a four-tap horizontal kernel and a two-tap vertical kernel
  - Arbitrary non-integer scaling ratio separately for both dimensions
  - Maximum output width is 3x input width
  - Maximum output height is 3x input height
- Support image down-scaling:
  - Arbitrary non-integer scaling ratio separately for both dimensions
  - Unlimited down-scaling ratio
- Support YUV to RGB color conversioin, compatible with BT.601-5, BT.709 and user definable conversion coefficient
- Support dithering (2x2 ordered spatial dithering for 4,5,6bit RGB channel precision
- Support programmable alpha channel and alpha blending operation with the following overlay input formats:
  - 8bit alpha +YUV444, big endian channel order with AYUV8888
  - 8bit alpha +24bit RGB, big endian channel order with ARGB8888
- Support deinterlacing with conditional spatial deinterlace filtering, only compatible with YUV420 input format
- Support RGB image contrast / brightness / color saturation adjustment
- Support image cropping & digital zoom only for JPEG or stand-alone mode
- Support picture in pcture
- Support image rotation (horizontal flip, vertical flip, rotation 90,180 or 270 degrees)

1.1.9 Graphics Engine

- 3D Graphics Engine :
  - High performance OpenGL ES1.1 and 2.0, OpenVG1.1 etc.
  - Embedded 4 shader cores with shared hierarchical tiler
  - Separate vertex(geometry) and fragment(pixel) processing for maximum parallel throughput
  - Provide MMU and L2 Cache with 32KB size

- 2D Graphics Engine :
  - Pixel rate: 266M pixel/s without scale, 133M pixel/s with bilinear scale, 66.5M pixel/s with bicubic scale.
  - Bit Blit with Strength Blit, Simple Blit and Filter Blit
  - Color fill with gradient fill, and pattern fill
  - Line drawing with anti-aliasing and specified width
  - High-performance stretch and shrink
  - Monochrome expansion for text rendering
  - ROP2, ROP3, ROP4 full alpha blending and transparency
  - Alpha blending modes including Java 2 Porter-Duff compositing blending rules , chroma key, and pattern mask
  - 8K x 8K raster 2D coordinate system
  - Arbitrary degrees rotation with anti-aliasing on every 2D primitive
  - Programmable bicubic filter to support image scaling
  - Blending, scaling and rotation are supported in one pass for stretch blit

1.1.10 Video IN/OUT

- Camera Interface
  - Support up to 5M pixels
  - 8bits CCIR656(PAL/NTSC) interface
  - 8bits raw data interface
  - YUV422 data input format with adjustable YUV sequence
  - YUV422,YUV420 output format with separately Y and UV space
  - Support picture in picture (PIP)
  - Support image crop with arbitrary windows

- Display Interface
  - independent display controller
  - Support LCD or TFT interfaces up to 1920x1080
  - Support HDMI 1.4 output up to 1080p@30fps
  - Parallel RGB LCD Interface:
    RGB888(24bits),RGB666(18bits) ,RGB565(16bits)
  - 4 display layers:
    - One background layer with programmable 24bits color
    - One video layer (win0)
      - RGB888, ARGB888, RGB565, YUV422, YUV420
      - maximum resolution is 1920x1080,support virtual display
      - 1/8 to 8 scaling up/down engine with arbitrary non-integer ratio
      - 256 level alpha blending
      - Support transparency color key
    - One video layer (win1)
      - RGB888, ARGB888, RGB565
      - Support virtual display
      - 256 level alpha blending
      - Support transparency color key
    - Hardware cursor(win3)
      - 2BPP
      - Maximum resolution 64x64
      - 3-color and transparent mode
      - 2-color + transparency + tran_invert mode
      - 16 level alpha blending
  - Win0 and Win1 layer overlay exchangeable
  - Support color space conversion :
    YUV2RGB(rec601-mpeg/rec601-jpeg/rec709) and RGB2YUV
  - Deflicker support for interlace output
  - Support replication(16bits to 24bits) and dithering(24bits to 16bits/ 18bits) operation
  - Blank and blank display
  - Support non-scaler and scaler output(max up to 1024x768)

- HDMI TX 1.4
  - HDMI version 1.4a, HDCP revision 1.2 and DVI version 1.0 compliant transmitter
  - Supports DTV from 480i to 1080i/p HD resolution
  - Supports 3D function defined in HDMI 1.4 spec
  - Supports data rate from 25MHz, 1.65bps up to 3.4Gbps over a Single channel HDMI
  - TMDS Tx Drivers with programmable output swing, resister values and pre-emphasis
  - Digital video interface supports a pixel size of 24, 30, 36, 48bits color depth in RGB
  - S/PDIF output supports PCM, Dolby Digital, DTS digital audio transmission (32-192kHz Fs) using IEC60958 and IEC 61937
  - Multiphase 4MHz fixed bandwidth PLL with low jitter

- HDCP encryption and decryption engine contains all the necessary logic to encrypt the incoming audio and video data
- Support HDMI LipSync if needed as addon feature
- Lower power operation with optimal power management feature
- The EDID and CEC function are also supported by Innosilicon HDMI Transmitter Controller
- Optional Monitor Detection supported through Hot Plug

- LVDS interface
  - 135MHz clock support
  - 28:4 data sub_channel compression at data rates up to 945 Mbps per channel
  - Support VGA,SVGA,XGA and single pixel SXGA
  - PLL requires no external components
  - Comply with the Standard TIA/EIA-644-A LVDS standard
  - Support alternative LVDS output or LVTTL output

1.1.11 Audio Interface

- I2S/PCM with 2ch
  - Up to 2 channels (2xTX, 2xRX)
  - Audio resolution from 16bits to 32bits
  - Sample rate up to 192KHz
  - Provides master and slave work mode, software configurable
  - Support 3 I2S formats (normal , left-justified , right-justified)
  - Support 4 PCM formats(early , late1 , late2 , late3)
  - I2S and PCM cannot be used at the same time

- Audio Codec
  - 18 to 24 bit High Order Sigma-Delta modulation for DAC for >93 dB SNR configurable
  - 16 to 18 bit High Order Sigma-Delta modulation for ADC for >90 dB SNR configurable
  - Digital interpolation and decimation filter integrated
  - Line-in, Microphone in and Speaker out Interface
  - On-Chip Analog Post Filter and digital filters
  - Single–ended or differential Input and Output
  - Sampling Rate of 8kHz/12kHz/16kHz/ 24kHz/32kHz /48kHz/44.1K/96KHz
  - Support 16ohm to 32ohm Head Phone and Speaker Phone Output
  - Mono, Stereochannel supported
  - Optional Fractional PLL available that support 6Mhz to 20Mhz clock input to any clockoutput that meets 8kHz/12kHz/16kHz/ 24kHz/32kHz /48kHz/44.1K/96KHz and 128 time oversampling ratio.

1.1.12 Connectivity

- SDIO interface
  - Compatible with SDIO 3.0 protocol
  - Support FIFO over-run and under-run prevention by stopping card clock automatically
  - 4bits data bus width

- SPI Controller
  - Support serial-master and serial-slave mode, software-configurable
  - DMA-based or interrupt-based operation
  - Embedded two 32x16bits FIFO for TX and RX operation respectively
  - Support 2 chip-selects output in serial-master mode

- Uart Controller
  - 3 on-chip uart controller inside
  - DMA-based or interrupt-based operation

- UART0 Embeddeds two 64Bytes FIFO fRK292X or TX and RX operation respectively
- UART1/UART2 Embedded two 32Bytes FIFO for TX and RX operation respectively
- Support 5bit,6bit,7bit,8bit serial data transmit or receive
- Standard asynchronous communication bits such as start,stop and parity
- Support different input clock for uart operation to get up to 4Mbps or other special baud rate
- Support non-integer clock divides for baud clock generation
- Support auto flow control mode

- I2C controller
  - 4 on-chip I2C controller in RK292X
  - Multi-master I2C operation
  - Support 7bits and 10bits address mode
  - Software programmable clock frequency and transfer rate up to 400Kbit/s in the fast mode
  - Serial 8bits oriented and bidirectional data transfers can be made at up to 100Kbit/s in the standard mode

- GPIO
  - 4 groups of GPIO (GPIO0~GPIO3) , 32 GPIOs per group in GPIO0~GPIO3, totally have 128 GPIOs
  - All of GPIOs can be used to generate interrupt to Cortex-A9
  - All of pullup GPIOs are software-programmable for pullup resistor or not
  - All of pulldown GPIOs are software-programmable for pulldown resistor or not
  - All of GPIOs are always in input direction in default after power-on-reset

- USB Host2.0
  - Compatible with usb host2.0 specification
  - Supports high-speed(480Mbps), full-speed(12Mbps) and low-speed(1.5Mbps) mode
  - Provides 16 host mode channels
  - Support periodic out channel in host mode

- USB OTG2.0
  - Compatible with usb otg2.0 specification
  - Supports high-speed(480Mbps), full-speed(12Mbps) and low-speed(1.5Mbps) mode
  - Support up to 9 device mode endpoints in addition to control endpoint 0
  - Support up to 6 device mode IN endpoints including control endpoint 0
  - Endpoints 1/3/5/7 can be used only as data IN endpoint
  - Endpoints 2/4/6 can be used only as data OUT endpoint
  - Endpoints 8/9 can be used as data OUT and IN endpoint
  - Provides 9 host mode channels

1.1.13 Others

- SAR-ADC(Successive Approximation Register)
  - 3-channel single-ended 10-bit SAR analog-to-digital converter
  - Sample rate Fs is 200KHz
  - SAR-ADC clock must be large than 11*Fs, recommend is 11*Fs
  - DNL less than1 LSB , INL less than 2.0 LSB
  - Power supply is 3.3V (±10%) for analog interface

- eFuse
  - 64bits (64x1) high-density electrical Fuse
  - Programming condition : VP must be 2.5V(±10%)

- Program time is 64 cycles of eFuse operating clock.
- Read condition : VP must be 0V or floating or 2.5V(±10%)
- Provide inactive mode

- Package Type
  - RK2928G BGA313 (body: 16mm x 16mm; ball size: 0.4mm; ball pitch: 0.8mm)
  - RK2926 eLQFP176(body: 20mm x 20mm; pin pitch:0.4mm)

Notes :①: DDR3/LVDDR3 are not used simultaneously as well as async and sync ddr nand flash

②: In RK292X, Video decoder and encoder are not used simultaneously because of shared internal buffer

③: Actual maximum frame rate will depend on the clock frequency and system bus performance

④: Actual maximum data rate will depend on the clock frequency and JPEG compression rate

1.2 Block Diagram

The following diagram shows the basic block diagram for RK292X.

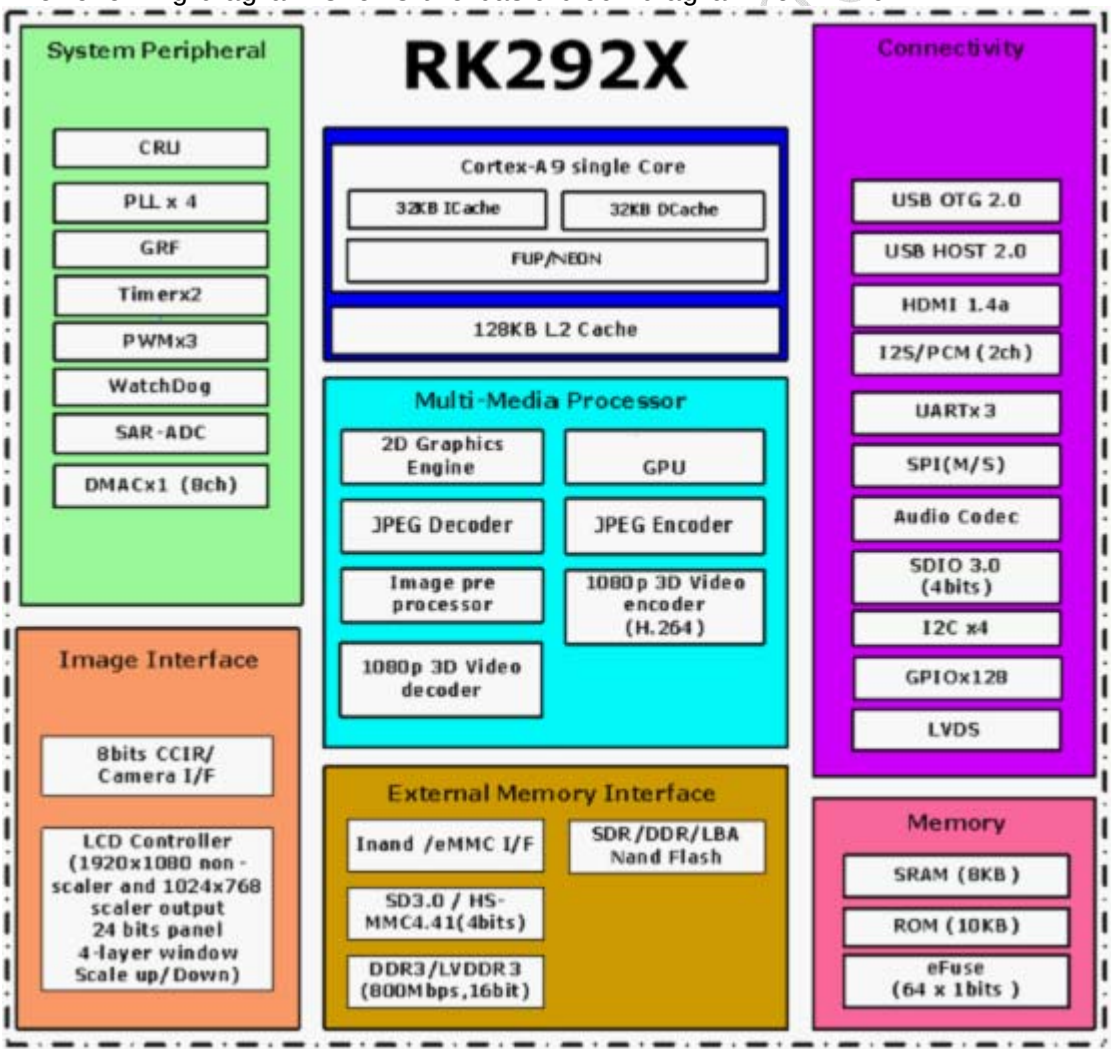


Fig 1 RK292X Block Diagram

Chapter 2 Pin Description

In this chapter, the pin description will be divided into two parts, one is all power/ground descriptions in Table 1-1, include analog power/ground, another is all the function signals descriptions in Table 1-2, also include analog power/ground.

2.1 RK292X power/ground IO descriptions

Table 2 1 RK292X Power/Ground IO informations

Group	Min(V)	Typ(V)	Max(V)	Descriptions
GND	N/A	N/A	N/A	Internal Core Ground and Digital IO Ground
AVDD	1.08	1.2	1.32	Internal CPU Power (@ cpu frequency <= 1GHz)
CVDD	1.08	1.2	1.32	Internal Core Power
VDDIO	3	3.3	3.6	Digital GPIO Power
DDR_VDD	1.4 N/A	1.5 1.35	1.6 N/A	DDR3 Digital IO Power LVDDR3 Digital IO Power
PLL_VSS1	N/A	N/A	N/A	PLL Analog Ground
PLL_VSS2	N/A	N/A	N/A	PLL Analog Ground
APLL_DVDD12	1.08	1.2	1.32	ARM PLL Analog Power
DPLL_DVDD12	1.08	1.2	1.32	DDR PLL Analog Power
CGPLL_DVDD12	1.08	1.2	1.32	CODEC/GENERAL PLL Analog Power
PLL_VCCIO	3	3.3	3.6	DDR PLL Analog Power
SAR_AVDD33	2.97	3.3	3.67	SAR-ADC Analog Power
USB_DVDD12	1.08	1.2	1.32	USB OTG2.0/Host2.0 Digital Power
USB_AVDD33	2.97	3.3	3.63	USB OTG2.0/Host2.0 Analog Power
CODEC_AVDD CODEC_AVSS	2.97 N/A	3.3 N/A	3.63 N/A	Audio Codec Analog Power Audio Codec Analog Ground
HDMI_DVDD12	1.08	1.2	1.32	HDMI Digital Power
HDMI_AVDD33	3.0	3.3	3.6	HDMI Analog Power
HDMI_VSS	N/A	N/A	N/A	HDMI Analog Ground
LVDS_DVDD12	1.08	1.2	1.32	LVDS Digital Power
LVDS_VCC	2.97	3.3	3.63	LVDS Aanlog Power

2.2 IO pin name descriptions

This sub-chapter will focus on the detailed function description of every pins based on different interface.

Table 2 2 RK292X IO function description list

Interface	Pin Name	Direction	Description
Misc	XIN24M	I	Clock input of 24MHz crystal
	XOUT24M	O	Clock output of 24MHz crystal
	NPOR	I	Power on reset for chip
Debug	TRST_N	I	JTAG interface reset input
	TCK	I	JTAG interface clock input/SWD interface clock input
	TDI	I	JTAG interface TDI input
	TMS	I/O	JTAG interface TMS input/SWD interface data out
	TDO	O	JTAG interface TDO output
SD/MMC Host Controller	sdmmc_clkout	O	sdmmc card clock.
	sdmmc_cmd	I/O	sdmmc card command output and reponse input.
	sdmmc_datai (i=0~3)	I/O	sdmmc card data input and output.
	sdmmc_detect_n	I	sdmmc card detect signal, a 0 represents presence of card.
	sdmmc_write_prt	I	sdmmc card write protect signal, a 1 represents write is protected.
	sdmmc_rstn_out	O	sdmmc card reset signal
	sdmmc_pwr_en	O	sdmmc card power-enable control signal
SDIO Host Controller	sdio_clkout	O	sdio card clock.
	sdio_cmd	I/O	sdio card command output and reponse input.
	sdio_datai (i=0~3)	I/O	sdio card data input and output.
	sdio_detect_n	I	sdio card detect signal, a 0 represents presence of card.
	sdio_write_prt	I	sdio card write protect signal, a 1 represents write is protected.
	sdio_pwr_en	O	sdio card power-enable control signal
	sdio_int_n	O	sdio card interrupt indication
	sdio_backend	O	the back-end power supply for embedded device
eMMC Interface	emmc_clkout	O	emmc card clock.
	emmc_cmd	I/O	emmc card command output and reponse input.
	emmc_datai (i=0~7)	I/O	emmc card data input and output.
	emmc_pwr_en	O	emmc card power-enable control signal
	emmc_rstn_out	O	emmc card reset signal
DMC	CLK	O	Active-high clock signal to the memory device.
	CLK_B	O	Active-low clock signal to the memory device.
	CKE	O	Active-high clock enable signal to the memory device
	CSBi (i=0,1)	O	Active-low chip select signal to the memory device. AThere are two chip select.
	RASB	O	Active-low row address strobe to the memory device.
	CASB	O	Active-low column address strobe to the memory device.
	WEB	O	Active-low write enable strobe to the memory device.
	BA[2:0]	O	Bank address signal to the memory device.
	A[15:0]	O	Address signal to the memory device.
	DQi_A(i=0~7) DQi_B(i=0~7)	I/O	Bidirectional data line to the memory device.

	DQS_A DQS_B	I/O	Active-high bidirectional data strobes to the memory device.
	DQSB_A DQSB_B	I/O	Active-low bidirectional data strobes to the memory device.
	DM_A DM_B	O	Active-low data mask signal to the memory device.
	ODTi (i=0,1)	O	On-Die Termination output signal for two chip select.
	RESETN	O	DDR3 reset signal to the memory device
NandC	flash_wp	O	Flash write-protected signal
	flash_ale	O	Flash address latch enable signal
	flash_cle	O	Flash command latch enable signal
	flash_wrn	O	Flash write enable and clock signal
	flash_rdn	O	Flash read enable and write/read signal
	flash_data[i](i=0~7)	I/O	8bits of flash data inputs/outputs signal
	flash_dqs	I/O	Flash data strobe signal
	flash_rdy	I	Flash ready/busy signal
	flash_csni(i=0~3)	O	Flash chip enable signal for chip i, i=0~3
I2S/PCM Controller (2 channel)	i2s_clk	O	I2S/PCM clock source
	i2s_sclk	I/O	I2S/PCM serial clock
	i2s_lrck_rx	I/O	I2S/PCM left & right channel signal for receiving serial data, synchronous left & right channel in I2S mode and the beginning of a group of left & right channels in PCM mode
	i2s_sdi	I	I2S/PCM serial data input
	i2s_sdo	O	I2S/PCM serial data ouput
	i2s_lrck_tx	I/O	I2S/PCM left & right channel signal for transmitting serial data, synchronous left & right channel in I2S mode and the beginning of a group of left & right channels in PCM mode
SPI Controller	spi_clk	I/O	spi serial clock
	spi_csny (y=0,1)	I/O	spi chip select signal, low active
	spi_txd	O	spi serial data output
	spi_rxd	I	spi serial data input
LCDC	lcdc_dclk	O	LCDC RGB interface display clock out, MCU i80 interface RS signal
	lcdc_vsync	O	LCDC RGB interface vertival sync pulse, MCU i80 interface CSN signal
	lcdc_hsync	O	LCDC RGB interface horizontial sync pulse, MCU i80 interface WEN signal
	lcdc_den	O	LCDC RGB interface data enable, MCU i80 interface REN signal
	lcdc_data[23:0]	I/O	LCDC data output/input
Camera IF	cif_clkin	I	Camera interface input pixel clock
	cif_clkout	O	Camera interface output work clock
	cif_vsync	I	Camera interface vertical sync signal
	cif_href	I	Camera interface horizontial sync signal
	cif_data[7:0]	I	Camera interface 8-bit input pixel data
GPS	gps_sign	I	GPS sign data input
	gps_mag	I	GPS mag data input
	gps_clk	I	GPS rf clock input
PWM	Pwm2	O	Pulse Width Modulation output
	pwm1	O	Pulse Width Modulation output
	pwm0	O	Pulse Width Modulation output
I2C	i2c0_sda	I/O	I2C0 data
	i2c0_scl	I/O	I2C0 clock

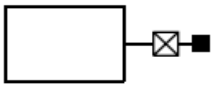
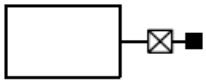
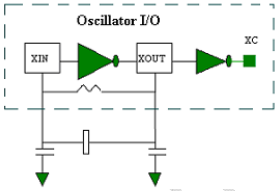
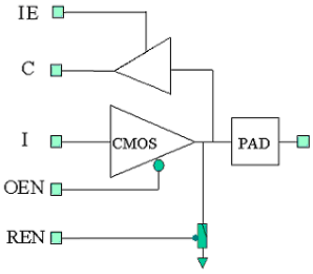
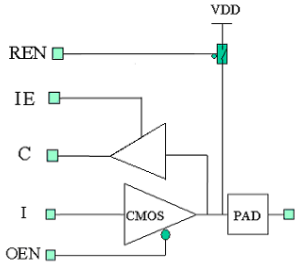
	i2c1_sda	I/O	I2C1 data
	i2c1_scl	I/O	I2C1 clock
	i2c2_sda	I/O	I2C2 data
	i2c2_scl	I/O	I2C2 clock
	i2c3_sda	I/O	I2C3 data
	i2c3_scl	I/O	I2C3 clock
UART	uart0_sin	I	UART0 searial data input
	uart0_sout	O	UART0 searial data output
	uart0_cts_n	I	UART0 clear to send
	uart0_rts_n	O	UART0 request to send
	uart1_sin	I	UART1 searial data input
	uart1_sout	O	UART1 searial data output
	uart1_cts_n	O	UART1 clear to send
	uart1_rts_n	I	UART1 request to send
	uart2_sin	I	UART2 searial data input
	uart2_sout	O	UART2 searial data output
USB OTG2.0 /HOST 2.0	USB0PP	I/O	USB OTG 2.0 Data signal DP
	USB0PN	I/O	USB OTG 2.0 Data signal DM
	VBUS_0	N/A	USB OTG 2.0 5V power supply pin
	USB0ID	I	USB OTG 2.0 ID indicator
	otg_drv_vbus	O	USB OTG 2.0 drive VBUS
	USB1PP	I/O	USB HOST 2.0 Data signal DP
	USB1PN	I/O	USB HOST 2.0 Data signal DM
	VBUS_1	N/A	USB HOST 2.0 5V power supply pin
	USB1ID	I	USB HOST 2.0 ID indicator
	USBRBIAS	N/A	45 Ohm Reference external resistance
LVDS	Dn_m	I	Transmit parallel data in, n=1~4,m=0~6
	OEN	I	Output enable pin (Active Low)
	PDN	I	Transmitter power down enable pin(Active Low)
	CK_REF	I	Input clock
	DSn	I	Output loading selection, n=0~1
	PD_PLL	I	PLL Power down enable pin(Active High)
	PDN_CBG	I	CBG Power down enable pin (Active Low)
	XRES	I	Connected to external 12Komh through bonding pad
	PADP_n	O	Transmit serial data out, n=1~4
	PADN_n	O	Transmit serial data out(Negative), n=1~4
	CLKP	O	Output clock
	CLKN	O	Output clock(Negative)
	Tn	I	TTL data input, n=1~10
Audio Codec	MICL	I	Left channel microphone PGA positive input
	LINEL	I	Left channel line-in input
	VCM	I	Decoupling for voltage reference
	VREF_MIC	O	Microphone bias voltage output
	LINER	I	Right channel line-in input
	MICR	I	Right channel microphone PGA positive input
	VOUTL	O	Left channel DAC driver amplifier output
	VOUTR	O	Right channel DAC driver amplifier output
HDMI	EXTR	O	Connect 2.0Kohm resistor to ground to generate reference current

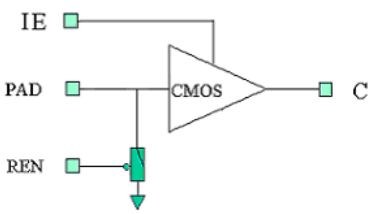
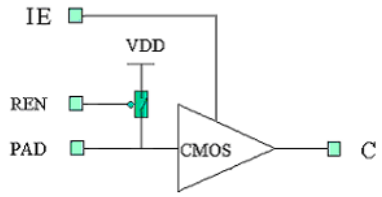
	TX3N	O	TMDS negative clock line
	TX3P	O	TMDS positive clock line
	TX0N	O	TMDS channel 0 negative data line
	TX0P	O	TMDS channel 0 positive data line
	TX1N	O	TMDS channel 1 negative data line
	TX1P	O	TMDS channel 1 positive data line
	TX2N	O	TMDS channel 2 negative data line
	TX2P	O	TMDS channel 2 positive data line
SAR-ADC	SARADC_AIN[i] (i=0~2)	N/A	SAR-ADC input signal for 3 channel
eFuse	EFUSE_VP	N/A	eFuse program and sense power

1.3 2.3 RK292x IO Type

The following list shows IO type except DDR IO and all of Power/Ground IO .

Table 2 3 RK292x IO Type List

	Diagram	Description	Pin Name
A		Analog IO Cell with IO voltage	EFUSE_VP
B		Dedicated Power supply to Internal Macro with IO voltage	SARADC_AIN[2:0]
C		Crystal Oscillator with internal register	XIN24M/XOUT24M
D		CMOS 3-state output pad with controllable input and controllable pulldown	Part of digital GPIO (PBCDxRN)
E		CMOS 3-state output pad with controllable input and controllable pullup	Part of digital GPIO (PBCUxRN)

F		controllable input pad with controllable pulldown	Part of digital GPIO (PICDRN)
G		controllable input pad with controllable pullup	Part of digital GPIO (PICURN)

Chapter 3 Package information

RK292X has two type of package:
RK2926 is eLQFP176: (body: 20mm x 20mm ; pin pitch : 0.4mm)
RK2928G is TBGA313: (body: 16mm x 16mm ; ball size : 0.4mm ; ball pitch : 0.8mm)

3.1 RK2928G Ball Map

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	
A	DDR_BA2	DDR_CSN1	DDR_CASN	DDR_CLK	DDR_ODT0	DDR_BA1	DDR_A11	DDR_A14	DDR_DM0	DDR_DQ4	DDR_DQS0	CODEC_AOL	CODEC_AVDD	CODEC_AIL	GPIO3_D1	GPIO3_D4	HDMI_CEC/GPIO0_C4	UART0_RX/GPIO0_C1	UART0_TX/GPIO0_C0	A
B	DDR_A3	DDR_WEN	DDR_RASN	DDR_CLK_N	DDR_CKE	DDR_A12	DDR_A15	DDR_A6	DDR_DQ1	DDR_DQ6	DDR_DQS0_N	CODEC_AOR	CODEC_AVSS	CODEC_MICL	I2C3_SDA/HDMI_SDA/GPIO0_A7	GPIO3_D3	GPIO3_D6	UART0_RTSN/GPIO0_C2	UART0_CTSN/GPIO0_C3	B
C	DDR_A0	DDR_A2	DDR_CSN0	VSS	DDR_A10	DDR_A4		DDR_A8	DDR_DQ5		DDR_DQ2	CODEC_AIR		CODEC_MICBIAS	I2C3_SCL/HDMI_SCL/GPIO0_A6	GPIO3_D2	GPIO3_D5	GPIO0_C6	UART2_RTSN/GPIO0_D0	C
D	DDR_A5	DDR_A9	DDR_A13		DDR_BA0	DDR_A1		DDR_DQ3	DDR_DQ7		DDR_DQ0	CODEC_MICR		CODEC_VCM	HDMI_HPD/GPIO0_B7		UART2_CTSN/GPIO0_D1	GPIO0_C5	SDMMC0_WP/GPIO1_A7	D
E	DDR_A7	DDR_ODT1	DDR_RESETN	DDR_DQ10		DDR_VDD		CVDD	DDR_VDD		DDR_VDD	VSS		VSS		SPI_CSN1/GPIO1_B4	SDMMC1_PWR/GPIO0_D6	I2C0_SCL/GPIO0_A0	I2C0_SDA/GPIO0_A1	E
F	DDR_DQS1	DDR_DQS1_N	DDR_DQ8	DDR_DQ14	DDR_VDD		VSS	VSS	VSS	VSS	VSS	VSS	VSS		JTAG_TDO	JTAG_TMS	SDMMC0_CMD/GPIO1_B7	I2C1_SDA/GPIO0_A3	I2C1_SCL/GPIO0_A2	F
G	DDR_DQ12	DDR_DQ15				VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VCCIO				I2S_SCLK/GPIO1_A1	I2S_MCLK/GPIO1_A0	G
H	DDR_DQ13	DDR_DQ9	DDR_DM1	DDR_DQ11	DDR_VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	JTAG_TDI	I2S_SDI/GPS_SIGN/GPIO1_A5	I2S_SDO/GPS_MAG/GPIO1_A4	I2S_LRCK_TX/GPIO1_A3	I2S_LRCK_RX/GPS_CLK/GPIO1_A2	H
J	LCDC_D16/GPIO2_C2	LCDC_D17/GPIO2_C3	LCDC_D19/I2C2_SCL/GPIO2_C5	LCDC_D18/I2C2_SDA/GPIO2_C4	C/GPLL_DVDD12	CVDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	JTAG_TCK	SPI_RXD/UART1_RX/GPIO1_B2	SPI_TXD/UART1_TX/GPIO1_B1	GPIO3_C0	SPI_CLK/UART1_CTSN/GPIO1_B0	J

K	XOUT24M	XIN24M					PLL_VSS1	VSS	VSS	VSS	VSS	VSS	VSS	VSS	CVDD					GPIO3_C3	GPIO3_C2	K
L	LCDC_D15/GPIO2_C1	LCDC_D21/UART2_TX/GPIO2_C7	LCDC_D20/UART2_RX/GPIO2_C6	LCDC_D13/GPIO2_B7	APLL_DVDD12	PLL_VSS2	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VCCIO	TEST	GPIO3_C5	SDMMC0_CLKO/GPIO1_C0	SPI_CSN0/UART1_RTSN/GPIO1_B3	GPIO3_C4	L
M	LCDC_D14/GPIO2_C0	LCDC_D23/GPIO2_D1	LCDC_D22/GPIO2_D0	LCDC_D12/GPIO2_B6	DPLL_DVDD12	PLL_VCCIO	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	JTAG_RSTN	SDMMC1_CLKO/GPIO0_B1	SDMMC1_CMD/GPIO0_B0	GPIO3_C7	GPIO3_C6	M
N	LCDC_D10/GPIO2_B4	LCDC_D11/GPIO2_B5				VCCIO	VSS	VSS	VSS	VSS	VSS	VSS	VSS	AVDD				SDMMC1_D1/GPIO0_B4	SDMMC1_D0/GPIO0_B3	N
P	HDMI_TX3P	HDMI_TX3N	HDMI_VSS	LCDC_DEN/GPIO2_B3	LCDC_HSYNC/GPIO2_B1		LVDS_VCC	USB_DVDD12	USB_AVDD33	SAR_AVDD33	CVDD	VCCIO	AVDD		AVDD	TEST_CLKO/GPIO3_D7	SDMMC0_DET/GPIO1_C1	SDMMC1_D3/GPIO0_B6	SDMMC1_D2/GPIO0_B5	P
R	HDMI_TX0P	HDMI_TX0N	HDMI_VSS	LCDC_CLK/GPIO2_B0		LCDC_VSYNC/GPIO2_B2		EFUSE	ADCIN2		CIF_D4	PWM2/GPIO0_D4		AVDD		SDMMC0_D3/GPIO1_C5	SDMMC0_D2/GPIO1_C4	SDMMC0_D1/GPIO1_C3	SDMMC0_D0/GPIO1_C2	R
T	HDMI_TX1P	HDMI_TX1N	HDMI_VSS		HDMI_DVDD12	LVDS_DVDD12		USB0_VBUS	ADCIN1		CIF_D5	CIF_HREF		AVDD	FLASH_CS3/EMMC_RST/GPIO1_C7		FLASH_D6/EMMC_D6/GPIO1_D6	FLASH_WRN/GPIO2_A2	NPOR	T
U	HDMI_TX2P	HDMI_TX2N	HDMI_VSS	HDMI_AVDD33	HDMI_EXTR	USB_RBIAS		USB0_ID	ADCIN0		CIF_D6	CIF_CLKO		PWM1/GPIO0_D3	FLASH_CS2/EMMC_CMD/GPIO1_C6	FLASH_D3/EMMC_D3/GPIO1_D3	FLASH_D7/EMMC_D7/GPIO1_D7	FLASH_RDN/GPIO2_A3	SDMMC0_PWR/GPIO1_B6	U
V	LVDS_TX3P/LCDC_D6	LVDS_CLKP/LCDC_D8	LVDS_TX2P/LCDC_D4	LVDS_TX1P/LCDC_D2	LVDS_TX0P/LCDC_D0	VSS	USB1_DN	USB0_DN	CIF_D0	CIF_D2	CIF_D7	CIF_CLKI	GPIO3_B3/CIF_PDN1	FLASH_WP/EMMC_PWR/GPIO2_A5	FLASH_D1/EMMC_D1/GPIO1_D1	FLASH_D4/EMMC_D4/GPIO1_D4	FLASH_ALE/GPIO2_A0	FLASH_RDY/GPIO2_A4	FLASH_DQS/EMMC_CLKO/GPIO2_A7	V
W	LVDS_TX3N/LCDC_D7	LVDS_CLKN/LCDC_D9	LVDS_TX2N/LCDC_D5	LVDS_TX1N/LCDC_D3	LVDS_TX0N/LCDC_D1	LVDS_XRES	USB1_DP	USB0_DP	CIF_D1	CIF_D3	CIF_VSYNC	DRIVE_VBUS/GPIO3_C1/CIF_PDN0	PWM0/GPIO0_D2	FLASH_D0/EMMC_D0/GPIO1_D0	FLASH_D2/EMMC_D2/GPIO1_D2	FLASH_D5/EMMC_D5/GPIO1_D5	FLASH_CLE/GPIO2_A1	FLASH_CS0/GPIO2_A6	FLASH_CS1/GPIO0_C7	W
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	

Fig 2 TFBGA313 Ball Map

3.2 RK2928G function IO descriptions

Table 3 1 RK2928G IO descriptions

Ball Name	Ball #	func2	func3	func4	pad① type	driving ②	Pull up /down	Reset State ③
DDR_A5	D1				O	N/A	N/A	O
DDR_A9	D2				O	N/A	N/A	O
DDR_A13	D3				O	N/A	N/A	O
DDR_A7	E1				O	N/A	N/A	O
DDR_ODT1	E2				O	N/A	N/A	O
DDR_RESETN	E3				O	N/A	N/A	O
DDR_DQ10	E4				I/O	N/A	N/A	I
DDR_DQ8	F3				I/O	N/A	N/A	I
DDR_DQS1	F1				I/O	N/A	N/A	I
DDR_DQS1_N	F2				I/O	N/A	N/A	I
DDR_DQ14	F4				I/O	N/A	N/A	I
DDR_DQ12	G1				I/O	N/A	N/A	I
DDR_DQ15	G2				I/O	N/A	N/A	I
DDR_DQ13	H1				I/O	N/A	N/A	I
DDR_DQ9	H2				I/O	N/A	N/A	I
DDR_DM1	H3				I/O	N/A	N/A	I
DDR_DQ11	H4				I/O	N/A	N/A	I
XOUT24M	K1				O	N/A	N/A	O
XIN24M	K2				I	N/A	N/A	I
LCDC_D20/UART2_RX/GPIO2_C6	L3	lcdc0_d20	lcdc1_d20	urt2_sin	I/O	8	down	I
LCDC_D21/UART2_TX/GPIO2_C7	L2	lcdc0_d21	lcdc1_d21	urt2_sout	I/O	8	down	I
LCDC_D19/I2C2_SCL/GPIO2_C5	J3	lcdc0_d19	lcdc1_d19	i2c2_scl	I/O	8	down	I
LCDC_D18/I2C2_SDA/GPIO2_C4	J4	lcdc0_d18	lcdc1_d18	i2c2_sda	I/O	8	down	I
LCDC_D17/GPIO2_C3	J2	lcdc0_d17	lcdc1_d17		I/O	8	down	I
LCDC_D16/GPIO2_C2	J1	lcdc0_d16	lcdc1_d16		I/O	8	down	I
LCDC_D15/GPIO2_C1	L1	lcdc0_d15	lcdc1_d15		I/O	8	down	I
LCDC_D14/GPIO2_C0	M1	lcdc0_d14	lcdc1_d14		I/O	8	down	I
LCDC_D23/GPIO2_D1	M2	lcdc0_d23	lcdc1_d23		I/O	8	down	I
LCDC_D22/GPIO2_D0	M3	lcdc0_d22	lcdc1_d22		I/O	8	down	I
LCDC_D13/GPIO2_B7	L4	lcdc0_d13	lcdc1_d13		I/O	8	down	I
LCDC_D12/GPIO2_B6	M4	lcdc0_d12	lcdc1_d12		I/O	8	down	I
LCDC_D11/GPIO2_B5	N2	lcdc0_d11	lcdc1_d11		I/O	8	down	I
LCDC_D10/GPIO2_B4	N1	lcdc0_d10	lcdc1_d10		I/O	8	down	I
LCDC_DEN/GPIO2_B3	P4	lcdc0_den	lcdc1_den		I/O	8	down	I
LCDC_VSYNC/GPIO2_B2	R6	lcdc0_vsync	lcdc1_vsync		I/O	8	down	I
LCDC_HSYNC/GPIO2_B1	P5	lcdc0_hsync	lcdc1_hsync		I/O	8	down	I
LCDC_CLK/GPIO2_B0	R4	lcdc0_dclk	lcdc1_dclk		I/O	12	down	I
HDMI_EXTR	U5				A	N/A	N/A	N/A
HDMI_TX3N	P2				A	N/A	N/A	N/A
HDMI_TX3P	P1				A	N/A	N/A	N/A
HDMI_TX0N	R2				A	N/A	N/A	N/A
HDMI_TX0P	R1				A	N/A	N/A	N/A
HDMI_TX1N	T2				A	N/A	N/A	N/A
HDMI_TX1P	T1				A	N/A	N/A	N/A
HDMI_TX2N	U2				A	N/A	N/A	N/A
HDMI_TX2P	U1				A	N/A	N/A	N/A
LVDS_XRES	W6				A	N/A	N/A	N/A
LVDS_CLKN/LCDC_D9	W2	lvds_clkn	lcdc0_d9		A	N/A	N/A	N/A

LVDS_CLKP/LCDC_D8	V2	lvds_clkp	lcdc0_d8		A	N/A	N/A	N/A
LVDS_TX3N/LCDC_D7	W1	lvds_n3	lcdc0_d7		A	N/A	N/A	N/A
LVDS_TX3P/LCDC_D6	V1	lvds_p3	lcdc0_d6		A	N/A	N/A	N/A
LVDS_TX2N/LCDC_D5	W3	lvds_n2	lcdc0_d5		A	N/A	N/A	N/A
LVDS_TX2P/LCDC_D4	V3	lvds_p2	lcdc0_d4		A	N/A	N/A	N/A
LVDS_TX1N/LCDC_D3	W4	lvds_n1	lcdc0_d3		A	N/A	N/A	N/A
LVDS_TX1P/LCDC_D2	V4	lvds_p1	lcdc0_d2		A	N/A	N/A	N/A
LVDS_TX0N/LCDC_D1	W5	lvds_n0	lcdc0_d1		A	N/A	N/A	N/A
LVDS_TX0P/LCDC_D0	V5	lvds_p0	lcdc0_d0		A	N/A	N/A	N/A
USB1_DP	W7				A	N/A	N/A	N/A
USB1_DM	V7				A	N/A	N/A	N/A
USB_RBIAS	U6				A	N/A	N/A	N/A
USB0_VBUS	T8				A	N/A	N/A	N/A
USB0_ID	U8				A	N/A	N/A	N/A
USB0_DM	V8				A	N/A	N/A	N/A
USB0_DP	W8				A	N/A	N/A	N/A
ADCIN0	U9				A	N/A	N/A	N/A
ADCIN1	T9				A	N/A	N/A	N/A
ADCIN2	R9				A	N/A	N/A	N/A
EFUSE	R8				A	N/A	N/A	N/A
CIF_D0	V9				I	N/A	down	I
CIF_D1	W9				I	N/A	down	I
CIF_D2	V10				I	N/A	down	I
CIF_D3	W10				I	N/A	down	I
CIF_D4	R11				I	N/A	down	I
CIF_D5	T11				I	N/A	down	I
CIF_D6	U11				I	N/A	down	I
CIF_D7	V11				I	N/A	down	I
CIF_VSYNC	W11				I	N/A	down	I
CIF_HREF	T12				I	N/A	down	I
CIF_CLKI	V12				I	N/A	down	I
CIF_CLKO	U12				I/O	4	down	I
DRIVE_VBUS/GPIO3_C1/CIF_PDN0	W12	drive_vbus			I/O	4	down	I
GPIO3_B3/CIF_PDN1	V13				I/O	4	up	I
PWM0/GPIO0_D2	W13	pwm_0			I/O	4	down	I
PWM1/GPIO0_D3	U14	pwm_1			I/O	4	down	I
PWM2/GPIO0_D4	R12	pwm_2			I/O	4	up	I
FLASH_WP/EMMC_PWR/GPIO2_A5	V14	nand_wp	emmc_pwren		I/O	8	down	I
FLASH_CS2/EMMC_CMD/GPIO1_C6	U15	nand_cs2	emmc_cmd		I/O	4	up	I
FLASH_CS3/EMMC_RST/GPIO1_C7	T15	nand_cs3	emmc_rstnout		I/O	4	up	I
FLASH_D0/EMMC_D0/GPIO1_D0	W14	nand_d0	emmc_d0		I/O	8	up	I
FLASH_D1/EMMC_D1/GPIO1D1	V15	nand_d1	emmc_d1		I/O	8	up	I
FLASH_D2/EMMC_D2/GPIO1D2	W15	nand_d2	emmc_d2		I/O	8	up	I
FLASH_D3/EMMC_D3/GPIO1_D3	U16	nand_d3	emmc_d3		I/O	8	up	I
FLASH_D4/EMMC_D4/GPIO1_D4	V16	nand_d4	emmc_d4		I/O	8	up	I
FLASH_D5/EMMC_D5/GPIO1D5	W16	nand_d5	emmc_d5		I/O	8	up	I
FLASH_D6/EMMC_D6/GPIO1_D6	T17	nand_d6	emmc_d6		I/O	8	up	I
FLASH_D7/EMMC_D7/GPIO1_D7	U17	nand_d7	emmc_d7		I/O	8	up	I
FLASH_ALE/GPIO2_A0	V17	nand_ale			I/O	8	down	I
FLASH_CLE/GPIO2_A1	W17	nand_cle			I/O	8	down	I
FLASH_WRN/GPIO2_A2	T18	nand_wrn			I/O	8	up	I
FLASH_RDN/GPO2_A3	U18	nand_rdn			I/O	8	up	I
FLASH_RDY/GPIO2_A4	V18	nand_rdy			I/O	8	up	I

FLASH_CS0/GPIO2_A6	W18	nand_cs0			I/O	8	up	I
FLASH_DQS/EMMC_CLKO/GPIO2_A7	V19	nand_dqs	emmc_clkout		I/O	8	up	I
FLASH_CS1/GPIO0_C7	W19	nand_cs1			I/O	4	up	I
TEST	L15				I	N/A	down	I
JTAG_RSTN	M15				I	N/A	down	I
JTAG_TCK	J15				I	N/A	down	I
JTAG_TDI	H15				I	N/A	up	I
JTAG_TDO	F15				I/O	4	down	I
JTAG_TMS	F16				I/O	4	down	I
SDMMC0_PWR/GPIO1_B6	U19	mmc0_pwren			I/O	4	down	I
NPOR	T19				I	N/A	down	I
SDMMC0_D3/GPIO1_C5	R16	mmc0_d3			I/O	4	up	I
SDMMC0_D2/GPIO1_C4	R17	mmc0_d2			I/O	4	up	I
SDMMC0_D1/GPIO1_C3	R18	mmc0_d1			I/O	4	up	I
SDMMC0_D0/GPIO1_C2	R19	mmc0_d0			I/O	4	up	I
SDMMC0_DET/GPIO1_C1	P17	mmc0_detn			I/O	4	up	I
SDMMC1_D3/GPIO0_B6	P18	mmc1_d3			I/O	4	up	I
TEST_CLKO/GPIO3_D7	P16	testclk_out			I/O	4	down	I
SDMMC1_D2/GPIO0_B5	P19	mmc1_d2			I/O	4	up	I
SDMMC1_D1/GPIO0_B4	N18	mmc1_d1			I/O	4	up	I
SDMMC1_D0/GPIO0_B3	N19	mmc1_d0			I/O	4	up	I
SDMMC1_CLKO/GPIO0_B1	M16	mmc1_clkout			I/O	4	up	I
SDMMC1_CMD/GPIO0_B0	M17	mmc1_cmd			I/O	4	up	I
GPIO3_C7	M18				I/O	4	up	I
GPIO3_C6	M19				I/O	4	up	I
GPIO3_C5	L16				I/O	4	down	I
SDMMC0_CLKO/GPIO1_C0	L17	mmc0_clkout			I/O	4	down	I
GPIO3_C4	L19				I/O	4	down	I
SPI_CSN0/UART1_RTSN/GPIO1_B3	L18	spi_csn0	uart1_rtsn		I/O	4	up	I
GPIO3_C3	K18				I/O	4	down	I
SPI_RXD/UART1_RX/GPIO1_B2	J16	spi_rxd	uart1_sin		I/O	4	down	I
GPIO3_C2	K19				I/O	4	down	I
SPI_TXD/UART1_TX/GPIO1_B1	J17	spi_txd	uart1_sout		I/O	4	down	I
GPIO3_C0	J18				I/O	4	down	I
SPI_CLK/UART1_CTSN/GPIO1_B0	J19	spi_clk	uart1_ctsn		I/O	4	down	I
I2S_SDI/GPS_SIGN/GPIO1_A5	H16	i2s_sdi	gps_sign		I/O	4	down	I
I2S_SDO/GPS_MAG/GPIO1_A4	H17	i2s_sdo	gps_mag		I/O	4	down	I
I2S_LRCK_TX/GPIO1_A3	H18	i2s_lrcktx			I/O	4	down	I
I2S_LRCK_RX/GPS_CLK/GPIO1_A2	H19	i2s_lrckrx	gps_clk		I/O	4	down	I
I2S_SCLK/GPIO1_A1	G18	i2s_sclk			I/O	4	down	I
I2S_MCLK/GPIO1_A0	G19	i2s_mclk			I/O	4	down	I
SDMMC0_CMD/GPIO1_B7	F17	mmc0_cmd			I/O	4	up	I
I2C1_SDA/GPIO0_A3	F18	i2c1_tpsda			I/O	4	up	I
I2C1_SCL/GPIO0_A2	F19	i2c1_tpscl			I/O	4	up	I
I2C0_SDA/GPIO0_A1	E19	i2c0_pmusda			I/O	4	up	I
I2C0_SCL/GPIO0_A0	E18	i2c0_pmuscl			I/O	4	up	I
SPI_CSN1/GPIO1_B4	E16	spi_csn1			I/O	4	up	I
SDMMC0_WP/GPIO1_A7	D19	mmc0_wrprt			I/O	4	down	I
SDMMC1_PWR/GPIO0_D6	E17	mmc1_pwren			I/O	4	down	I
UART2_CTSN/GPIO0_D1	D17	urt2_ctsn			I/O	4	up	I
UART2_RTSN/GPIO0_D0	C19	urt2_rtsn			I/O	4	up	I
GPIO0_C6	C18				I/O	4	up	I
GPIO0_C5	D18				I/O	4	up	I
HDMI_CEC/GPIO0_C4	A17	hdmi_cecsda			I/O	4	up	I

UART0_CTSN/GPIO0_C3	B19	urt0_ctsn			I/O	4	up	I
UART0_RTSN/GPIO0_C2	B18	urt0_rtsn			I/O	4	up	I
UART0_RX/GPIO0_C1	A18	urt0_sin			I/O	4	up	I
UART0_TX/GPIO0_C0	A19	urt0_sout			I/O	4	down	I
GPIO3_D6	B17				I/O	4	down	I
GPIO3_D5	C17				I/O	4	down	I
GPIO3_D4	A16				I/O	4	down	I
GPIO3_D3	B16				I/O	4	up	I
GPIO3_D2	C16				I/O	4	up	I
GPIO3_D1	A15				I/O	4	up	I
I2C3_SDA/HDMI_SDA/GPIO0_A7	B15	i2c3_cifsda	hdmi_ddcsda		I/O	4	up	I
I2C3_SCL/HDMI_SCL/GPIO0A6	C15	i2c3_cifscl	hdmi_ddcscl		I/O	4	up	I
HDMI_HPD/GPIO0_B7	D15	hdmi_hotplugin			I/O	4	down	I
CODEC_MICL	B14				A	N/A	N/A	N/A
CODEC_AIL	A14				A	N/A	N/A	N/A
CODEC_VCM	D14				A	N/A	N/A	N/A
CODEC_MICBIAS	C14				A	N/A	N/A	N/A
CODEC_AIR	C12				A	N/A	N/A	N/A
CODEC_MICR	D12				A	N/A	N/A	N/A
CODEC_AOL	A12				A	N/A	N/A	N/A
CODEC_AOR	B12				A	N/A	N/A	N/A
DDR_DQ2	C11				I/O	N/A	N/A	I
DDR_DQ0	D11				I/O	N/A	N/A	I
DDR_DQS0	A11				I/O	N/A	N/A	I
DDR_DQS0_N	B11				I/O	N/A	N/A	I
DDR_DQ6	B10				I/O	N/A	N/A	I
DDR_DQ4	A10				I/O	N/A	N/A	I
DDR_DQ7	D9				I/O	N/A	N/A	I
DDR_DQ5	C9				I/O	N/A	N/A	I
DDR_DQ1	B9				I/O	N/A	N/A	I
DDR_DM0	A9				I/O	N/A	N/A	I
DDR_DQ3	D8				I/O	N/A	N/A	I
DDR_A8	C8				O	N/A	N/A	O
DDR_A6	B8				O	N/A	N/A	O
DDR_A14	A8				O	N/A	N/A	O
DDR_A15	B7				O	N/A	N/A	O
DDR_A11	A7				O	N/A	N/A	O
DDR_A1	D6				O	N/A	N/A	O
DDR_A4	C6				O	N/A	N/A	O
DDR_A12	B6				O	N/A	N/A	O
DDR_BA1	A6				O	N/A	N/A	O
DDR_BA0	D5				O	N/A	N/A	O
DDR_A10	C5				O	N/A	N/A	O
DDR_CKE	B5				O	N/A	N/A	O
DDR_ODT0	A5				O	N/A	N/A	O
DDR_CLK_N	B4				O	N/A	N/A	O
DDR_CLK	A4				O	N/A	N/A	O
DDR_RASN	B3				O	N/A	N/A	O
DDR_CASN	A3				O	N/A	N/A	O
DDR_CSN1	A2				O	N/A	N/A	O
DDR_CSN0	C3				O	N/A	N/A	O
DDR_WEN	B2				G	N/A	N/A	O
DDR_BA2	A1				O	N/A	N/A	O
DDR_A3	B1				O	N/A	N/A	O

Notes :

①: *Pad types : I = input , O = output , I/O = input/output (bidirectional) ,*
AP = Analog Power , AG = Analog Ground
DP = Digital Power , DG = Digital Ground
A = Analog

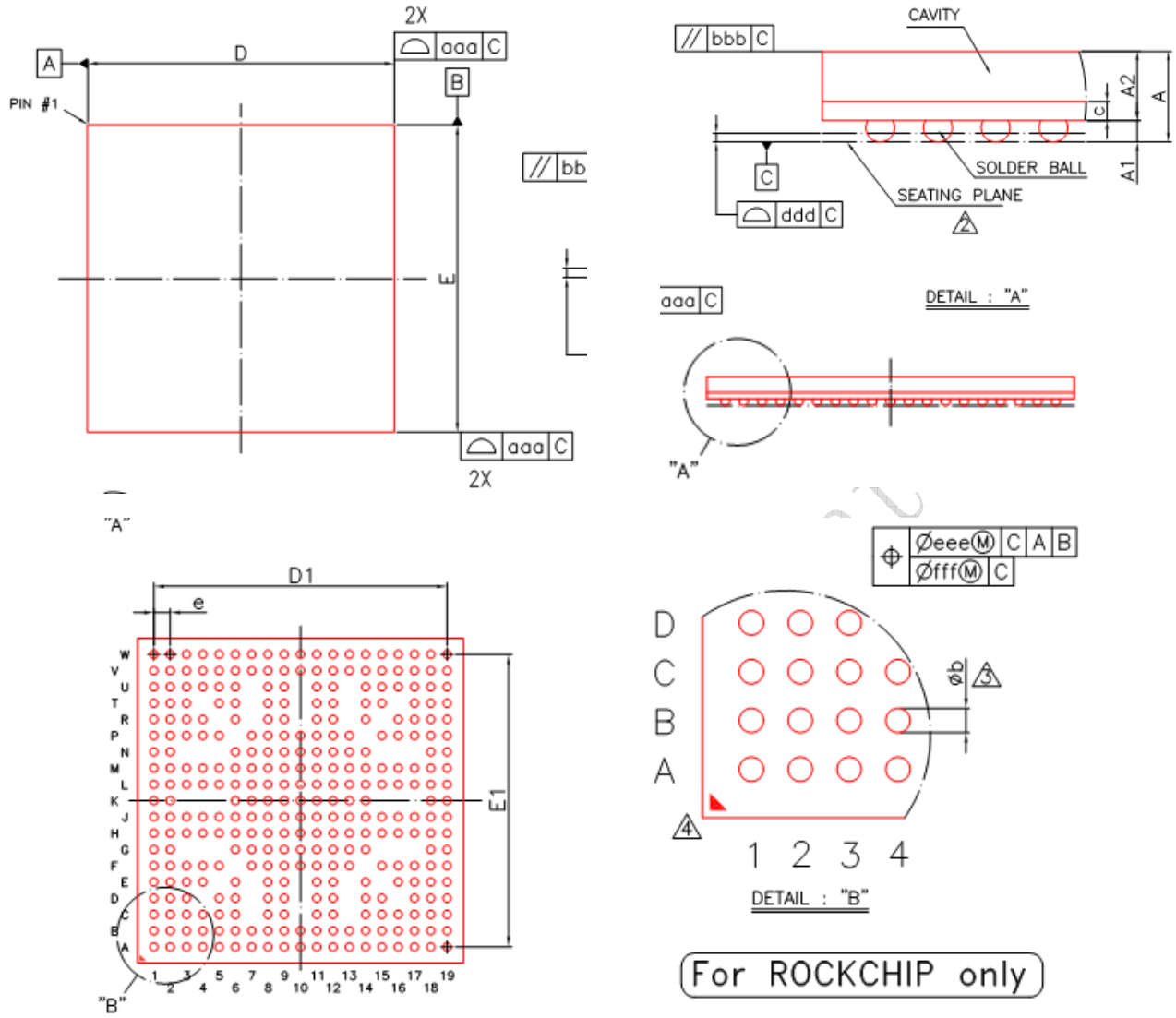
②: *Output Drive Unit is mA , only Digital IO have drive value*

③: *Reset state : I = input without any pull resistor , O = output without any pull resistor ,*

④ : *It is die location. For examples, "Left side" means that all the related IOs are always in left side of die*

⑤ : *Power supply means that all the related IOs is in these IO power domain. If multiple powers is included, they are connected together in one IO power ring*

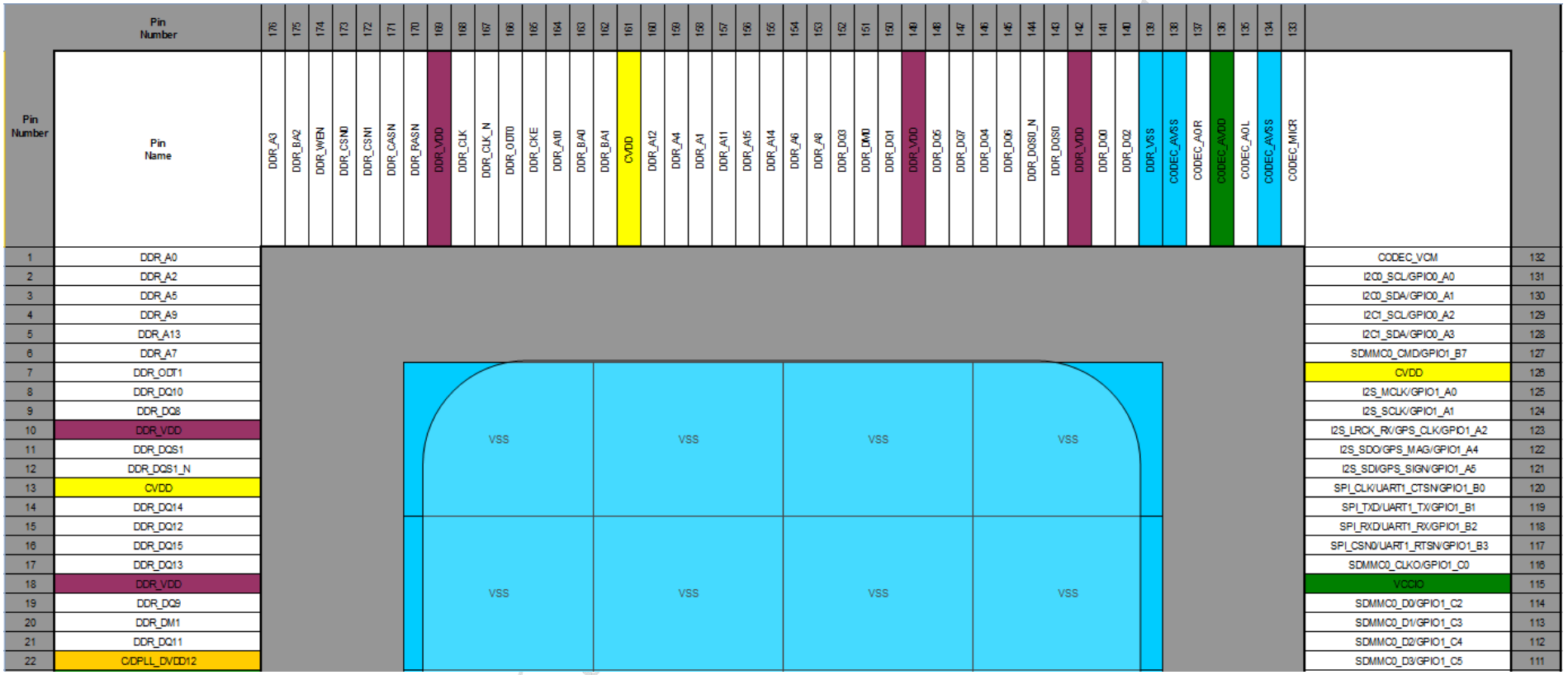
3.3 RK2928G Dimension



Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.40	---	---	0.055
A1	0.25	0.30	0.35	0.010	0.012	0.014
A2	0.91	0.96	1.01	0.036	0.038	0.040
c	0.22	0.26	0.30	0.009	0.010	0.012
D	15.90	16.00	16.10	0.626	0.630	0.634
E	15.90	16.00	16.10	0.626	0.630	0.634
D1	---	14.40	---	---	0.567	---
E1	---	14.40	---	---	0.567	---
e	---	0.80	---	---	0.031	---
b	0.35	0.40	0.45	0.014	0.016	0.018
aaa	0.15			0.006		
bbb	0.15			0.006		
ddd	0.13			0.005		
eee	0.15			0.006		
fff	0.08			0.003		
MD/ME	19/19			19/19		

Fig 3 RK2928G Package Dimension

3.4 RK2926 Ball Map



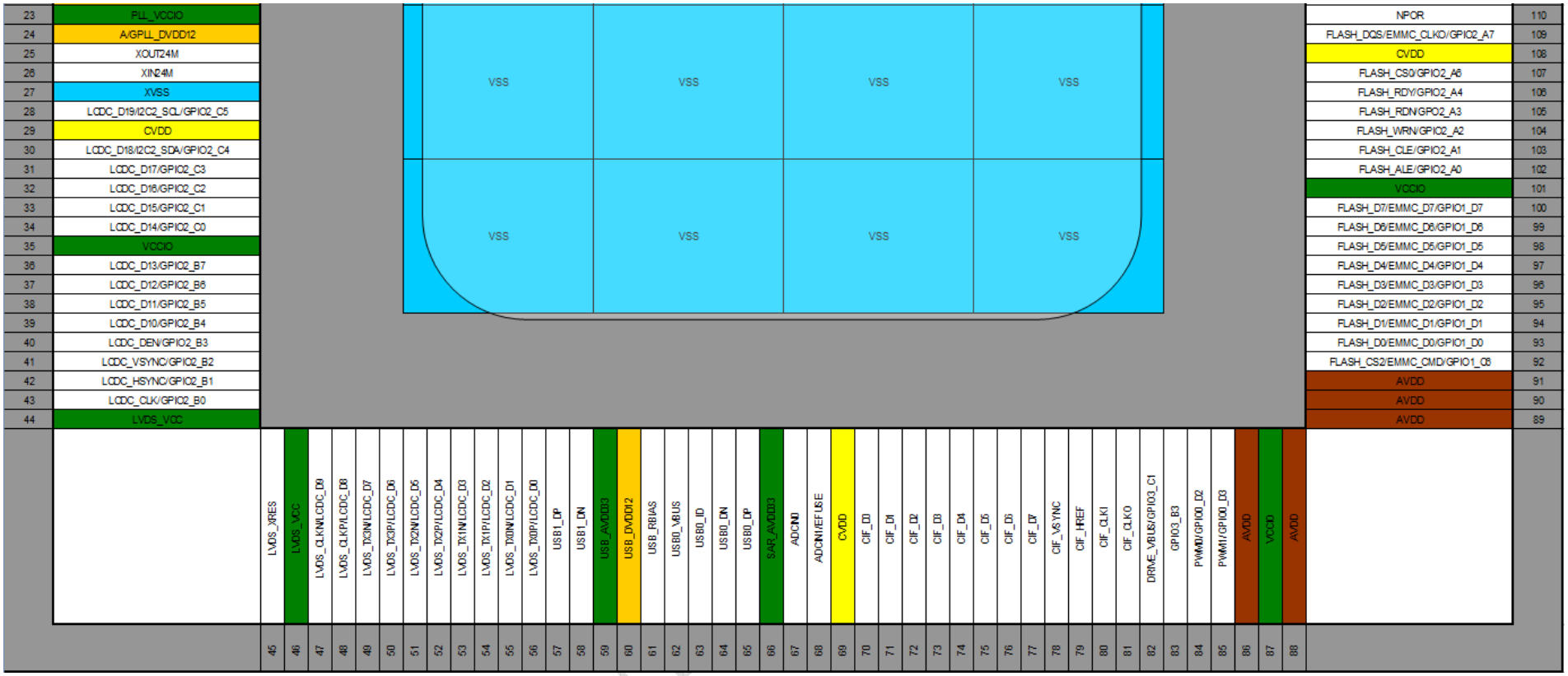


Fig 4 RK2926 Ball Map

3.5 RK2926 function IO descriptions

Table 3 2 RK2926 IO LIST

Pin	Ball Pin Name	IO Pull	Defual Dir	Defual function	Defual function description	Function 2	IO domain
1	DDR_A0	N/A	O	DDR_A0	DRAM address port		11_DDR
2	DDR_A2	N/A	O	DDR_A2	DRAM address port		11_DDR
3	DDR_A5	N/A	O	DDR_A5	DRAM address port		11_DDR
4	DDR_A9	N/A	O	DDR_A9	DRAM address port		11_DDR
5	DDR_A13	N/A	O	DDR_A13	DRAM address port		11_DDR
6	DDR_A7	N/A	O	DDR_A7	DRAM address port		11_DDR
7	DDR_ODT1	N/A	O	DDR_ODT1	DRAM on die termination contral1		11_DDR
8	DDR_DQ10	N/A	I/O	DDR_DQ10	DRAM data port		11_DDR
9	DDR_DQ8	N/A	I/O	DDR_DQ8	DRAM data port		11_DDR
10	DDR_VDD1	N/A	DP	DDR_VDD1	DRAM Digital power		12_POWER
11	DDR_DQS1	N/A	I/O	DDR_DQS1	DRAM data strobe1		11_DDR
12	DDR_DQS1n	N/A	I/O	DDR_DQS1n	DRAM data strobe1		11_DDR
13	CVDD1	N/A	DP	CVDD1	LOGIC/GPU core power		12_POWER
14	DDR_DQ14	N/A	I/O	DDR_DQ14	DRAM data port		11_DDR
15	DDR_DQ12	N/A	I/O	DDR_DQ12	DRAM data port		11_DDR
16	DDR_DQ15	N/A	I/O	DDR_DQ15	DRAM data port		11_DDR
17	DDR_DQ13	N/A	I/O	DDR_DQ13	DRAM data port		11_DDR
18	DDR_VDD2	N/A	DP	DDR_VDD2	DRAM Digital power		12_POWER
19	DDR_DQ9	N/A	I/O	DDR_DQ9	DRAM data port		11_DDR
20	DDR_DM1	N/A	I/O	DDR_DM1	DRAM data mask1		11_DDR
21	DDR_DQ11	N/A	I/O	DDR_DQ11	DRAM data port		11_DDR
22	C/DPLL_DVDD12	N/A	DP	C/DPLL_DVDD12	CODEC/DRAM PLL power		04_PLL
23	PLL_VCCIO	N/A	AP	PLL_VCCIO	PLL IO power		04_PLL
24	A/GPLL_DVDD12	N/A	DP	A/GPLL_DVDD12	ARM/GENERAL PLL power		04_PLL
25	XOUT24M	N/A	O	XOUT24M	24MHz clock output		03_MISC
26	XIN24M	N/A	I	XIN24M	24MHz clock input		03_MISC
27	XVSS	N/A	AG	XVSS	Crystal power ground		03_MISC
28	GPIO2_C5/I2C2_SCL/LCD_D19	down	I/O	I2C2_SCL	I2C2 serial port, for touch panel,need external pull-up		01_LCD/LVDS
29	CVDD2	N/A	DP	CVDD2	LOGIC/GPU core power		12_POWER
30	GPIO2_C4/I2C2_SDA/LCD_D18	down	I/O	I2C2_SDA	I2C2 serial port, for touch panel,need external pull-up		01_LCD/LVDS

31	GPIO2_C3/LCD_D17	down	I/O	LCD_D17	LCDC data port		01_LCD/LVDS
32	GPIO2_C2/LCD_D16	down	I/O	LCD_D16	LCDC data port		01_LCD/LVDS
33	GPIO2_C1/LCD_D15	down	I/O	LCD_D15	LCDC data port		01_LCD/LVDS
34	GPIO2_C0/LCD_D14	down	I/O	LCD_D14	LCDC data port		01_LCD/LVDS
35	VCCIO1	N/A	DP	VCCIO1	CPU IO power		12_POWER
36	GPIO2_B7/LCD_D13	down	I/O	LCD_D13	LCDC data port		01_LCD/LVDS
37	GPIO2_B6/LCD_D12	down	I/O	LCD_D12	LCDC data port		01_LCD/LVDS
38	GPIO2_B5/LCD_D11	down	I/O	LCD_D11	LCDC data port		01_LCD/LVDS
39	GPIO2_B4/LCD_D10	down	I/O	LCD_D10	LCDC data port		01_LCD/LVDS
40	GPIO2_B3/LCD_DEN	down	I/O	LCD_DEN	LCDC data enable		01_LCD/LVDS
41	GPIO2_B2/LCD_VSYNC	down	I/O	LCD_VSYNC	LCDC vertical sync signal output		01_LCD/LVDS
42	GPIO2_B1/LCD_HSYNC	down	I/O	LCD_HSYNC	LCDC horizontal sync signal output		01_LCD/LVDS
43	GPIO2_B0/LCD_DCLK	down	I/O	LCD_DCLK	LCDC pixel clk output		01_LCD/LVDS
44	LVDS_VCC	N/A	AP	LVDS_VCC	LCD power 3.3V/LVDS power 2.5V		01_LCD/LVDS
45	LVDS_XRES	N/A	A	LVDS_XRES	External a 12KOhm%1 resistor to VSS with LVDS mode		01_LCD/LVDS
46	LVDS_VCC	N/A	AP	LVDS_VCC	LCD power 3.3V/LVDS power 2.5V		01_LCD/LVDS
47	LVDS_CLKN/LCD_D9	N/A	A	LCD_D9	LCDC data port	LVDS_CLKN	01_LCD/LVDS
48	LVDS_CLKP/LCD_D8	N/A	A	LCD_D8	LCDC data port	LVDS_CLKP	01_LCD/LVDS
49	LVDS_TX3N/LCD_D7	N/A	A	LCD_D7	LCDC data port	LVDS_TX3N	01_LCD/LVDS
50	LVDS_TX3P/LCD_D6	N/A	A	LCD_D6	LCDC data port	LVDS_TX3P	01_LCD/LVDS
51	LVDS_TX2N/LCD_D5	N/A	A	LCD_D5	LCDC data port	LVDS_TX2N	01_LCD/LVDS
52	LVDS_TX2P/LCD_D4	N/A	A	LCD_D4	LCDC data port	LVDS_TX2P	01_LCD/LVDS
53	LVDS_TX1N/LCD_D3	N/A	A	LCD_D3	LCDC data port	LVDS_TX1N	01_LCD/LVDS
54	LVDS_TX1P/LCD_D2	N/A	A	LCD_D2	LCDC data port	LVDS_TX1P	01_LCD/LVDS
55	LVDS_TX0N/LCD_D1	N/A	A	LCD_D1	LCDC data port	LVDS_TX0N	01_LCD/LVDS
56	LVDS_TX0P/LCD_D0	N/A	A	LCD_D0	LCDC data port	LVDS_TX0P	01_LCD/LVDS
57	HOST_DP	N/A	A	HOST_DP	USB HOST Data Plus port		05_USB
58	HOST_DM	N/A	A	HOST_DN	USB HOST Data Minus port		05_USB
59	USB_AVDD33	N/A	AP	USB_AVDD33	USB analog power		05_USB
60	USB_DVDD12	N/A	DP	USB_DVDD12	USB digital power		05_USB
61	USB_RBIAS	N/A	A	USB_RBIAS	USB reference voltage output,connect a 44.2R%1 resistor		05_USB
62	OTG_VBUS	N/A	A	OTG_VBUS	USB OTG connected detect input		05_USB
63	OTG_ID	N/A	A	OTG_ID	USB OTG ID detect input,need external pull-up		05_USB
64	OTG_DM	N/A	A	OTG_DN	USB OTG Data Minus port		05_USB

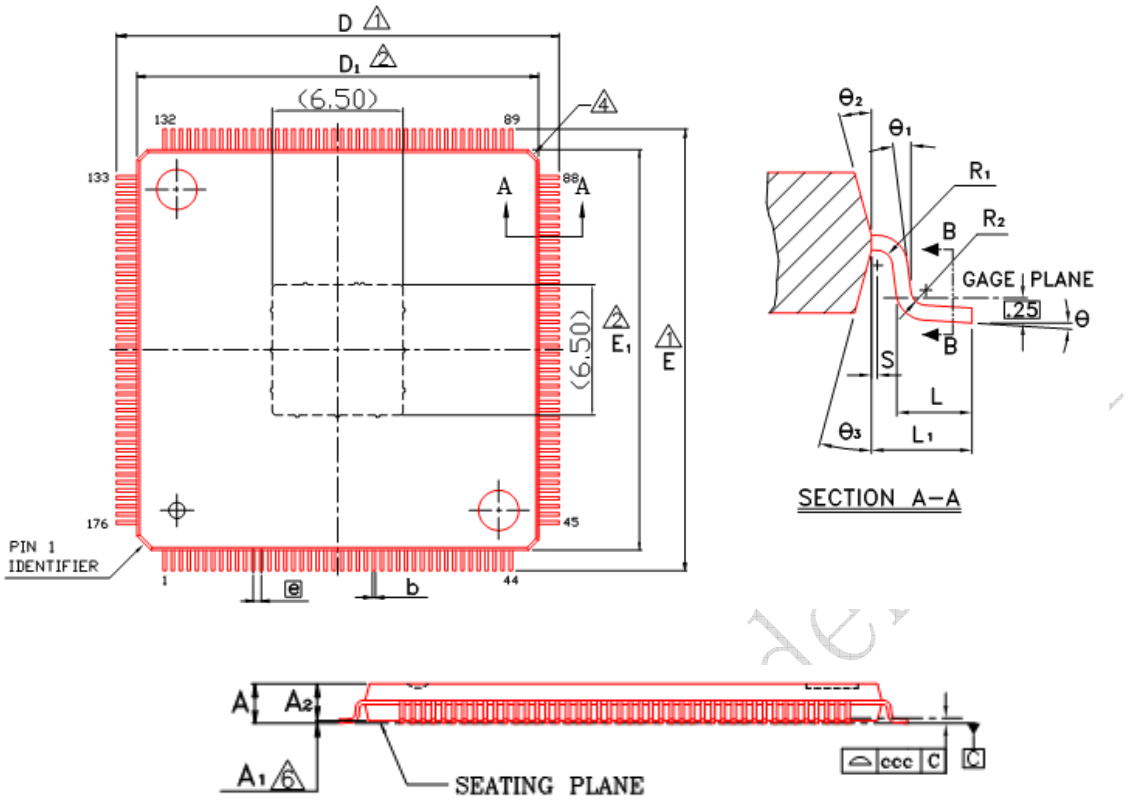
65	OTG_DP	N/A	A	OTG_DP	USB OTG Data Plus port		05_USB
66	SAR_AVDD33	N/A	AP	SAR_AVDD33	SARADC vref and analog power		05_USB
67	ADC_IN0	N/A	A	BAT_DET	Battery voltage input		06_ADC
68	ADC_IN1/EFUSE	N/A	A	ADKEY_IN	AD keyboard input	EFUSE	06_ADC
69	CVDD3	N/A	DP	CVDD3	LOGIC/GPU core power		12_POWER
70	CIF_D0	down	I	CIF_D0	Camera data port		02_CIF
71	CIF_D1	down	I	CIF_D1	Camera data port		02_CIF
72	CIF_D2	down	I	CIF_D2	Camera data port		02_CIF
73	CIF_D3	down	I	CIF_D3	Camera data port		02_CIF
74	CIF_D4	down	I	CIF_D4	Camera data port		02_CIF
75	CIF_D5	down	I	CIF_D5	Camera data port		02_CIF
76	CIF_D6	down	I	CIF_D6	Camera data port		02_CIF
77	CIF_D7	down	I	CIF_D7	Camera data port		02_CIF
78	CIF_VSYNC	down	I	CIF_VSYNC	Camera VYSNC input		02_CIF
79	CIF_HREF	down	I	CIF_HREF	Camera HREF input		02_CIF
80	CIF_CLKIN	down	I	CIF_CLKIN	Camera clock input		02_CIF
81	CIF_CLKO	down	I/O	CIF_CLKO	Camera clock output		02_CIF
82	GPIO3_C1/OTG_DRV	down	I/O	BL_EN	Backlight power enable		10_GPIO
83	GPIO3_B3/CIF_PDN	up	I/O	CIF_PDN	Camera power enable		10_GPIO
84	PWM0/GPIO0_D2	down	I/O	LCDC_BL	Display panel backlight brightness contral		10_GPIO
85	PWM1/GPIO0_D3	down	I/O	VIB_CTL	Vibration contral	PWM_LOG	10_GPIO
86	AVDD1	N/A	DP	AVDD1	ARM core power		12_POWER
87	VCCIO2	N/A	DP	VCCIO2	CPU IO power		12_POWER
88	AVDD2	N/A	DP	AVDD2	ARM core power		12_POWER
89	AVDD3	N/A	DP	AVDD3	ARM core power		12_POWER
90	AVDD4	N/A	DP	AVDD4	ARM core power		12_POWER
91	AVDD4	N/A	DP	AVDD4	ARM core power		12_POWER
92	GPIO1_C6/FLASH_CS2	up	I/O	FLASH_CS2	Nand flash select2 port		08_FLASH
93	GPIO1_D0/FLASH_D0	up	I/O	FLASH_D0	Nand flash data port		08_FLASH
94	GPIO1_D1/FLASH_D1	up	I/O	FLASH_D1	Nand flash data port		08_FLASH
95	GPIO1_D2/FLASH_D2	up	I/O	FLASH_D2	Nand flash data port		08_FLASH
96	GPIO1_D3/FLASH_D3	up	I/O	FLASH_D3	Nand flash data port		08_FLASH
97	GPIO1_D4/FLASH_D4	up	I/O	FLASH_D4	Nand flash data port		08_FLASH
98	GPIO1_D5/FLASH_D5	up	I/O	FLASH_D5	Nand flash data port		08_FLASH

99	GPIO1_D6/FLASH_D6	up	I/O	FLASH_D6	Nand flash data port		08_FLASH
100	GPIO1_D7/FLASH_D7	up	I/O	FLASH_D7	Nand flash data port		08_FLASH
101	VCCIO3	N/A	DP	VCCIO3	CPU IO power		12_POWER
102	GPIO2_A0/FLASH_ALE	down	I/O	FLASH_ALE	Nand flash address latch enable		08_FLASH
103	GPIO2_A1/FLASH_CLE	down	I/O	FLASH_CLE	Nand flash command latch enable		08_FLASH
104	GPIO2_A2/FLASH_WRN	up	I/O	FLASH_WRN	Nand flash write enable		08_FLASH
105	GPIO2_A3/FLASH_RDN	up	I/O	FLASH_RDN	Nand flash read enable		08_FLASH
106	GPIO2_A4/FLASH_RDY	up	I/O	FLASH_RDY	Nand flash read/busy output		08_FLASH
107	GPIO2_A6/FLASH_CSN0	up	I/O	FLASH_CS0	Nand flash select0 port		08_FLASH
108	CVDD4	N/A	DP	CVDD4	LOGIC/GPU core power		12_POWER
109	GPIO2_A7/FLASH_DQS	up	I/O	SDMMC_DET	SDMMC detect input		08_FLASH
110	NPOR	down	I	NPOR	System reset input		03_MISC
111	GPIO1_C5/SDMMC_D3	up	I/O	SDMMC0_D3	SDMMC data port		07_SDMMC
112	GPIO1_C4/SDMMC_D2	up	I/O	SDMMC0_D2	SDMMC data port		07_SDMMC
113	GPIO1_C3/SDMMC_D1	up	I/O	SDMMC0_D1	SDMMC data port		07_SDMMC
114	GPIO1_C2/SDMMC_D0	up	I/O	SDMMC0_D0	SDMMC data port		07_SDMMC
115	VCCIO4	N/A	DP	VCCIO4	CPU IO power		12_POWER
116	GPIO1_C0/SDMMC_CLKO	down	I/O	SDMMC0_CLKO	SDMMC clock output		07_SDMMC
117	GPIO1_B3/UART1_RTS/SPI_CSN	up	I/O	LCD_EN	Display panel power enable		10_GPIO
118	GPIO1_B2/UART1_RXD/SPI_RXD	up	I/O	GSENSOR_INT	Gsensor interupt input		10_GPIO
119	GPIO1_B1/UART1_TXD/SPI_TXD	up	I/O	PMIC_INT	PMIC interrupt input		10_GPIO
120	GPIO1_B0/UART1_CTS/SPI_CLK	up	I/O	TOUCH_INT	Touch panel interrupt input		10_GPIO
121	GPIO1_A5/I2S_SDI	down	I/O	DC_DET	DC insert detect input,need external pull-up	RTC_INT	10_GPIO
122	GPIO1_A4/I2S_SDO	down	I/O	PWR_KEY	Power key detect input		10_GPIO
123	GPIO1_A2/I2S_LRCK_RX	down	I/O	PWR_HOLD	System power hold up enable		10_GPIO
124	GPIO1_A1/I2S_SCLK	down	I/O	PMIC_SLEEP/WL_PWR	PMIC sleep output/WIFI power enable		10_GPIO
125	GPIO1_A0/I2S_MCLK	down	I/O	SPK_CTL	Speaker mute enable		10_GPIO
126	CVDD5	N/A	DP	CVDD5	LOGIC/GPU core power		12_POWER
127	GPIO1_B7/SDMMC_CMD	up	I/O	SDMMC0_CMD	SDMMC command		07_SDMMC
128	GPIO0_A3/I2C1_SDA	up	I/O	I2C1_SDA	I2C1 serial port,for external device,need external pull-up		10_GPIO
129	GPIO0_A2/I2C1_SCL	up	I/O	I2C1_SCL	I2C1 serial port,for external device,need external pull-up		10_GPIO
130	GPIO0_A1/I2C0_SDA	up	I/O	I2C0_SDA	I2C0 serial port,for PMIC and RTC,need external pull-up		10_GPIO
131	GPIO0_A0/I2C0_SCL	up	I/O	I2C0_SCL	I2C0 serial port,for PMIC and RTC,need external pull-up		10_GPIO
132	CODEC_VCM	N/A	A	CODEC_VCM	Codec VCM ,connected with GND through a 4.7uF CAP		09_CODEC

133	CODEC_MIC	N/A	A	CODEC_MIC	Codec mic input		09_CODEC
134	CODEC_AVSS	N/A	AG	CODEC_AVSS	Codec power ground		09_CODEC
135	CODEC_AOL	N/A	A	CODEC_AOL	Codec left analog output		09_CODEC
136	CODEC_AVDD	N/A	AP	CODEC_AVDD	Codec vref voltage and analog power		09_CODEC
137	CODEC_AOR	N/A	A	CODEC_AOR	Codec right analog output		09_CODEC
138	CODEC_AVSS	N/A	AG	CODEC_AVSS	Codec power ground		09_CODEC
139	DDR_VSS	N/A	GP	DDR_VSS	DRAM power ground		12_POWER
140	DDR_DQ2	N/A	I/O	DDR_DQ2	DRAM data port		11_DDR
141	DDR_DQ0	N/A	I/O	DDR_DQ0	DRAM data port		11_DDR
142	DDR_VDD3	N/A	DP	DDR_VDD3	DRAM Digital power		12_POWER
143	DDR_DQS0	N/A	I/O	DDR_DQS0	DRAM data strobe0		11_DDR
144	DDR_DQS0n	N/A	I/O	DDR_DQS0n	DRAM data strobe0		11_DDR
145	DDR_DQ6	N/A	I/O	DDR_DQ6	DRAM data port		11_DDR
146	DDR_DQ4	N/A	I/O	DDR_DQ4	DRAM data port		11_DDR
147	DDR_DQ7	N/A	I/O	DDR_DQ7	DRAM data port		11_DDR
148	DDR_DQ5	N/A	I/O	DDR_DQ5	DRAM data port		11_DDR
149	DDR_VDD4	N/A	DP	DDR_VDD4	DRAM Digital power		12_POWER
150	DDR_DQ1	N/A	I/O	DDR_DQ1	DRAM data port		11_DDR
151	DDR_DM0	N/A	I/O	DDR_DM0	DRAM data mask0		11_DDR
152	DDR_DQ3	N/A	I/O	DDR_DQ3	DRAM data port		11_DDR
153	DDR_A8	N/A	O	DDR_A8	DRAM address port		11_DDR
154	DDR_A6	N/A	O	DDR_A6	DRAM address port		11_DDR
155	DDR_A14	N/A	O	DDR_A14	DRAM address port		11_DDR
156	DDR_A15	N/A	O	DDR_A15	DRAM address port		11_DDR
157	DDR_A11	N/A	O	DDR_A11	DRAM address port		11_DDR
158	DDR_A1	N/A	O	DDR_A1	DRAM address port		11_DDR
159	DDR_A4	N/A	O	DDR_A4	DRAM address port		11_DDR
160	DDR_A12	N/A	O	DDR_A12	DRAM address port		11_DDR
161	CVDD7	N/A	DP	CVDD7	LOGIC/GPU core power		12_POWER
162	DDR_BA1	N/A	O	DDR_BA1	DRAM bank select 1		11_DDR
163	DDR_BA0	N/A	O	DDR_BA0	DRAM bank select 0		11_DDR
164	DDR_A10	N/A	O	DDR_A10	DRAM address port		11_DDR
165	DDR_CKE	N/A	O	DDR_CKE	DRAM clock enable		11_DDR
166	DDR_ODT0	N/A	O	DDR_ODT0	DRAM on die termination contral0		11_DDR

167	DDR_CLKn	N/A	O	DDR_CKn	DRAM defferential clock output		11_DDR
168	DDR_CLK	N/A	O	DDR_CK	DRAM defferential clock output		11_DDR
169	DDR_VDD5	N/A	DP	DDR_VDD5	DRAM Digital power		12_POWER
170	DDR_RASN	N/A	O	DDR_RASN	DRAM command output		11_DDR
171	DDR_CASN	N/A	O	DDR_CASN	DRAM command output		11_DDR
172	DDR_CSN1	N/A	O	DDR_CSN1	DRAM chip select1		11_DDR
173	DDR_CSN0	N/A	O	DDR_CSN0	DRAM chip select0		11_DDR
174	DDR_WEN	N/A	O	DDR_WEN	DRAM command output		11_DDR
175	DDR_BA2	N/A	O	DDR_BA2	DRAM bank select 2		11_DDR
176	DDR_A3	N/A	O	DDR_A3	DRAM address port		11_DDR
ePAD	VSS	N/A	GP	VSS	CPU power ground		12_POWER

3.6 RK2926 Dimension



Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.60	—	—	0.063
A_1	0.05	—	0.15	0.002	—	0.006
A_2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.13	0.18	0.23	0.005	0.007	0.009
b_1	0.13	0.16	0.19	0.005	0.006	0.007
c	0.09	—	0.20	0.004	—	0.008
c_1	0.09	0.12	0.16	0.004	0.005	0.006
D	21.60	22.00	22.40	0.850	0.866	0.882
D_1	—	20.00	—	—	0.787	—
E	21.60	22.00	22.40	0.850	0.866	0.882
E_1	—	20.00	—	—	0.787	—
e	0.40 BSC			0.016 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1	1.00 REF			0.039 REF		
R_1	0.08	—	—	0.003	—	—
R_2	0.08	—	—	0.003	—	—
S	0.20	—	—	0.008	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
$θ_1$	0°	—	—	0°	—	—
$θ_2$	11°	12°	13°	11°	12°	13°
$θ_3$	11°	12°	13°	11°	12°	13°
ccc	0.08			0.003		

Chapter 4 Electrical Specification

4.1 Absolute Maximum Ratings

Table 4 1 RK292X absolute maximum ratings

Paramerters	Related Power Group	Max	Unit
DC supply voltage for Internal digital logic	AVDD,CVDD, USB_DVDD12,HDMI_DVDD12,LVDS_DVDD12	1.32	V
DC supply voltage for Digital GPIO (except for SAR-ADC, PLL, USB, DDR IO)	VDDIO	3.6	V
DC supply voltage for DDR IO	DDR_VDD	1.95	V
DC supply voltage for Analog part of SAR-ADC	SAR_AVDD33	3.6	V
DC supply voltage for Analog part of PLL	PLL_VCCIO APLL_DVDD12,DPLL_DVDD12,CGPLL_DVDD12	3.3 1.32	V
DC supply voltage for Analog part of USB OTG/Host2.0	USB_AVDD33	3.63	V
DC supply voltage for Analog part of HDMI	HDMI_AVDD33	3.63	V
DC supply voltage for Analog part of Acodec	CODEC_AVDD	3.63	V
DC supply voltage for Analog part of LVDS	LVDS_VCC	3.63	V
Analog Input voltage for SAR-ADC		2.75	V
Analog Input voltage for DP/DM/VBUS of USB OTG/Host2.0		5	V
Digital input voltage for input buffer of GPIO		3.6	V
Digital output voltage for output buffer of GPIO		3.6	V
Storage Temperature		150	℃

Absolute maximum ratings specify the values beyond which the device may be damaged permanently. Long-term exposure to absolute maximum ratings conditions may affect device reliability.

4.2 Recommended Operating Conditions

Table 4 2 RK292X recommended operating conditions

Parameters	Symbol	Min	Typ	Max	Units
Internal digital logic Power	AVDD,CVDD, USB_DVDD12,HDMI_DVDD12,LVDS_DVDD12	1.08	1.2	1.32	V
Digital GPIO Power(3.3V)	VDDIO	2.97	3.3	3.63	V
DDR IO (DDRIII mode) Power	DDR_VDD	1.425	1.5	1.575	V
DDR IO (LVDDRIII mode) Power	DDR_VDD	1.28	1.35	1.45	V
PLL Analog Power	PLL_VCCIO	2.97	3.3	3.63	V
PLL Analog Power	APLL_DVDD12,DPLL_DVDD12, CGPLL_DVDD12	1.08	1.2	1.32	V
SAR-ADC Analog Power	SAR_AVDD33	2.97	3.3	3.63	V
SAR-ADC external reference Power	VREF	0.2* SAR_AVDD33		0.9* SAR_AVDD33	
USB OTG/Host2.0 Analog Power(3.3V)	USB_AVDD33	2.97	3.3	3.63	V
USB OTG/Host2.0 external resistor	REXT	40.5	45	49.5	Ohm
Acodec Analog Power	CODEC_AVDD	2.97	3.3	3.63	V

HDMI Analog Power	HDMI_AVDD33	2.97	3.3	3.63	V
EFUSE programming voltage		N/A	2.5	N/A	V
PLL input clock frequency		N/A	24	N/A	MHz
Operating Temperature		-40	25	85	℃

4.3 DC Characteristics

Table 4 3 RK292X DC Characteristics

Parameters		Symbol	Min	Typ	Max	Units
Digital GPIO @3.3V	Input Low Voltage	Vil	-0.3	0	0.8	V
	Input High Voltage	Vih	2	3.3	3.6	V
	Output Low Voltage	Vol	N/A	0	0.4	V
	Output High Voltage	Voh	2.4	3.3	N/A	V
	Threshold Point	Vt	1.21	1.42	1.64	V
	Schmitt trig Low to High threshold point	Vt+	1.36	1.6	1.86	V
	Schmitt trig High to Low threshold point	Vt-	0.93	1.09	1.3	V
	Pullup Resistor	Rpu	33	41	62	Kohm
	Pulldown Resistor	Rpd	33	42	68	Kohm
Digital GPIO @1.8V	Input Low Voltage	Vil	-0.3	0	0.63	V
	Input High Voltage	Vih	1.17	1.8	2.1	V
	Output Low Voltage	Vol	N/A	0	0.45	V
	Output High Voltage	Voh	1.35	1.8	N/A	V
	Threshold Point	Vt	0.72	0.83	0.95	V
	Schmitt trig Low to High threshold point	Vt+	0.74	0.88	1.03	V
	Schmitt trig High to Low threshold point	Vt-	0.52	0.61	0.73	V
	Pullup Resistor	Rpu	67	93	152	Kohm
	Pulldown Resistor	Rpd	64	92	170	Kohm
DDR IO @DDRIII mode	Input High Voltage	Vih_ddr	VREFi + 0.125 (i=0~2)	1.8	VDDIO_DDRi + 0.3 (i=0~6)	V
	Input Low Voltage	Vil_ddr	-0.3	0	VREFi - 0.125 (i=0~2)	V
	Output High Voltage	Voh_ddr	VDDIO_DDRi - 0.28 (i=0~6)	1.8	N/A	V
	Output Low Voltage	Vol_ddr	N/A	0	0.28	V
	Input termination resistance(ODT) to VDDIO_DDRi/2 (i=0~6)	Rtt	120 60 40	150 75 50	180 90 60	Ohm
DDR IO @LPDDR mode	Input High Voltage	Vih_ddr	0.7*VDDIO_DDRi (i=0~6)	1.8	N/A	V
	Input Low Voltage	Vil_ddr	N/A	0	0.3*VDDIO_DDRi (i=0~6)	V
PLL	Input High Voltage	Vih_pll	0.8*DVDD_iPLL (i=A,D,CG)	DVDD_iPLL (i=A,D,CG)	DVDD_iPLL (i=A,D,CG)	V
	Input Low Voltage	Vil_pll	0	0	0.2*DVDD_iPLL (i=A,D,CG)	V
LVDS	Output voltage high, Voa or Vob(Rload = 100om+-1%)	Voh	N/A	1475	N/A	mV
	Output voltage low, Voa or Vob(Rload = 100om+-1%)	Vol	925	N/A	N/A	mV

	Output differential voltage (Rload = 100om+-1%)	|Vod|	250	N/A	450	mV
	Output offset voltage(Rload = 100om+-1%)	Vos	1125	N/A	1375	mv
	Change in |Vod| between '0' and '1'(Rload = 100om+-1%)	|△ Vod|	N/A	N/A	50/150①	mV
	change in Vos between '0' and '1'(Rload = 100om+-1%)	△Vos	N/A	N/A	50	mv
	Output current(Transmitter shorted to ground)	Isa,Isb	N/A	N/A	24	mA
	Output current(Transmitter shorted to ground)	Isab	N/A	N/A	12	mA
HDMI	single-ended high level output voltage, VH(when sink <=165Mhz)	Voh	HDMI_AVDD33-10mv	N/A	HDMI_AVDD33+10mv	mV
	single-ended high level output voltage, VH(when sink > 165Mhz)	Voh	HDMI_AVDD33-200mv	N/A	HDMI_AVDD33+10mv	mV
	single-ended low level output voltage, VL (when sink <= 165Mhz)	Vol	HDMI_AVDD33 -600mv	N/A	HDMI_AVDD33-400mv	mV
	single-ended low level output voltage, VL (when sink > 165Mhz)	Vol	HDMI_AVDD33-700mv	N/A	HDMI_AVDD33-400mv	mv
	single-ended output swing voltage, Vswing	Vswing	400	N/A	600	mV
	single-ended standby (off) output voltage,	Voff	HDMI_AVDD33 -10mv	N/A	HDMI_AVDD33+10mv	mv
	single-ended standby (off) output current	Ioff	-10	N/A	10	uA

4.4 Recommended Operating Frequency

Table 4 4 Recommended operating frequency for PLL and oscillator domain

Parameter	Condition	Symbol	MIN	TYP	MAX	Unit
XIN Oscillator	1.2V , 25 ℃	XIN24M	24	24	24	MHz
	1.32V , -40 ℃		24	24	24	
	1.08V , 125 ℃		24	24	24	
DDR PLL	1.2V , 25 ℃	ddr_pll_clk	N/A	N/A	1323	MHz
	1.32V , -40 ℃		N/A	N/A	1798	
	1.08V , 125 ℃		N/A	N/A	806	
ARM PLL	1.2V , 25 ℃	arm_pll_clk	N/A	N/A	1347	MHz
	1.32V , -40 ℃		N/A	N/A	1763	

	1.08V , 125 ℃		N/A	N/A	792	
CODEC PLL	1.2V , 25 ℃	cocec_pll_clk	N/A	N/A	976	MHz
	1.32V , -40 ℃		N/A	N/A	1315	
	1.08V , 125 ℃		N/A	N/A	593	
GENERAL PLL	1.2V , 25 ℃	general_pll_clk	N/A	N/A	927	MHz
	1.32V , -40 ℃		N/A	N/A	1362	
	1.08V , 125 ℃		N/A	N/A	533	

4.5 Electrical Characteristics for General IO

Table 4 5 RK292X Electrical Characteristics for Digital General IO

Parameters		Symbol	Test condition	Min	Typ	Max	Units
Digital GPIO@3.3V	Input leakage current	Il	Vin = 3.3V or 0V	-1	N/A	1	uA
	Tri-state output leakage current	Ioz	Vout = 3.3V or 0V	-1	N/A	1	uA
	High level input current	Iih	Vin = 3.3V, pulldown disabled	TBD	N/A	TBD	uA
			Vin = 3.3V, pulldown enabled	TBD	TBD	TBD	uA
	Low level input current	Iil	Vin = 0V, pullup disabled	TBD	N/A	TBD	uA
			Vin = 0V, pullup enabled	TBD	TBD	TBD	uA
Digital GPIO @1.8V	Input leakage current	Ii	Vin = 1.8V or 0V	-1	N/A	1	uA
	Tri-state output leakage current	Ioz	Vout = 1.8V or 0V	-1	N/A	1	uA
	High level input current	Iih	Vin = 1.8V, pulldown disabled	TBD	N/A	TBD	uA
			Vin = 1.8V, pulldown enabled	TBD	TBD	TBD	uA
	Low level input current	Iil	Vin = 0V, pullup disabled	TBD	N/A	TBD	uA
			Vin = 0V, pullup enabled	TBD	TBD	TBD	uA

4.6 Electrical Characteristics for PLL

Table 4 6 RK292X Electrical Characteristics for PLL

Parameters		Symbol	Test condition	Min	Typ	Max	Units
PLL	Input clock frequency	Fin	Fin = FREF @3.3V/1.2V①	1/10	24	800	MHz
	Comparison frequency	Fref	FREF = Fin/REFDIV @3.3V/1.2V	1	N/A	40	MHz
	VCO operating range	Fvco	Fvco = Fref * FBDIV① @3.3V/1.2V	400	N/A	1600	MHz
	Output clock frequency	Fout	Fout = Fvco/POSTDIV① @3.3V/1.2V	1	N/A	1600	MHz
	Lock time②	Tlt	@ 3.3V/1.2V, FREF=24M,REFDIV=1	N/A	41.7	62.5	us
	VDDHV Power consumption ③ (normal mode)	N/A	Fvco = 1000MHz, @3.3V, 25 ℃	N/A	1	1.2	mA
	VDD Power consumption (normal mode)	N/A	@3.3V/1.2V, 25 ℃	N/A	3	4	uW/MHz
	Power consumption (bypass mode)	N/A	BYPASS=HIGH , PD= LOW , Fin = 24MHz, Fout = 24MHz, @3.3V/1.2V, 25 ℃	N/A	N/A	N/A	uW

	Power consumption (power-down mode)	N/A	PD=HIGH, @27 ℃	N/A	10	N/A	uA

Notes : ①: REFDIV is the input divider value;
FBDIV is the feedback divider value;
POSTDIV is the output divider value
②Lock Time is 1000cycles of input clocks in typ, and 1500cycles of input clocks in max.
③Current scale as (Fvco/1GHz)$^{1.5}$

4.7 Electrical Characteristics for SAR-ADC

Table 4 7 RK292X Electrical Characteristics for SAR-ADC

Parameters	Symbol	Test condition	Min	Typ	Max	Units
ADC resolution			N/A	10	N/A	bits
Conversion speed	Fs		N/A	N/A	N/A	MSPS
Differential Non Linearity	DNL		N/A	N/A	N/A	LSB
Integral Nn Linearity	INL		N/A	N/A	N/A	LSB
Gain Error	Egain		N/A	N/A	N/A	%FS
Offset Error	Eoffset		N/A	N/A	N/A	%FS
Input Range	CH[2:0]	3-channel single-ended input	0.01*SAR_AVDD33	N/A	0.99*SAR_AVDD33	V
Input Resistance	RIN		N/A	N/A	N/A	Kom
Input Capacitance	CIN		N/A	1	N/A	pF
Sampling Clock			N/A	200	N/A	KHz
Main Clock Frequency	CLK		N/A	2.2	N/A	MHz
Data Latency			N/A	11	N/A	Clock Cycle
SNR plus Distortion(Up to 5th harmonic)	SINAD	Fin=10K Fin=99K	N/A	61.49 60.58	N/A	dB
Spurious-Free Dynamic Range	SFDR	Fin=10K Fin=99K	N/A	66.29 67.14	N/A	dB
Second-Harmonic Distortion	2HD	Fin=10K Fin=99K	N/A	-72.64 -69.94	N/A	dB
Third-Harmonic Distortion	3HD	Fin=10K Fin=99K	N/A	-74.79 -68.85	N/A	dB
Effective Number of Bits	ENOB	Fin=10K Fin=99K	N/A	9.92 9.77	N/A	Bits
Positive Reference	VREF		0.2*SARADC_AVDD33		0.9*SARADC_AVDD33	V
Analog Supply Current(SARADC_VDDA)			N/A	N/A	200	uA
Digital Supply Current			N/A	N/A	50	uA
Reference Supply Current			N/A	N/A	50	uA
Power Down Current			N/A	N/A	N/A	uA
Power up time			N/A	N/A	N/A	1/Fs

4.8 Electrical Characteristics for USB OTG/Host Interface

Table 4 8 RK292X Electrical Characteristics for USB OTG/Host2.0 Interface

Parameters	Test condition	Min	Typ	Max	Units

HS transmit,(quiescent supply current; Vin=0 or 1)	Current From USB_AVDD33	USB_AVDD33 = 3.3V USB_DVDD12 = 1.2V	N/A	N/A	0.1	mA
	Current From USB_DVDD12		N/A	N/A	20	mA
Classic mode active(quiescent supply current; Vin=0 or 1)	Current From USB_AVDD33		N/A	N/A	0.5	mA
	Current From USB_DVDD12		N/A	N/A	0.5	mA
HS mode(CL=10pF) Active supply current	Current From USB_AVDD33		N/A	0.1	N/A	mA
	Current From USB_DVDD12		N/A	2.22	N/A	mA
FS transmit,(CL=50pF) Active supply current	Current From USB_AVDD33		N/A	10	30	mA
	Current From USB_DVDD12		N/A	5	10	mA
LS transmit(CL=50 to 350pF) Active supply current	Current From USB_AVDD33		N/A	2	25	mA
	Current From USB_DVDD12		N/A	2	5	mA
Suspend mode	Current From USB_AVDD33		N/A	N/A	50	uA
	Current From USB_DVDD12		N/A	N/A	5	uA

4.9 Electrical Characteristics for HDMI

Table 4 9 RK292X Electrical Characteristics for HDMI

Parameters	Symbol	Test condition	Min	Typ	Max	Units
rise time/fall time(20%-80%)	Tfall/Trise		75	N/A	0.4Tbit	ps
overshoot, max			15% of full differential amplitude(Vswing*2)			ps
undershoot, max			25% of full differential amplitude(Vswing*2)			ps
Intra-pair skew at transmitter connector, max			N/A	N/A	0.15 Tbit	ps
inter-pair skew at transmitter connector, max			N/A	N/A	0.2 Tpixel	ps
TMDS Differential clock jitter, max			N/A	N/A	0.25 Tbit	ps
clock duty cycle			40%	N/A	60%	

4.10 Electrical Characteristics for DDR IO

Table 4 10 RK292X Electrical Characteristics for DDR IO

Parameters		Symbol	Test condition	Min	Typ	Max	Units
DDR IO @DDR3 mode	DDR IO power standby current, ODT OFF		@ 1.5V , 125℃	N/A	N/A	N/A	uA
	Input leakage current, SSTL mode, unterminated		@ 1.5V , 125℃	N/A	N/A	N/A	uA
DDR IO @LVDDR3 mode	Input leakage current		@ 1.35V , 125℃	N/A	N/A	N/A	uA
	DDR IO power quiescent current		@ 1.35V , 125℃	N/A	N/A	N/A	uA

4.11 Electrical Characteristics for eFuse

Table 4 11 RK292X Electrical Characteristics for eFuse

	Parameters	Symbol	Test condition	Min	Typ	Max	Units
Active mode	read current	Iactive	STROBE high	N/A	2.53	N/A	mA

standby mode	standby current	Istandby		N/A	0.4	N/A	uA
power-down mode	power-down current	Ipd_vdd		N/A	N/A	N/A	uA
Peak program current	Peak program current	Iprog		N/A	20.8	N/A	mA

Chapter 5 Hardware Guideline

5.1 Reference design for RK292X oscillator

RK292X only use one oscillator, and its typical clock frequency is 24MHz. The oscillator will provide input clock to four on-chip PLLs.

- External reference circuit for oscillators with 24MHz input

In the following diagram , Rf is used to bias the inverter in the high gain region. The recommend value is 1Mohm.

Rd is used to increase stability, low power consumption, suppress the gain in high frequency region and also reduce -Rd of the oscillator. Thus, proper Rd cannot be too large to cease the loop oscillating.

C1 and C2 are deciding regard to the crystal or resonator CL specification.

the value for Rf,Rd,C1,C2 must be adjusted a little to improve performance of oscillator based on real crystal model .

In RK292X, the crystal oscillator I/O cells have embedded internal resistor, so we need not add feedback resistor (Rf) as above description.

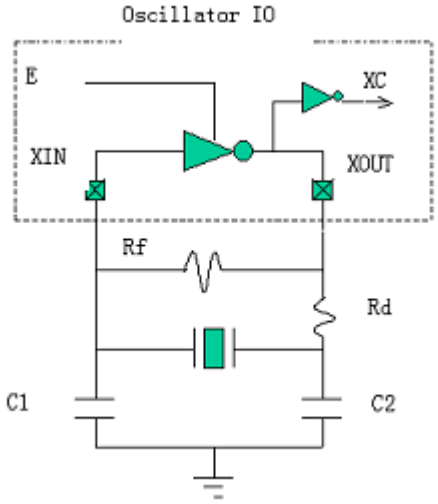


Fig 5 External Reference Circuit for 24MHzOscillators

5.2 Reference design for PLL PCB connection

The following reference design is suitable for PLL in RK292X.

For optimal jitter performance it is suggested to place external decoupling capacitorson the boardbetween VDDHV-VSS(PLL_VSS1) and

VDDPOST-VSS(PLL_VSS2) . VDDREF is typically connected to the global chipsupply and does not require dedicated decoupling.

It is recommended to use at least one large capacitor (e.g. 4.7uF) capacitor for each separate supply.Additionally, a 100nF and 10nF capacitor may be placed in parallel since the lead inductance of the4.7uF capacitor may be large.

Capacitors with minimal lead inductance should be selected. Ceramic type capacitors work well. Thecapacitors should be placed as close to the package pins as possible. No series impedance shouldbe added anywhere on the board, and impedance to the voltage source should be minimized.

5.3 Reference design for USB OTG/Host2.0 connection

In RK292X there are USB OTG and USB Host2.0 interface, and they share a common PHY.

- Decouple Capacitance

We should include decoupling and bypass capacitors at each power pin in the layout.

These are shown schematically in Figure 1-9. Place these components as closely as possible to the power pins.

- Differential Lines

The differential lines should be routed together, minimizing the number of vias through which the signal lines are routed. Layout the differential pairs with controlled impedance of 100 ohm differential.

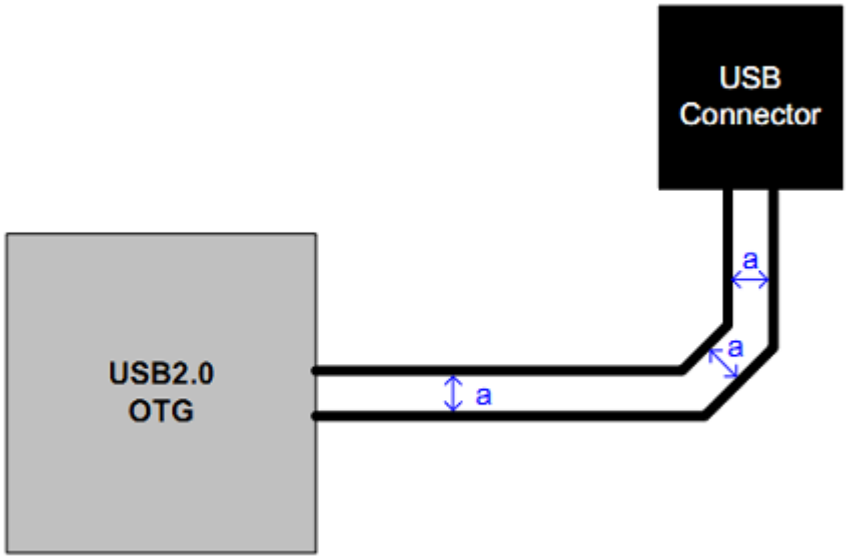


Fig 6 RK292X USB OTG/Host2.0 differential lines requirement

If high-speed signals are routed on the Top layer, best results will be obtained if the Layer 2 is a Ground plane. Furthermore, there must have only one ground plane under high-speed signals in order to avoid the high-speed signals to cross another ground plane.

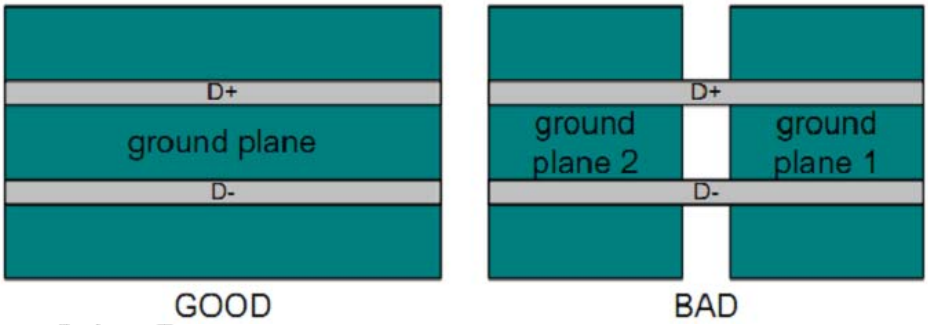


Fig 7 RK292X USB OTG/Host2.0 ground plane guide.

- Component Placement

It is very important to not create stubs on the high-speed lines, to avoid that, the placement of component should be the closed as possible from D+ and D- lines, like shown in the following figure.

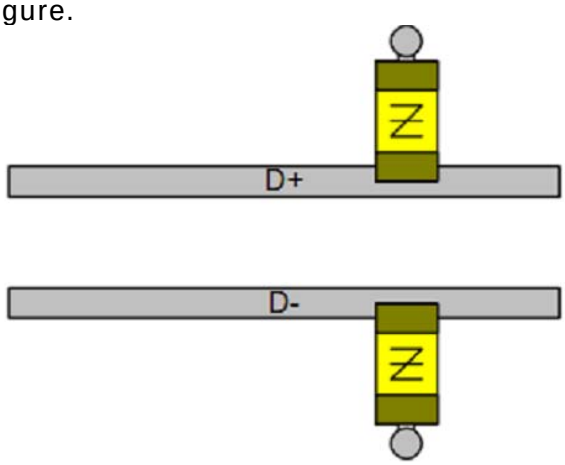


Fig 错误！未找到引用源。 RK292X USB OTG/Host2.0 component placement.

5.4 Reference design for HDMI Tx PHY connection

In RK2928G, the following diagram shows external PCB reference design for HDMI Tx PHY.It mainly introduces how to connect the TMDS channel, DDC channel, CEC channel and HPD signal of RK2928G HDMI Transmitter to the HDMI port type A.

- TMDS channel

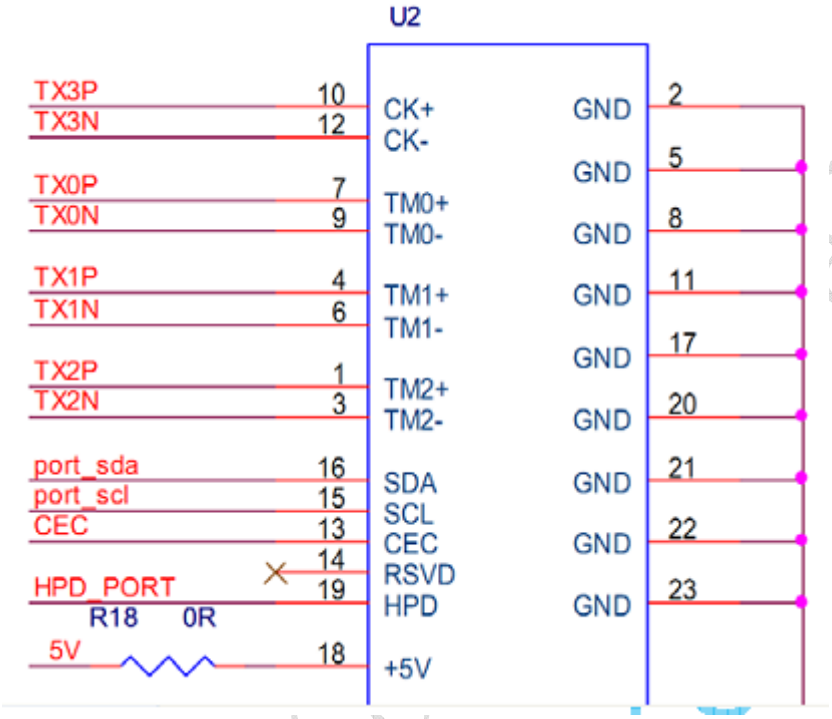


Fig 8 RK2928G HDMI interface reference connection

- DDC channel

As shown the PCB Scheme below, the DDC_sda and DDC_scl on the Transmitter IP must be changed the working voltage from 3.3V to 5V by the component UPA672T. The DDC_sda and DDC_scl on Transmitter IP side must be pulled up through a 10K resistor to 3.3V DC power. The port_sda and port_scl on the HDMI port side must be pulled up through a 10K resistor to 5V DC power.

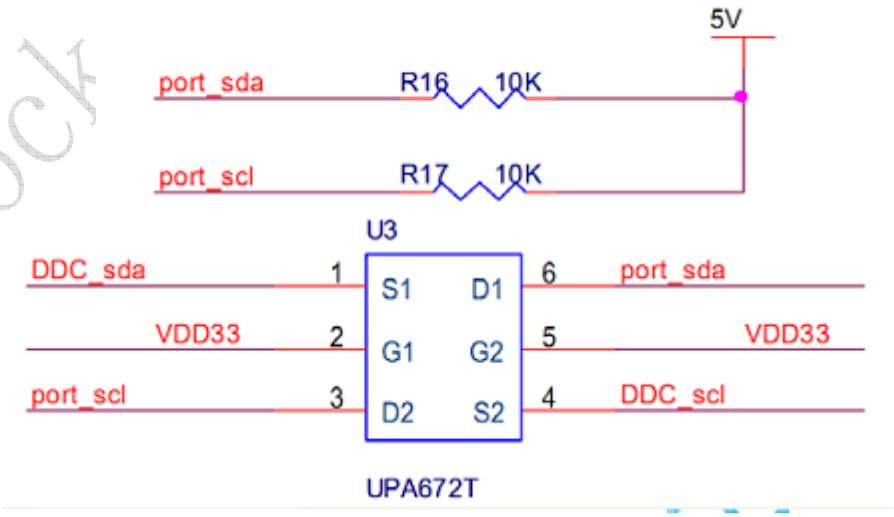


Fig 9 RK2928G HDMI DDC interface reference connection

- CEC channel

The signal CEC_sda on the HDMI Transmitter must be pulled up through a 10K resistor to 3.3V DC power, then directly connect to CEC pad on the HDMI port.

- HPD

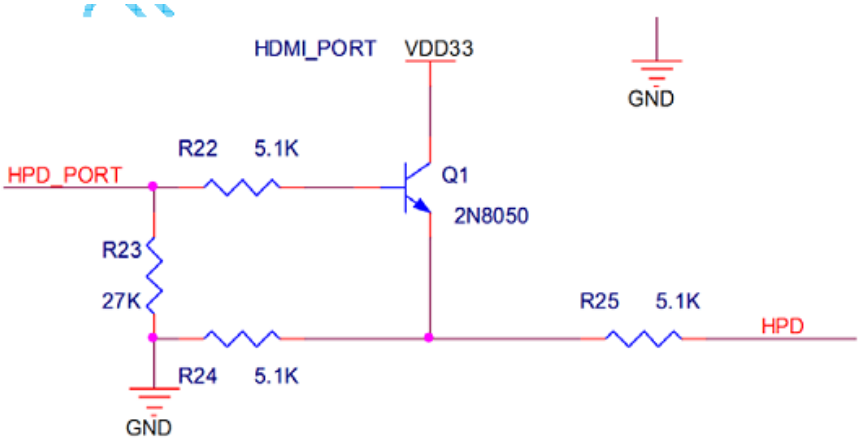


Fig 10 RK2928G HDMI CEC interface reference connection

- ESD

If ESD suppression devices or common mode chokes are used, place them near the HDMI connector.

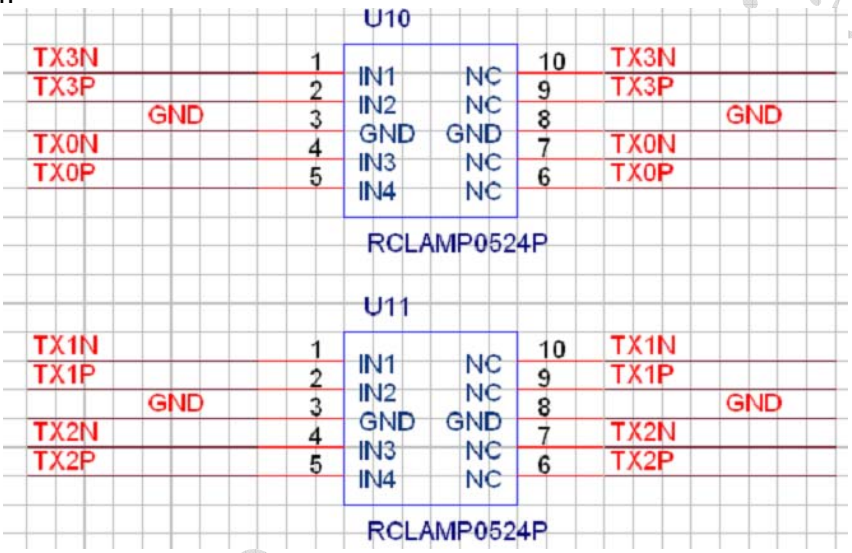


Fig 11 RK2928G HDMI ESD interface reference connection

5.5 Reference design for Audio Codec connection

In RK292X, the following diagram shows external PCB reference design for Audio Codec.

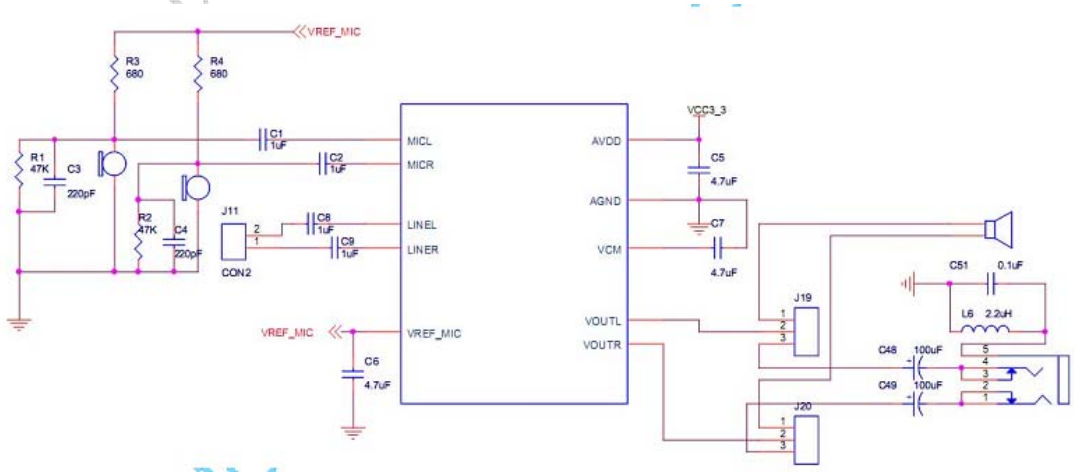


Fig 12 RK292X Audio Codec interface reference connection

As above diagram shows, the MICL and MICR are each connected with a MIC through a 1uf CAP, the LINEL and LINER have the same function as the MICL and MICR. The R1 and C3 are formed a filter for the MIC, and the R2, C4 have same function. The VREF_MIC is used for bias the MIC through a resistor. The resistor value should be

changed according the MIC. The AVDD should be supplied by 3.3V. The CAP connected with AVDD should be placed as close as possible

The VCM is connected with GND through a 4.7Uf CAP. The CAP should be placed as close as possible. The VOUTL and VOUTR could be connected with a speaker or an earphone. When connecting with a speaker, they could connect it directly. When connecting with an earphone, they should connect it through a 100uF CAP. The J19 and J20 are dip-switches, and you could select a speaker or an earphone as the output.

5.6 RK292X Power on reset descriptions

NPOR is hardware reset signal from out-chip, which is filtered glitch to obtain signal sysrstn. To make PLLs work normally, the PLL reset signal (pllrstn) must maintain high for more than 1us, and PLLs start to lock when pllrstn deassert, andthe PLL max lock time is 1500 PLL REFCLK cycles. And then the system will wait about 138us, and then deactive reset signal chiprstn. The signal chiprstn is used to generate output clocks in CRU. After CRU start output clocks, the system waits again for 512cycles (21.3us) to deactive signal rstn_pre, which is used to generate power on reset of all IP.

Fig 13 RK292X reset signals sequence