FUJITSU SEMICONDUCTOR
DATA SHEET

DS07-xxxxx-0.8E

8-bit Proprietary Microcontrollers

CMOS

F²MC®-8FX MB95130H Series

MB95F136HW/F136TW/F136KW/FV100B-103

■ DESCRIPTION

The MB95130H series is general-purpose, single-chip microcontrollers. In addition to a compact instruction set, the microcontrollers contain a peripheral functions for small package.

■ FEATURES

- F²MC-8FX CPU core
  Instruction set that is optimum to the controllers
  - · Multiplication and division instructions
  - · 16-bit arithmetic operation
  - · Bit test branch instruction
  - · Bit manipulation instructions etc.
- Clock
  - · Main clock
  - · Main PLL clock
  - · Subclock (for dual clock product)
  - · Sub PLL clock (for dual clock product)

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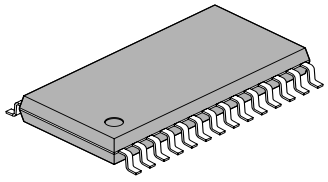
■ PACKAGES

28-pin plastic SOP



(FPT-28P-M17)

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- Timer
  - 8/16-bit compound timer × 1 channels
  - 8/16-bit PPG × 1 channels
  - 16-bit PPG
  - Timebase timer
  - Watch prescaler (for dual clock product)
- LIN-UART
  - Full duplex double buffer
  - Clock asynchronous or synchronous serial transfer capable
- UART/SIO
  - Clock asynchronous or synchronous serial transfer capable
- External interrupt
  - Interrupt by edge detection (rising, falling, or both edges can be selected)
  - Can be used to recover from low-power consumption modes.
- 10-bit A/D converter
  - 10-bit resolution
- Low-power consumption (standby mode)
  - Stop mode
  - Sleep mode
  - Watch mode (for dual clock product)
  - Timebase timer mode
- I/O port: Max 20
  - General-purpose I/O ports (CMOS) : 20 ports

■ PRODUCT LINEUP

Parameter \ Part number		MB95F136HW MB95F136TW MB95F136KW	MB95FV100B-103
Type		FLASH product	EVA product
ROM capacity		32 Kbytes	
RAM capacity		1 Kbytes	3.75 Kbytes
Reset output		No	
Option		Dual clock	Selectable single/dual clock*1
CPU functions		Number of basic instructions : 136 Instruction bit length : 8 bits Instruction length : 1 to 3 bytes Data bit length : 1, 8, and 16 bits Minimum instruction execution time : 0.1 μs (at internal 10 MHz) Interrupt processing time : 0.9 μs (at internal 10 MHz)	
Peripheral functions	Ports (Max 20 ports)	General-purpose I/O port (CMOS) : 20 ports	
	Timebase timer	Interrupt cycle : 0.5 ms, 2.05 ms, 8.2 ms, 32.8 ms (at main oscillation clock 4 MHz)	
	Watchdog timer	Reset generated cycle At main oscillation clock 10 MHz : Minimum 105 ms At sub oscillation clock 32.768 kHz (for dual clock product) : Minimum 250 ms	
	Wild register	Capable of replacing 3 bytes of data	
	UART/SIO	Data transfer capable in UART/SIO Full duplex double buffer, variable data length (5/6/7/8-bit), built-in baud rate generator Transfer rate : 2400 bps to 125000 bps (at machine clock 10 MHz) NRZ type transfer format, error detected function LSB-first or MSB-first can be selected. Clock synchronous (SIO) or clock asynchronous (UART) data transfer capable	
	LIN-UART	Dedicated reload timer allowing a wide range of communication speeds to be set. Capable of data transfer synchronous or asynchronous to clock signal. LIN functions available as the LIN master or LIN slave.	
	A/D converter (8 channels)	8-bit or 10-bit resolution can be selected.	
	8/16-bit compound timer (1 channels)	Each channel of the timer can be used as "8-bit timer × 2 channels" or "16-bit timer × 1 channel". Built-in timer function, PWC function, PWM function, capture function and square waveform output Count clock : 7 internal clocks and external clock can be selected.	

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Parameter \ Part number		MB95F136HW MB95F136TW MB95F136KW	MB95FV100B-103
Peripheral functions	16-bit PPG	PWM mode or one-shot mode can be selected. Counter operating clock : Eight selectable clock sources Support for external trigger start	
	8/16-bit PPG (2 channels)	Each channel of the PPG can be used as "8-bit PPG × 2 channels" or "16-bit PPG × 1 channel". Counter operating clock : Eight selectable clock sources	
	Watch counter (for dual clock product)	Count clock : Four selectable clock sources (125ms, 250ms, 500ms, or 1s) Counter value can be set from 0 to 63. (Capable of counting for 1 minute)	
	Watch prescaler (for dual clock product)	Four selectable interval times (125 ms, 250 ms, 500 ms, or 1 s)	
	External interrupt (8 channels)	Interrupt by edge detection (rising, falling, or both edges can be selected) Can be used to recover from standby modes.	
Standby mode		Sleep, stop, watch, and timebase timer	

*1 : Change by the switch on MCU board.

*2 : Specify clock mode when ordering MASK ROM.

■ PACKAGES AND CORRESPONDING PRODUCTS

Part number / Package	MB95F136HW MB95F136TW MB95F136KW	MB95FV100B-103
FPT-28P-M17	○	×
BGA-224P-M08	×	○

○ : Available
× : Unavailable

■ DIFFERENCES AMONG PRODUCTS AND NOTES ON SELECTING PRODUCTS

• Notes on Using EVA Products

The EVA product has not only the functions of the MB95130H series but also those of other products to support software development for multiple series and products of F²MC-8FX family. The I/O addresses for peripheral resources not used by the MB95130H series are therefore access-barred. Read/write access to these access-barred addresses may cause peripheral resources supposed to be unused to operate, resulting in unexpected malfunctions of hardware or software.

Take particular care not to use word, long word, or similar access to read or write odd numbered bytes in the prohibited areas.

Note that the values read from barred addresses are different between the EVA product and the FLASH or MASK product. Therefore, the data must not be used for software processing.

The EVA product does not support the functions of some bits in single-byte registers. Read/write access to these bits does not cause hardware malfunctions. Since the EVA, FLASH, and MASK products are designed to behave completely the same way in terms of hardware and software, you do not have to pay special attention to specific products.

• Difference of Memory Spaces

If the amount of memory on the EVA product is different from that of the FLASH or MASK product, carefully check the difference in the amount of memory from the product to be actually used when developing software.

• Current Consumption

- The current consumption of FLASH product is typically greater than for MASK product.
- For details of current consumption, refer to "■ ELECTRICAL CHARACTERISTICS".

• Package

For details of information on each package, see "■ PACKAGE DIMENSIONS".

• Operating voltage

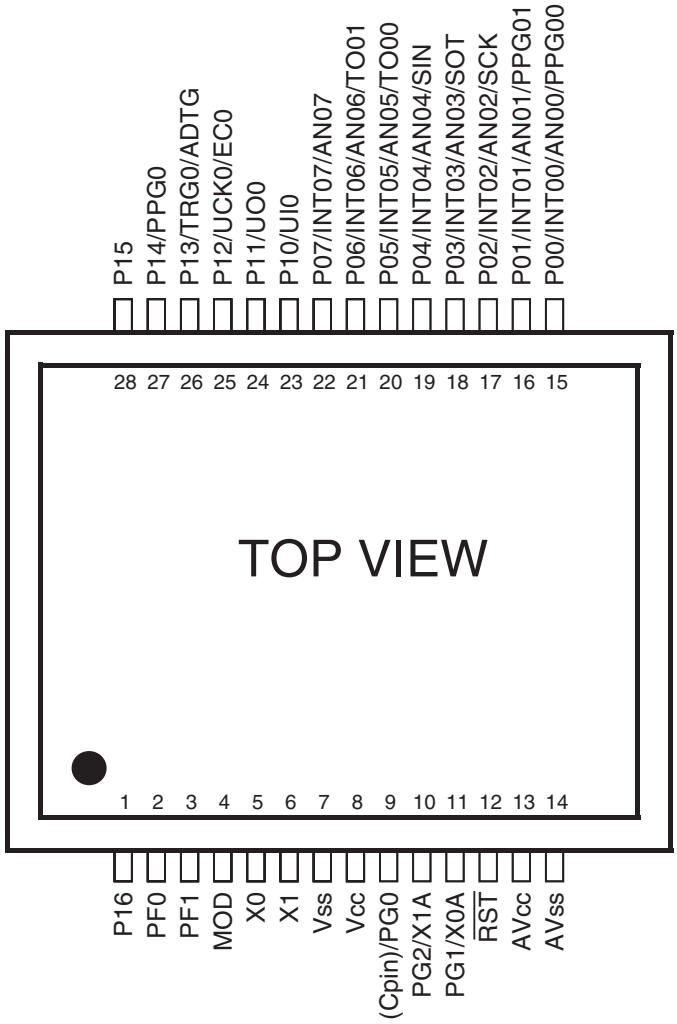
The operating voltage are different among the EVA, FLASH and MASK products.

For details of operating voltage, refer to "■ ELECTRICAL CHARACTERISTICS"

• Difference between $\overline{\text{RST}}$ and MOD pins

The $\overline{\text{RST}}$ and MOD pins are hysteresis inputs on the MASK product. A pull-down resistor is provided for the MOD pin of the MASK product.

■ PIN ASSIGNMENTS



(FPT-28P-M17)

■ PIN DESCRIPTION

Pin no.	Pin name	Circuit type	Description
1	P16	H	General-purpose I/O port.
2	PF0/HC10	K	General-purpose I/O port. Large current port.
3	PF1/HC11		
4	MOD	B	Operation mode specification pin.
5	X0	A	Crystal oscillation pin.
6	X1		
7	Vss	-	Power supply (GND) pin.
8	Vcc	-	Power supply pin.
9	PG0/(Cpin)	H	General-purpose I/O port (at 3 V). Capacitance connection pin (at 5 V).
10	X1A/PG2	A/H	Crystal oscillation pin (32KHz). Single clock product is general-purpose port.
11	X0A/PG1		
12	$\overline{\text{RST}}$	B'	Reset pin.
13	AVcc	-	Power supply pin for A/D.
14	AVss	-	Power supply (GND) pin for A/D.
15	P00/INT00/ AN00/PPG00	D	General-purpose I/O port. These pins are also used for external interrupt input (INT00), A/D analog input (AN00) and 8/16-bit PPG ch0 output (PPG00).
16	P01/INT01/ AN01/PPG01		General-purpose I/O port. These pins are also used for external interrupt input (INT01), A/D analog input (AN01) and 8/16-bit PPG ch0 output (PPG01).
17	P02/INT02/ AN02/SCK		General-purpose I/O port. These pins are also used for external interrupt input (INT02), A/D analog input (AN02) and LIN UART clock I/O(SCK).
18	P03/INT03/ AN03/SOT		General-purpose I/O port. These pins are also used for external interrupt input (INT03), A/D analog input (AN03) and LIN UART data output (SOT).
19	P04/INT04/ AN04/SIN	E	General-purpose I/O port. These pins are also used for external interrupt input (INT04), A/D analog input (AN04) and LIN UART data input (SIN).
20	P05/INT05/ AN05/T000	D	General-purpose I/O port. These pins are also used for external interrupt input (INT05, INT06), A/D analog input (AN05, AN06) and 8/16-bit compound timer ch0 output (TO00, TO01).
21	P06/INT06/ AN06/T001		
22	P07/INT07/ AN07		General-purpose I/O port. These pins are also used for external interrupt input (INT07), A/D analog input (AN07).

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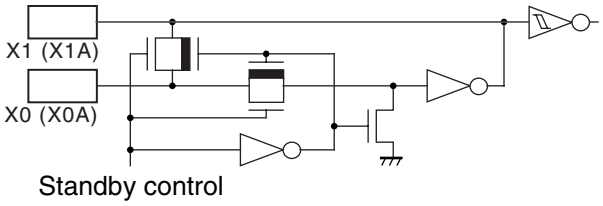
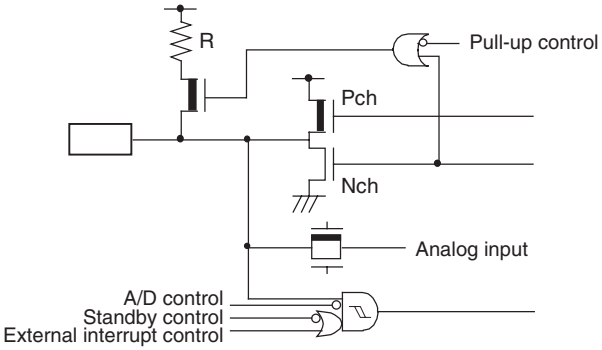
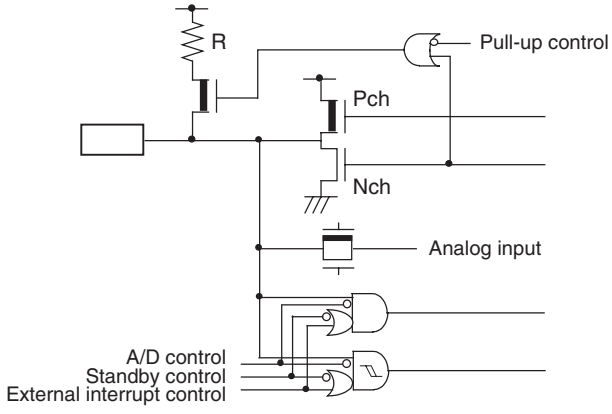
Pin no.	Pin name	Circuit type	Description
23	P10/U10	G	General-purpose I/O port. These pins are also used for UART/SIO ch0 data input.
24	P11/U00	H	General-purpose I/O port. These pins are also used for UART/SIO ch0 data output.
25	P12/UCK0/ EC0		General-purpose I/O port. These pins are also used for UART/SIO ch0 clock I/O (UCK0) and 8/16-bit compound timer ch0 clock input (EC0).
26	P13/TRG0/ ADTG		General-purpose I/O port. These pins are also used for 16-bit PPG ch0 trigger input (TRG0) and A/D trigger input (ADTG).
27	P14/PPG0		General-purpose I/O port. These pins are also used for 16-bit PPG ch0 output.
28	P15		General-purpose I/O port.

■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		· Oscillation circuit · Main-clock Feedback resistance value : approx. 1 MΩ · Sub-clock Feedback resistance : 10 MΩ (MB95FV100B:without dumping resistance)
B		· Only for input · Hysteresis input only for MASK product · With pull-down resistor only for MASK product
B'		· Hysteresis input only for MASK product
D		· CMOS output · Hysteresis input · Analog input · Pull-up control is available.
E		· CMOS output · CMOS intput · Hysteresis input · Analog input · Pull-up control is available.

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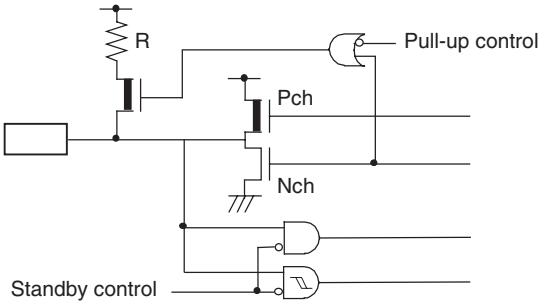
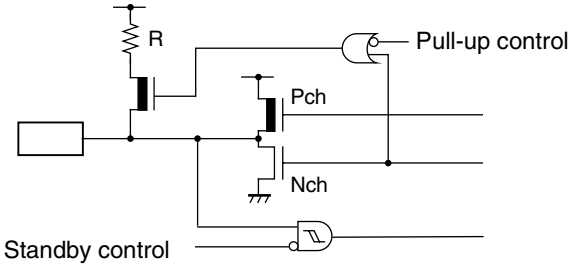
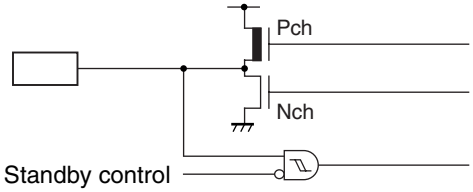
Type	Circuit	Remarks
G		· CMOS output · CMOS input · Hysteresis input · With pull-up control
H		· CMOS output · Hysteresis input · With pull-up control
K		· CMOS output · Hysteresis input

■ HANDLING DEVICES

- Preventing Latchup

  Care must be taken to ensure that maximum voltage ratings are not exceeded when it is used.

  Latchup may occur on CMOS ICs if voltage higher than V_{CC} or lower than V_{SS} is applied to input and output pins other than medium- and high-withstand voltage pins or if higher than the rating voltage is applied between V_{CC} and V_{SS}.

  When latchup occurs, power supply current increases rapidly and might thermally damage elements.

  Also, take care to prevent the analog power supply voltage (AV_{CC}) and analog input voltage from exceeding the digital power supply voltage (V_{CC}) when the analog system power supply is turned on or off.

- Stable Supply Voltage

  Supply voltage should be stabilized.

  A sudden change in power-supply voltage may cause a malfunction even within the guaranteed operating range of the Vcc power-supply voltage.

  For stabilization, in principle, keep the variation in Vcc ripple (p-p value) in a commercial frequency range (50 Hz to 60 Hz) not to exceed 10% of the Vcc value and suppress the voltage variation so that the transient variation rate does not exceed 0.1 V/ms during a momentary change such as when the power supply is switched.

- Treatment of Unused Input Pin

  An unused input pin may cause a malfunction if it is left open. It should be connected to a pull-up or pull-down resistor.

- Treatment of Power Supply Pins on A/D Converter

  Connect to be $AV_{CC} = V_{CC}$ and $AV_{SS} = V_{SS}$ even if the A/D converter is not in use.

- Precautions for Use of External Clock

  Even when an external clock is used, oscillation stabilization wait time is required for power-on reset, wake-up from subclock mode or stop mode.

- Precaution against Noise to the External Reset Pin ($\overline{RST}$)

  An input of a reset pulse below the specified level to the external reset pin ($\overline{RST}$) may cause malfunctions. Be sure not to allow an input of a reset pulse below the specified level to the external reset pin ($\overline{RST}$).

■ PROGRAMMING AND ERASE FLASH MEMORY ON THE MB95F136H

1. Flash Memory

The flash memory is located between 8000_H and $FFFF_H$ in the CPU memory map and incorporates a flash memory interface circuit that allows read access and program access from the CPU to be performed in the same way as mask ROM. Programming and erasing flash memory is also performed via the flash memory interface circuit by executing instructions in the CPU. This enables the flash memory to be updated in place under the control of the CPU, providing an efficient method of updating program and data.

2. Flash Memory Features

- 32 K byte x 8-bit configuration
- Automatic programming algorithm (Embedded algorithm*)
- Data polling and toggle bit for detection of program/erase completion
- Detection of program/erase completion via CPU interrupt
- Compatible with JEDEC-standard commands
- No. of program / erase cycles : Minimum 10,000

* : Embedded Algorithm is a trademark of Advanced Micro Devices.

3. Procedure for Programming and Erasing Flash Memory

Programming and reading flash memory cannot be performed at the same time. Accordingly, to program or erase flash memory, the program must first be copied from flash memory to RAM so that programming can be performed without program access from flash memory.

4. Flash Memory Status Register (FMS)

	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	
Address 072_H	-	-	RDYIRQ	RDY	Reserved	IRQEN	WRE	Reserved	Initial value 000X0000B
	-	-	R/W	R	R	R/W	R/W	R	

5. Memory Space

The memory space for the CPU access and for the parallel flash programmer access is listed below.

Memory size	CPU address	Programmer address
32 K bytes	$FFFF_H$ to 8000_H	$1FFFF_H$ to 18000_H

6. Flash Programmer Adaptor and Recommended Flash Programmers

Package	Applicable adapter model	Parallel programmers
FPT-28P-M17	TEF110-95F136HSPF	AF9708 (Ver 02.35G or more) AF9709/B (Ver 02.35G or more) AF9723+AF9834 (Ver 02.08E or more)

Notes: • For information on applicable adapter models and parallel programmers, contact the following:
Flash Support Group, Inc. TEL: (81)53-428-8380

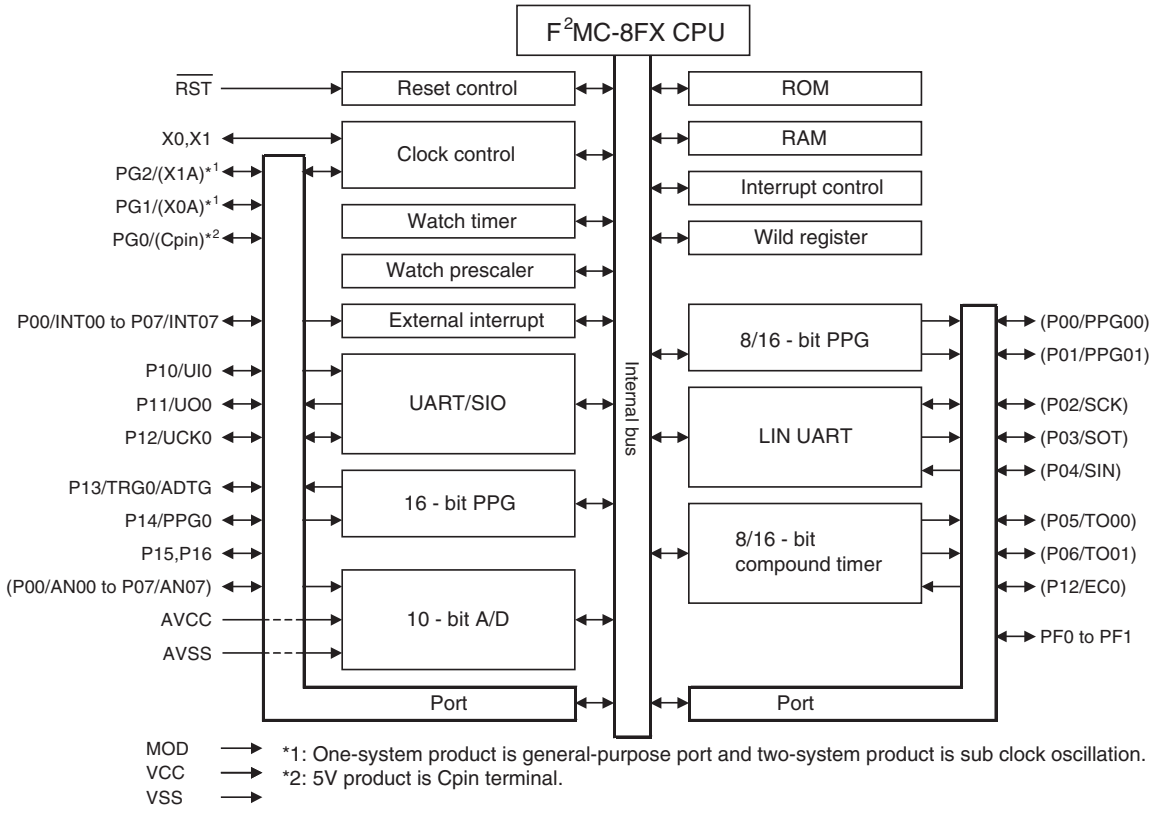
7. Flash Content Protection

Flash content can be read using parallel / serial programmer if the flash content protection mechanism is not activated.

One predefined area of the flash (8000_H) is assigned to be used for preventing the read access of flash content. If the protection code "01_H" is written in this address (8000_H), the flash content cannot be read by any parallel / serial programmer.

Note : The program written into the flash cannot be verified once the flash protection code is written ("01_H" in 8000_H). It is advised to write the flash protection code at last.

■ BLOCK DIAGRAM



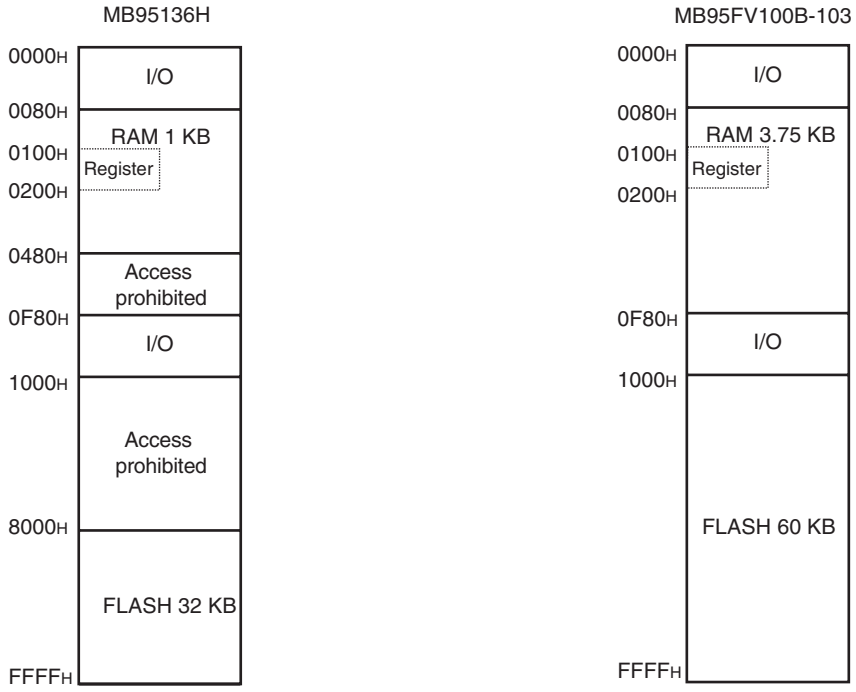
* : Single-system product is general-purpose port, and dual-system product is subclock oscillation.

■ CPU CORE

1. Memory space

Memory space of the MB95130H series is 64 Kbytes and consists of I/O area, data area, and program area. The memory space includes special-purpose areas such as the general-purpose registers and vector table. Memory map of the MB95130H series shown in below.

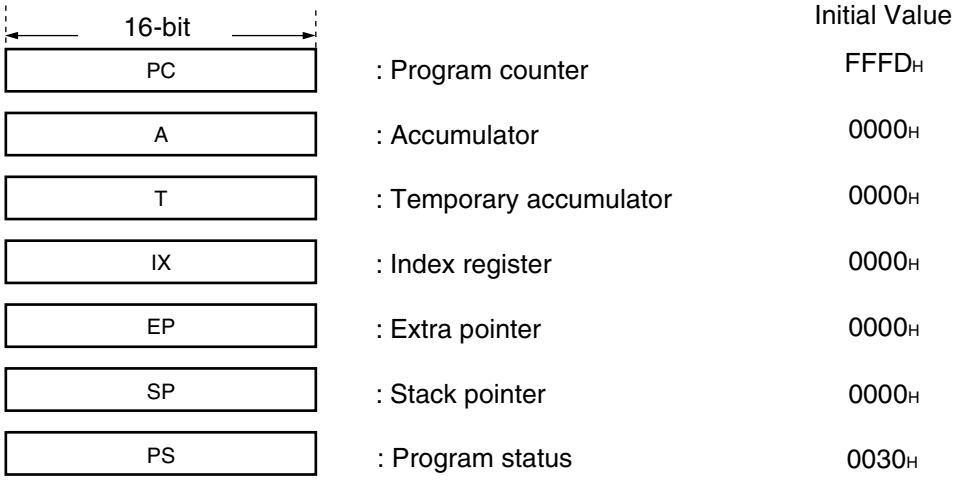
· Memory Map



2. Register

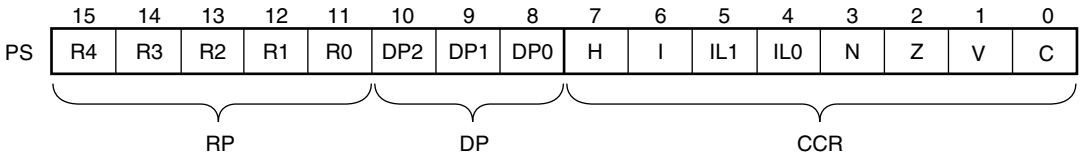
The MB95130H series has two types of registers; dedicated registers in the CPU and general-purpose registers in the memory. The dedicated registers are as follows:

Program counter (PC)	:	A 16-bit register to indicate locations where instructions are stored.
Accumulator (A)	:	A 16-bit register for temporary storage of arithmetic operations. In the case of an 8-bit data processing instruction, the lower one byte is used.
Temporary accumulator (T)	:	A 16-bit register which performs arithmetic operations with the accumulator. In the case of an 8-bit data processing instruction, the lower one byte is used.
Index register (IX)	:	A 16-bit register for index modification
Extra pointer (EP)	:	A 16-bit pointer to point to a memory address.
Stack pointer (SP)	:	A 16-bit register to indicate a stack area.
Program status (PS)	:	A 16-bit register for storing a register bank pointer, a direct bank pointer, and a condition code register



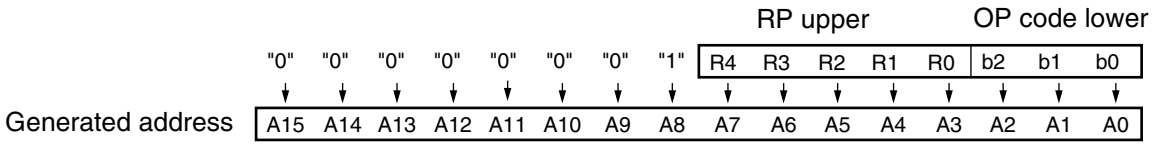
The PS can further be divided into higher 8 bits for use as a register bank pointer (RP) and a direct bank pointer (DP) and the lower 8 bits for use as a condition code register (CCR). (See the diagram below.)

· Structure of the program status



The RP indicates the address of the register bank currently being used. The relationship between the content of RP and the real address conforms to the conversion rule illustrated below:

- Rule for Conversion of Actual Addresses in the General-purpose Register Area



The DP specifies the area for mapping instructions (16 different instructions such as MOV A, dir) using direct addresses to 0080_H to $00FF_H$.

Direct bank pointer (DP2 to DP0)	Specified address area	Mapping area
Don't care	0000_H to $007F_H$	0000_H to $007F_H$ (without mapping)
000_B (initial value)	0080_H to $00FF_H$	0080_H to $00FF_H$ (without mapping)
001_B		0100_H to $017F_H$
010_B		0180_H to $01FF_H$
011_B		0200_H to $027F_H$
100_B		0280_H to $02FF_H$
101_B		0300_H to $037F_H$
110_B		0380_H to $03FF_H$
111_B		0400_H to $047F_H$

The CCR consists of the bits indicating arithmetic operation results or transfer data contents and the bits that control CPU operations at interrupt.

H flag : Set to "1" when a carry or a borrow from bit 3 to bit 4 occurs as a result of an arithmetic operation. Cleared to "0" otherwise. This flag is for decimal adjustment instructions.

I flag : Interrupt is enabled when this flag is set to "1". Interrupt is disabled when this flag is set to "0". The flag is set to "0" when reset.

IL1, IL0 : Indicates the level of the interrupt currently enabled. Processes an interrupt only if its request level is higher than the value indicated by this bit.

IL1	IL0	Interrupt level	Priority
0	0	0	High
0	1	1	↕
1	0	2	
1	1	3	Low = no interruption

N flag : Set to "1" if the MSB is set to "1" as the result of an arithmetic operation. Cleared to "0" when the bit is set to "0".

Z flag : Set to "1" when an arithmetic operation results in 0. Cleared to "0" otherwise.

V flag : Set to "1" if the complement on 2 overflows as a result of an arithmetic operation. Cleared to "0" otherwise.

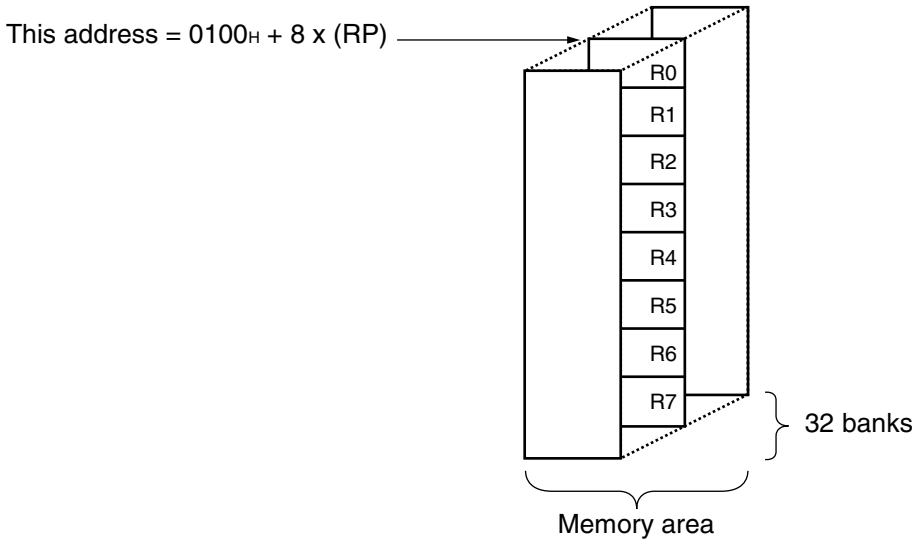
C flag : Set to "1" when a carry or a borrow from bit 7 occurs as a result of an arithmetic operation. Cleared to "0" otherwise. Set to the shift-out value in the case of a shift instruction.

The following general-purpose registers are provided:

General-purpose registers: 8-bit data storage registers

The general-purpose registers are 8 bits and located in the register banks on the memory. One bank contains eight registers. Up to a total of 32 banks can be used on the MB95130H series. The bank currently in use is indicated by the register bank pointer (RP).

· Register Bank Configuration



■ I/O MAP

Address	Register abbreviation	Register name	R/W	Initial value
0000_H	PDR0	Port 0 data register	R/W	00000000_B
0001_H	DDR0	Port 0 direction register	R/W	00000000_B
0002_H	PDR1	Port 1 data register	R/W	00000000_B
0003_H	DDR1	Port 1 direction register	R/W	00000000_B
0004_H	—	(Vacancy)	—	—
0005_H	WATR	Oscillation stabilization wait time setting register	R/W	11111111_B
0006_H	PLLC	PLL control register	R/W	00000000_B
0007_H	SYCC	System clock control register	R/W	$1010X011_B$
0008_H	STBC	Standby control register	R/W	00000000_B
0009_H	RSRR	Reset source register	R	$XXXXXXXX_B$
$000A_H$	TBTC	Timebase timer control register	R/W	00000000_B
$000B_H$	WPCR	Watch prescaler control register	R/W	00000000_B
$000C_H$	WDTC	Watchdog timer control register	R/W	00000000_B
$000D_H$ to 0027_H	—	(Vacancy)	—	—
0028_H	PDRF	Port F data register	R/W	00000000_B
0029_H	DDRF	Port F direction register	R/W	00000000_B
$002A_H$	PDRG	Port G data register	R/W	00000000_B
$002B_H$	DDRG	Port G direction register	R/W	00000000_B
$002C_H$	PUL0	Port 0 pull-up register	R/W	00000000_B
$002D_H$	PUL1	Port 1 pull-up register	R/W	00000000_B
$002E_H$ to 0034_H	—	(Vacancy)	—	—
0035_H	PULG	Port G pull-up register	R/W	00000000_B
0036_H	T01CR1	8/16-bit compound timer 01 control status register 1 ch0	R/W	00000000_B
0037_H	T00CR1	8/16-bit compound timer 00 control status register 1 ch0	R/W	00000000_B
0038_H	—	(Vacancy)	—	—
0039_H	—	(Vacancy)	—	—
$003A_H$	PC01	8/16-bit PPG1 control register ch0	R/W	00000000_B
$003B_H$	PC00	8/16-bit PPG0 control register ch0	R/W	00000000_B
$003C_H$ to 0041_H	—	(Vacancy)	—	—

(Continued)

Address	Register abbreviation	Register name	R/W	Initial value
0042H	PCNTH0	16-bit PPG status control register (Upper byte) ch0	R/W	00000000B
0043H	PCNTL0	16-bit PPG status control register (Lower byte) ch0	R/W	00000000B
0044H to 0047H	—	(Vacancy)	—	—
0048H	EIC00	External interrupt circuit control register ch0/1	R/W	00000000B
0049H	EIC10	External interrupt circuit control register ch2/3	R/W	00000000B
004AH	EIC20	External interrupt circuit control register ch4/5	R/W	00000000B
004BH	EIC30	External interrupt circuit control register ch6/7	R/W	00000000B
004CH to 004FH	—	(Vacancy)	—	—
0050H	SCR	LIN-UART serial control register	R/W	00000000B
0051H	SMR	LIN-UART serial mode register	R/W	00000000B
0052H	SSR	LIN-UART serial status register	R/W	00001000B
0053H	RDR/TDR	LIN-UART reception/transmission data register	R/W	00000000B
0054H	ESCR	LIN-UART extended status control register	R/W	00000100B
0055H	ECCR	LIN-UART extended communication control register	R/W	000000XXB
0056H	SMC10	UART/SIO serial mode control register 1 ch0	R/W	00000000B
0057H	SMC20	UART/SIO serial mode control register 2 ch0	R/W	00100000B
0058H	SSR0	UART/SIO serial status register ch0	R/W	00000001B
0059H	TDR0	UART/SIO serial output data register ch0	R/W	00000000B
005AH	RDR0	UART/SIO serial input data register ch0	R	00000000B
005BH to 006B	—	(Vacancy)	—	—
006CH	ADC1	A/D control register 1	R/W	00000000B
006DH	ADC2	A/D control register 2	R/W	00000000B
006EH	ADDH	A/D data register (Upper byte)	R/W	00000000B
006FH	ADDL	A/D data register (Lower byte)	R/W	00000000B
0070H	WCSR	Watch counter status register	R/W	00000000B
0071H	—	(Vacancy)	—	—
0072H	FSR	Flash memory status register	R/W	000X0000B
0073H	SWRE0	Flash memory sector writing control register 0	R/W	00000000B
0074H	SWRE1	Flash memory sector writing control register 1	R/W	00000000B
0075H	—	(Vacancy)	—	—

(Continued)

Address	Register abbreviation	Register name	R/W	Initial value
0076H	WREN	Wild register address compare enable register	R/W	00000000B
0077H	WROR	Wild register data test setting register	R/W	00000000B
0078H	—	(Mirror of register bank pointer (RP) and direct bank pointer (DP))	—	—
0079H	ILR0	Interrupt level setting register 0	R/W	11111111B
007AH	ILR1	Interrupt level setting register 1	R/W	11111111B
007BH	ILR2	Interrupt level setting register 2	R/W	11111111B
007CH	ILR3	Interrupt level setting register 3	R/W	11111111B
007DH	ILR4	Interrupt level setting register 4	R/W	11111111B
007EH	ILR5	Interrupt level setting register 5	R/W	11111111B
007FH	—	(Vacancy)	—	—
0F80H	WRARH0	Wild register address setting register (Upper byte) ch0	R/W	00000000B
0F81H	WRARL0	Wild register address setting register (Lower byte) ch0	R/W	00000000B
0F82H	WRDR0	Wild register data setting register ch0	R/W	00000000B
0F83H	WRARH1	Wild register address setting register (Upper byte) ch1	R/W	00000000B
0F84H	WRARL1	Wild register address setting register (Lower byte) ch1	R/W	00000000B
0F85H	WRDR1	Wild register data setting register ch1	R/W	00000000B
0F86H	WRARH2	Wild register address setting register (Upper byte) ch2	R/W	00000000B
0F87H	WRARL2	Wild register address setting register (Lower byte) ch2	R/W	00000000B
0F88H	WRDR2	Wild register data setting register ch2	R/W	00000000B
0F89H to 0F91H	—	(Vacancy)	—	—
0F92H	T01CR0	8/16-bit compound timer 01 control status register 0 ch0	R/W	00000000B
0F93H	T00CR0	8/16-bit compound timer 00 control status register 0 ch0	R/W	00000000B
0F94H	T01DR	8/16-bit compound timer 01 data register ch0	R/W	00000000B
0F95H	T00DR	8/16-bit compound timer 00 data register ch0	R/W	00000000B
0F96H	TMCR0	8/16-bit compound timer 00/01 timer mode control register ch0	R/W	00000000B
0F97H to 0F9BH	—	(Vacancy)	—	—
0F9CH	PPS01	8/16-bit PPG1 cycle setting buffer register ch0	R/W	11111111B
0F9DH	PPS00	8/16-bit PPG0 cycle setting buffer register ch0	R/W	11111111B
0F9EH	PDS01	8/16-bit PPG1 duty setting buffer register ch0	R/W	11111111B
0F9FH	PDS00	8/16-bit PPG0 duty setting buffer register ch0	R/W	11111111B

(Continued)

Address	Register abbreviation	Register name	R/W	Initial value
0FA0H to 0FA3H	—	(Vacancy)	—	—
0FA4H	PPGS	8/16-bit PPG starting register	R/W	00000000B
0FA5H	REVC	8/16-bit PPG output inversion register	R/W	00000000B
0FA6H to 0FA9H	—	(Vacancy)	—	—
0FAAH	PDCRH0	16-bit PPG down counter register (Upper byte) ch0	R	00000000B
0FABH	PDCRL0	16-bit PPG down counter register (Lower byte) ch0	R	00000000B
0FACH	PCSRH0	16-bit PPG cycle setting buffer register (Upper byte) ch0	R/W	11111111B
0FADH	PCSRL0	16-bit PPG cycle setting buffer register (Lower byte) ch0	R/W	11111111B
0FAEH	PDUTH0	16-bit PPG duty setting buffer register (Upper byte) ch0	R/W	11111111B
0FAFH	PDUTL0	16-bit PPG duty setting buffer register (Lower byte) ch0	R/W	11111111B
0FB0H to 0FBBH	—	(Vacancy)	—	—
0FBCH	BGR1	LIN-UART baud rate generator register 1	R/W	00000000B
0FBDH	BGR0	LIN-UART baud rate generator register 0	R/W	00000000B
0FBEH	PSSR0	UART/SIO prescaler selection register ch0	R/W	00000000B
0FBFH	BRSR0	UART/SIO baud rate setting register ch0	R/W	00000000B
0FC0H to 0FC2H	—	(Vacancy)	—	—
0FC3H	AIDRL	A/D input disable register (Lower byte)	R/W	00000000B
0FC4H to 0FE2H	—	(Vacancy)	—	—
0FE3H	WCDR	Watch counter data register	R/W	00111111B
0FE4H to 0FE9H	—	(Vacancy)	—	—
0FEAH	CSVCR	Clock supervisor control register	R/W	00011100B
0FEBH to 0FEDH	—	(Vacancy)	—	—
0FEEH	ILSR	Input level select register	R/W	00000000B
0FEFH	WICR	Interrupt pin control register	R/W	01000000B
0FF0H to 0FFFH	—	(Vacancy)	—	—

· Read/write access symbols

R/W : Readable and Writable

R : Read only

W : Write only

· Initial value symbols

0 : The initial value of this bit is "0".

1 : The initial value of this bit is "1".

X : The initial value of this bit is undefined.

■ INTERRUPT SOURCE TABLE

Interrupt source	Interrupt request number	Vector table address		Bit name of interrupt level setting register	Same level priority order (at simultaneous occurrence)
		Upper	Lower		
External interrupt ch0	IRQ0	FFFA$_H$	FFFB$_H$	L00 [1 : 0]	High
External interrupt ch4					
External interrupt ch1	IRQ1	FFF8$_H$	FFF9$_H$	L01 [1 : 0]	
External interrupt ch5					
External interrupt ch2	IRQ2	FFF6$_H$	FFF7$_H$	L02 [1 : 0]	
External interrupt ch6					
External interrupt ch3	IRQ3	FFF4$_H$	FFF5$_H$	L03 [1 : 0]	
External interrupt ch7					
UART/SIO ch0	IRQ4	FFF2$_H$	FFF3$_H$	L04 [1 : 0]	
8/16-bit compound timer ch0 (Lower)	IRQ5	FFF0$_H$	FFF1$_H$	L05 [1 : 0]	
8/16-bit compound timer ch0 (Upper)	IRQ6	FFEE$_H$	FFEF$_H$	L06 [1 : 0]	
LIN-UART (reception)	IRQ7	FFEC$_H$	FFED$_H$	L07 [1 : 0]	
LIN-UART (transmission)	IRQ8	FFEA$_H$	FFEB$_H$	L08 [1 : 0]	
(Unused)	IRQ9	FFE8$_H$	FFE9$_H$	L09 [1 : 0]	
(Unused)	IRQ10	FFE6$_H$	FFE7$_H$	L10 [1 : 0]	
(Unused)	IRQ11	FFE4$_H$	FFE5$_H$	L11 [1 : 0]	
8/16-bit PPG ch0 (Upper)	IRQ12	FFE2$_H$	FFE3$_H$	L12 [1 : 0]	
8/16-bit PPG ch0 (Lower)	IRQ13	FFE0$_H$	FFE1$_H$	L13 [1 : 0]	
(Unused)	IRQ14	FFDE$_H$	FFDF$_H$	L14 [1 : 0]	
16-bit PPG ch0	IRQ15	FFDC$_H$	FFDD$_H$	L15 [1 : 0]	
(Unused)	IRQ16	FFDA$_H$	FFDB$_H$	L16 [1 : 0]	
(Unused)	IRQ17	FFD8$_H$	FFD9$_H$	L17 [1 : 0]	
10-bit A/D converter	IRQ18	FFD6$_H$	FFD7$_H$	L18 [1 : 0]	
Timebase timer	IRQ19	FFD4$_H$	FFD5$_H$	L19 [1 : 0]	
Watch prescaler/counter	IRQ20	FFD2$_H$	FFD3$_H$	L20 [1 : 0]	
(Unused)	IRQ21	FFD0$_H$	FFD1$_H$	L21 [1 : 0]	
(Unused)	IRQ22	FFCE$_H$	FFCF$_H$	L22 [1 : 0]	
FLASH	IRQ23	FFCC$_H$	FFCD$_H$	L23 [1 : 0]	Low

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1	Vcc, AVcc	Vss − 0.3	Vss + 6.0	V	*2
	AVR	Vss − 0.3	Vss + 6.0		*2 MB95FV100B-103 only
Input voltage*1	V_I	Vss − 0.3	Vss + 6.0	V	*3
Output voltage*1	V_O	Vss − 0.3	Vss + 6.0	V	*3
Maximum clamp current	I_{CLAMP}	− 2.0	+ 2.0	mA	Applicable to pins*4
Total maximum clamp current	$\Sigma\lvert I_{CLAMP}\rvert$	—	20	mA	Applicable to pins*4
"L" level maximum output current	I_{OL1}	—	15	mA	Other than PF0 to PF1
	I_{OL2}		15		PF0 to PF1
"L" level average current	I_{OLAV1}	—	4	mA	Other than PF0 to PF1 Average output current = operating current × operating ratio (1 pin)
	I_{OLAV2}		12		PF0 to PF1 Average output current = operating current × operating ratio (1 pin)
"L" level total maximum output current	ΣI_{OL}	—	100	mA	
"L" level total average output current	ΣI_{OLAV}	—	50	mA	Total average output current = operating current × operating ratio (total of pins)
"H" level maximum output current	I_{OH1}	—	− 15	mA	Other than PF0 to PF1
	I_{OH2}		− 15		PF0 to PF1
"H" level average current	I_{OHAV1}	—	− 4	mA	Other than PF0 to PF1 Average output current = operating current × operating ratio (1 pin)
	I_{OHAV2}		− 8		PF0 to PF1 Average output current = operating current × operating ratio (1 pin)
"H" level total maximum output current	ΣI_{OH}	—	− 100	mA	
"H" level total average output current	ΣI_{OHAV}	—	− 50	mA	Total average output current = operating current × operating ratio (total of pins)
Power consumption	Pd	—	320	mW	
Operating temperature	T_A	− 40	+ 85	°C	Other than MB95FV100B-103
Storage temperature	Tstg	− 55	+ 150	°C	

(Continued)

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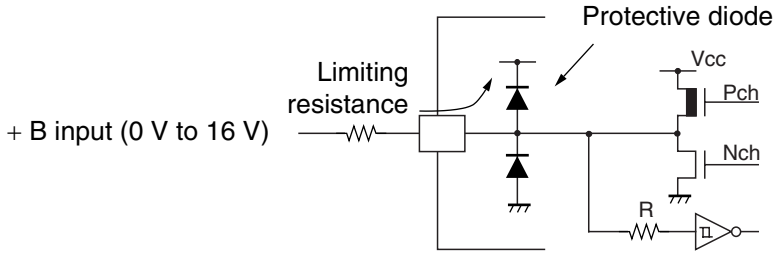
*1 : The parameter is based on $AV_{CC} = V_{SS} = 0.0$ V.

*2 : Apply equal potential to AVcc and Vcc. AVR should not exceed AVcc + 0.3 V.

*3 : V_{I1} and V_O should not exceed $V_{CC} + 0.3$ V. V_{I1} must not exceed the rating voltage. However, if the maximum current to/from an input is limited by some means with external components, the I_{CLAMP} rating supersedes the V_{I1} rating.

*4 :
- Applicable to pins : P00 to P07, P10 to P15, PF0 to PF1
- Use within recommended operating conditions.
- Use at DC voltage (current).
- The + B signal should always be applied a limiting resistance placed between the + B signal and the microcontroller.
- The value of the limiting resistance should be set so that when the + B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
- Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the VCC pin, and this may affect other devices.
- Note that if the + B signal is inputted when the microcontroller power supply is off (not fixed at 0 V), the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the + B input is applied during power-on, the power supply is provided from the pins and the resulting power supply voltage may not be sufficient to operate the power-on reset.
- Care must be taken not to leave the + B input pin open.
- Sample recommended circuits :

· Input/Output Equivalent Circuits



WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2. Recommended Operating Conditions

(AV_{SS} = V_{SS} = 0.0 V)

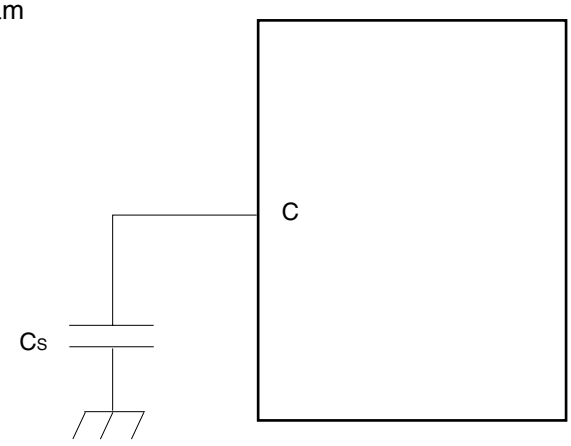
Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Power supply voltage	V_{CC}, AV_{CC}	2.5*1	5.5*2	V	At normal operating
		2.6	5.5		MB95FV100B-103
		2.4	5.5*2		Retain status of stop operation
Smoothing capacitor	C_S	0.1	1.0	µF	*3
Operating temperature	T_A	− 40	+ 85	°C	Other than MB95FV100B-103

*1 : The values vary with the operating frequency.

*2 : The value is 2.9 V when the low voltage detection reset is used.

*3 : Use a ceramic capacitor or a capacitor with equivalent frequency characteristics. A bypass capacitor of V_{CC} pin must have a capacitance value higher than C_S. For connection of smoothing capacitor C_S, see the diagram below

· C pin connection diagram



WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

3. DC Characteristics

(Vcc = AVcc = 5.0 V, AVss = Vss = 0.0 V, T_A = − 40 °C to + 85 °C [MB95FV100B-103 is T_A = +25 °C])

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage	V_{IH1}	P04(at SIN selection), P10(at UI selection)	*1	0.7 Vcc	—	Vcc + 0.3	V	At selecting of CMOS input level (hysteresis input)
	V_{IHS1}	P00 to P07, P10 to P15, PF0 to PF1, PG1, PG2	*1	0.8 Vcc	—	Vcc + 0.3	V	Hysteresis input
	V_{IHM}	$\overline{RST}$, MOD	—	0.7 Vcc	—	Vcc + 0.3	V	CMOS input (FLASH product)
			—	0.8 Vcc	—	Vcc + 0.3	V	Hysteresis input (MASK product)
"L" level input voltage	V_{IL}	P04(at SIN selection), P10(at UI selection)	*1	Vss − 0.3	—	0.3 Vcc	V	At selecting of CMOS input level (hysteresis input)
	V_{ILS}	P00 to P07, P10 to P16, PF0 to PF1, PG1, PG2	*1	Vss − 0.3	—	0.2 Vcc	V	Hysteresis input
	V_{ILM}	$\overline{RST}$, MOD	—	Vss − 0.3	—	0.3 Vcc	V	CMOS input (FLASH product)
			—	Vss − 0.3	—	0.2 Vcc	V	Hysteresis input (MASK product)
"H" level output voltage	V_{OH1}	Output pin other than PF0 to PF1	I_{OH} = − 4.0 mA	4.0	—	—	V	
	V_{OH2}	PF0 to PF1	I_{OH} = − 8.0 mA	4.0	—	—	V	
"L" level output voltage	V_{OL1}	Output pin other than PF0 to PF1	I_{OL} = 4.0 mA	—	—	0.4	V	When no clock supervisor is specified
	V_{OL2}	PF0 to PF1	I_{OL} = 12 mA	—	—	0.4	V	
Input leakage current (High-Z output leakage current)	I_{LI}	P00 to P07, P10 to P16, PF0 to PF1, PG0 to PG1	0.0 V < V_I < Vcc	− 5	—	+ 5	μA	When no pull-up resistor is specified

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(Vcc = AVcc = 5.0 V, AVss = Vss = 0.0 V, T_A = − 40 °C to + 85 °C [MB95FV100B-103 is T_A = +25 °C])

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Pull-up resistor	R_{PULL}	P00 to P07, P10 to P16, PF0 to PF1, PG0 to PG1	V_I = 0.0 V	25	50	100	kΩ	When pull-up resistor is specified
Pull-down resistor	R_{MOD}	MOD	V_I = Vcc	50	100	200	kΩ	MASK product only
Power supply current*3	I_{CC}	Vcc (external clock operation)	Vcc=5.5V F_{CH} = 20 MHz fmp = 10 MHz Main clock mode (divided by 2)	—	T.B.D	T.B.D	mA	FLASH product
				—	—	—	mA	MASK product
				—	30	35	mA	FLASH product (at FLASH writing and erasing)
	I_{CCS}		Vcc=5.5V F_{CH} = 20 MHz fmp = 10 MHz Main Sleep mode (divided by 2)	—	T.B.D	T.B.D	mA	
	I_{CCL}		Vcc=5.5V F_{CL} = 32 kHz fmpl = 16 kHz Subclock mode (divided by 2) , T_A = + 25 °C	—	45	100	μA	
	I_{CCLS}		Vcc=5.5V F_{CL} = 32 kHz fmpl = 16 kHz Sub sleep mode (divided by 2) , T_A = + 25 °C	—	10	81	μA	

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(Vcc = AVcc = 5.0 V, AVss = Vss = 0.0 V, T_A = − 40 °C to + 85 °C [MB95FV100B-103 is T_A = +25 °C])

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current*3	I_{CCT}	V_{CC} (external clock operation)	Vcc=5.5V F_{CL} = 32 kHz Watch mode Main stop mode T_A = + 25 °C	—	4.6	27	μA	
	I_{CCMPLL}		Vcc=5.5V F_{CH} = 4 MHz fmp = 10 MHz Main PLL mode (multiplied by 2.5)	—	T.B.D	T.B.D	mA	FLASH product
				—	—	—	mA	MASK product
	I_{CCSPLL}		Vcc=5.5V F_{CL} = 32 kHz fmpl = 128 kHz Sub PLL mode (multiplied by 4), T_A = + 25 °C	—	160	400	μA	
	I_{CTS}		Vcc=5.5V F_{CH} = 10 MHz Timebase timer mode T_A = + 25 °C	—	0.15	1.1	mA	
	I_{CCH}		Vcc=5.5V Substop mode T_A = + 25 °C	—	5	20	μA	
	I_A	AVcc	Vcc=5.5V F_{CH} = 10 MHz At A/D converting	—	2.4	4.7	mA	
	I_{AH}		Vcc=5.5V F_{CH} = 10 MHz At A/D converting stop T_A = + 25 °C	—	1	5	μA	
Input capacitance	C_{IN}	Other than AVcc, AVss, Vcc, and Vss	—	—	5	15	pF	

*1 : The power-supply current is determined by the external clock.

*If you select the "low voltage detection" and "clock supervisor clock" as the option, please adds the value at "9. Low Voltage Detection" and "10. Clock Supervisor Clock" to above supply current.

- Refer to "4. AC characteristics (1) Clock Timing" for F_{CH} and F_{CL}.
- Refer to "4. AC characteristics (2) Source Clock/Machine Clock" for fmp and fmpl.

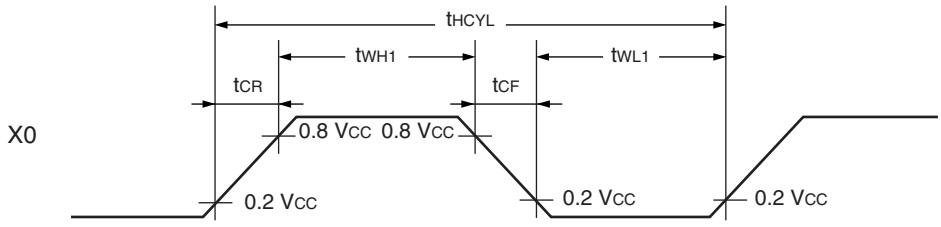
4. AC Characteristics

(1) Clock Timing

(Vcc = 5.0 V, AVss = Vss = 0.0 V, T_A = − 40 °C to + 85 °C)

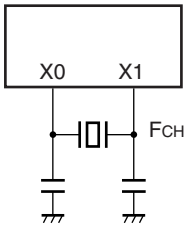
Parameter	Symbol	Pin	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Clock frequency	F_{CH}	X0, X1	—	1	—	10	MHz	When using Main oscillation circuit
				1	—	20	MHz	When using external clock
				3	—	10	MHz	Main PLL multiplied by 1
				3	—	5	MHz	Main PLL multiplied by 2
				3	—	4	MHz	Main PLL multiplied by 2.5
	F_{CL}	X0A, X1A		—	32.768	—	kHz	When using Sub oscillation circuit
				—	32.768	—	kHz	When using sub PLL Vcc = 2.3 V to 3.6 V
Clock cycle time	t_{HCYL}	X0, X1		100	—	1000	ns	When using Main oscillation circuit
				50	—	1000	ns	When using Sub oscillation circuit
	t_{LCYL}	X0A, X1A		—	30.5	—	μs	Subclock
Input clock pulse width	t_{WH1} t_{WL1}	X0		10	—	—	ns	When using external clock Duty ratio is about 30% to 70%.
	t_{WH2} t_{WL2}	X0A		—	15.2	—	μs	
Input clock rise time and fall time	t_{CR} t_{CF}	X0, X0A		—	—	5	ns	When using external clock

• X0 and X1 Timing and Applying Conditions

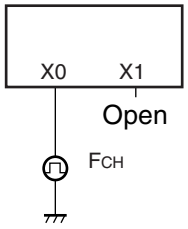


• Main Clock Applying Conditions

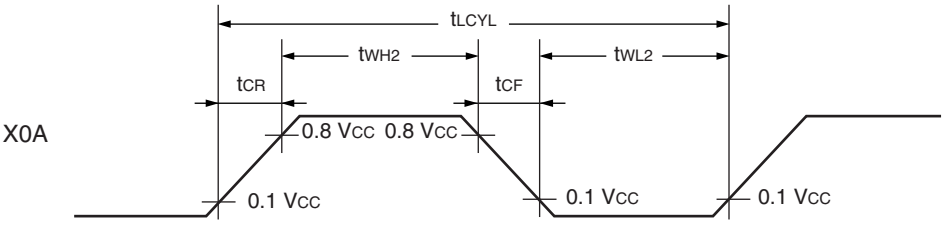
When using a crystal or ceramic oscillator



When using external clock

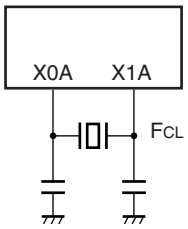


• X0A and X1A Timing and Applying Conditions

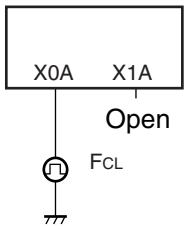


• Subclock Applying Conditions

When using a crystal or ceramic oscillator



When using external clock



(2) Source Clock/Machine Clock

(Vcc = 5.0 V, AVss = Vss = 0.0 V, T_A = − 40 °C to + 85 °C)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Source clock*1 (Clock before setting division)	SCLK	—	100	—	2000	ns	When using Main clock Min : F_{CH} = 10 MHz, PLL multiplied by 1 Max : F_{CH} = 1 MHz, divided by 2
			7.6	—	61.0	µs	When using Subclock Min : F_{CL} = 32 kHz, PLL multiplied by 4 Max : F_{CL} = 32 kHz, divided by 2
Source clock frequency	f_{sp}	—	0.5	—	10.0	MHz	When using Main clock
	f_{spl}	—	16.384	—	131.072	kHz	When using Subclock
Machine clock*2 (Minimum instruction execution time)	MCLK	—	100	—	32000	ns	When using Main clock Min : SLCK = 10 MHz, no division Max : SLCK = 0.5 MHz, divided by 16
			7.6	—	976.5	µs	When using Subclock Min : SLCK = 131 kHz, no division Max : SLCK = 16 kHz, divided by 16
Machine clock frequency	f_{mp}	—	0.031	—	10.000	MHz	When using Main clock
	f_{mpl}		1.024	—	131.072	kHz	When using Subclock

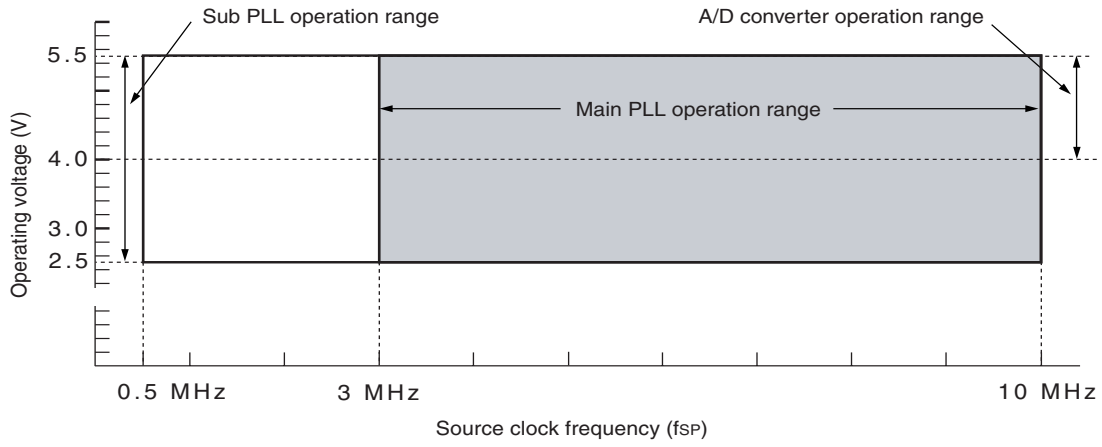
*1 : Clock before setting division due to machine clock division ratio selection bit (SYCC : DIV1 and DIV0) . This source clock is divided by the machine clock division ratio selection bit (SYCC : DIV1 and DIV0) , and it becomes the machine clock. Further, the source clock can be selected as follow.

- Main clock divided by 2
- PLL multiplication of main clock (select from 1, 2, 2.5 multiplication)
- Subclock divided by 2
- PLL multiplication of subclock (select from 2, 3, 4 multiplication)

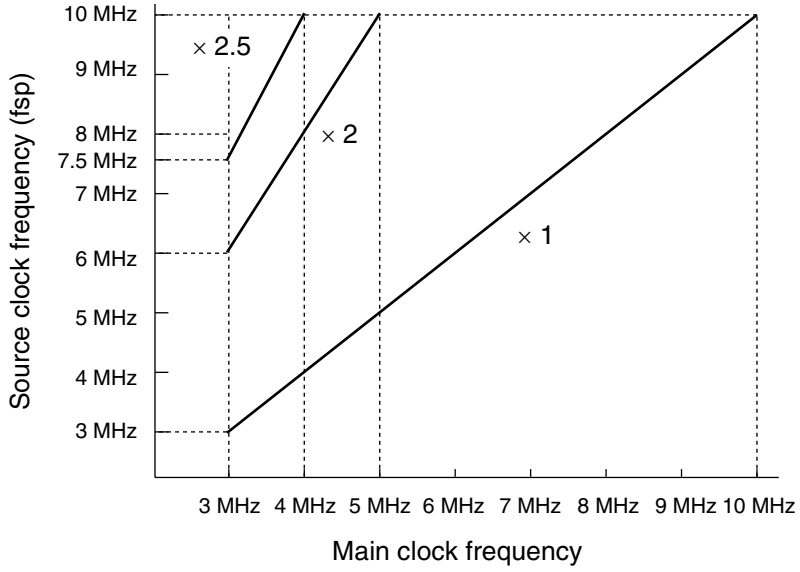
*2 : Operation clock of the microcontroller. Machine clock can be selected as follow.

- Source clock (no division)
- Source clock divided by 4
- Source clock divided by 8
- Source clock divided by 16

• **Operating voltage – Operating frequency**



• **Main PLL operation frequency**



(3) Reset Timing

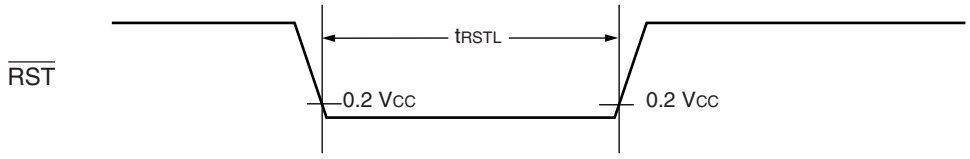
(Vcc = 5.0 V, AVss = Vss = 0.0 V, T_A = − 40 °C to + 85 °C)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
$\overline{RST}$ "L" level pulse width	t_{RSTL}	2 MCLK*1	—	ns	At normal operating
		Oscillation time of oscillator*2 + 100	—	ns	At stop mode, subclock mode, Sub sleep mode, and watch mode
		100	—	µs	At timebase timer mode

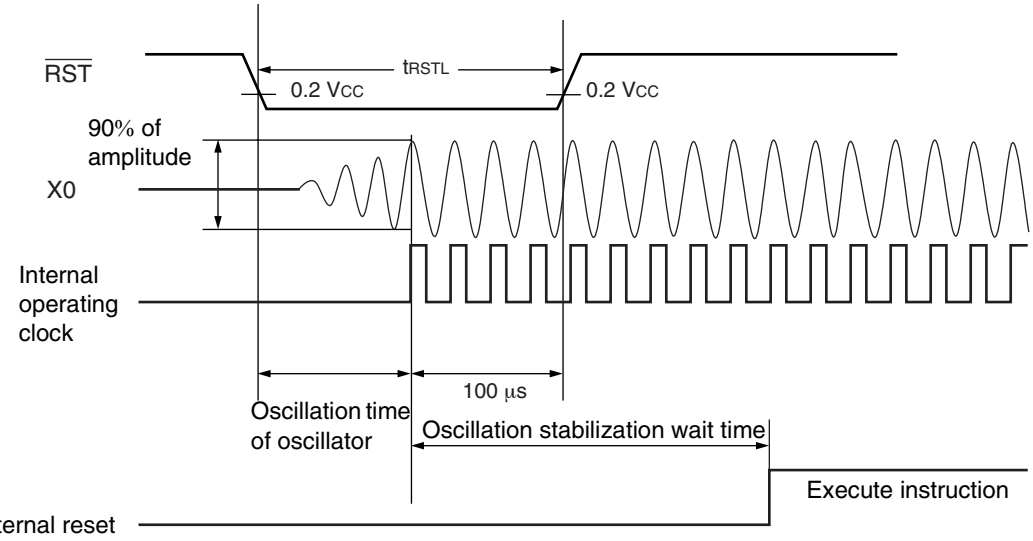
*1 : Refer to " (2) Source Clock/Machine Clock" for MCLK.

*2 : Oscillation time of oscillator is the time that the amplitude reaches 90 %. In the crystal oscillator, the oscillation time is between several ms and tens of ms. In FAR/ceramic oscillators, the oscillation time is between hundreds of µs and several ms. In the external clock, the oscillation time is 0 ms.

• At normal operating



• At stop mode, subclock mode, sub sleep mode, and watch mode

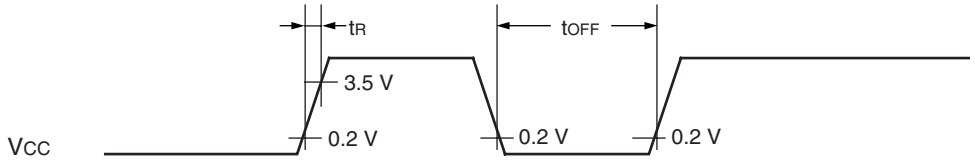


(4) Power-on Reset

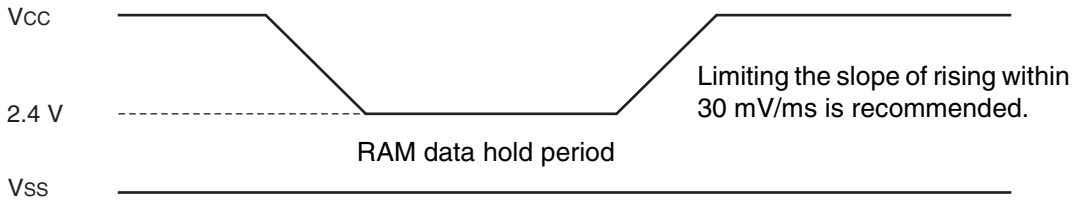
(AVss = Vss = 0.0 V, T_A = − 40 °C to + 85 °C)

Parameter	Symbol	Conditions	Value		Unit	Remarks
			Min	Max		
Power supply rising time	t_R	—	—	36	ms	
Power supply cutoff time	t_{OFF}	—	1	—	ms	Due to repeated operations

Note : The power supply must be turned on within the selected oscillation stabilization time.



Sudden change of power supply voltage may activate the power-on reset function. When changing power supply voltages during operation, set the slope of rising within 20 mV/ms as shown below. In this case, do not use PLL clock. However, if voltage drop is 1V/s or less, use of PLL clock is allowed during operation.

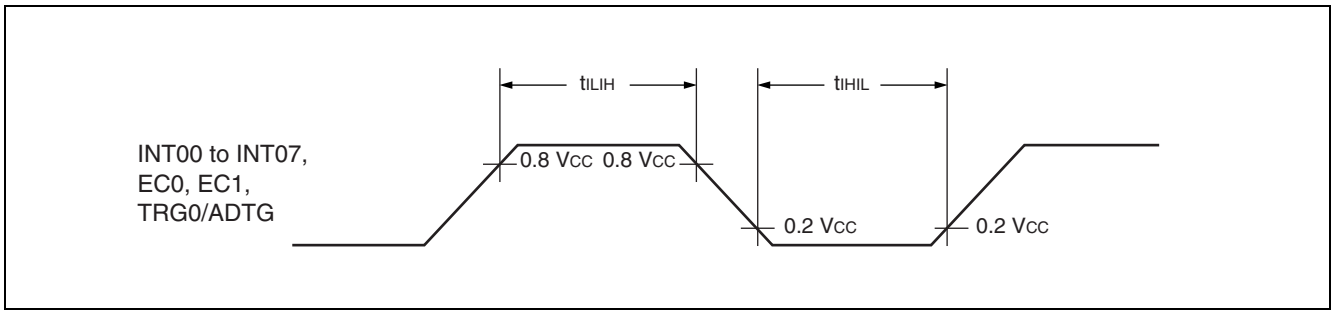


(5) Peripheral Input Timing

(Vcc = 5.0 V, AVss = Vss = 0.0 V, T_A = − 40 °C to + 85 °C)

Parameter	Symbol	Pin name	Value		Unit	Remarks
			Min	Max		
Peripheral input "H" pulse width	t_{ILIH}	INT00 to INT07, EC0, EC1, TRG0/ADTG	2 MCLK*	—	ns	
Peripheral input "L" pulse width	t_{IHIL}		2 MCLK*	—	ns	

* : Refer to "(2) Source Clock/Machine Clock" for MCLK.



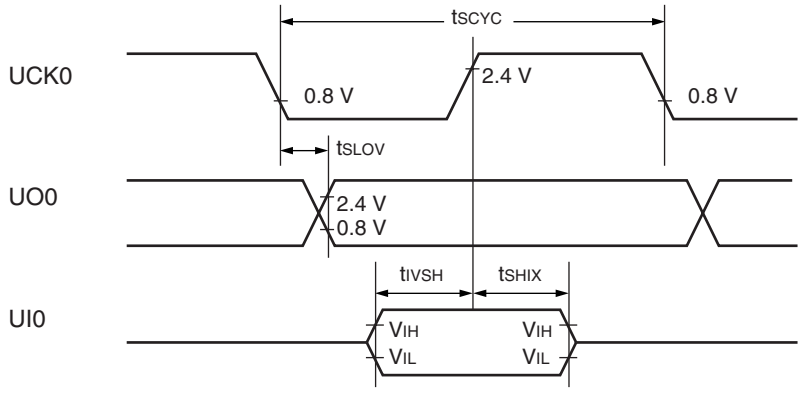
(6) UART/SIO, Serial I/O Timing

(Vcc = 5.0 V, AVss = Vss = 0.0 V, T_A = − 40 °C to + 85 °C)

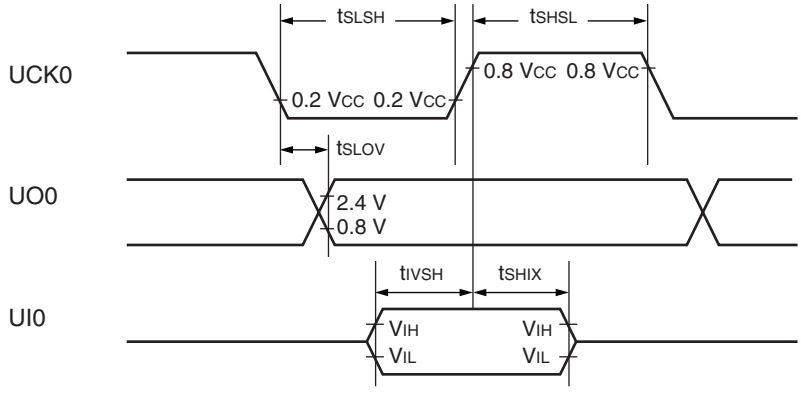
Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	UCK0	Internal clock operation	4 MCLK*	—	ns	
UCK ↓ → UO time	t_{SLOV}	UCK0, UO0		− 190	190	ns	
Valid UI → UCK ↑	t_{IVSH}	UCK0, UI0		2 MCLK*	—	ns	
UCK ↑ → valid UI hold time	t_{SHIX}	UCK0, UI0		2 MCLK*	—	ns	
Serial clock "H" pulse width	t_{SHSL}	UCK0	External clock operation	4 MCLK*	—	ns	
Serial clock "L" pulse width	t_{SLSH}	UCK0		4 MCLK*	—	ns	
UCK ↓ → UO time	t_{SLOV}	UCK0, UO0		—	190	ns	
Valid UI → UCK ↑	t_{IVSH}	UCK0, UI0		2 MCLK*	—	ns	
UCK ↑ → valid UI hold time	t_{SHIX}	UCK0, UI0		2 MCLK*	—	ns	

* : Refer to " (2) Source Clock/Machine Clock" for MCLK.

• Internal shift clock mode



• External shift clock mode



(7) LIN-UART Timing

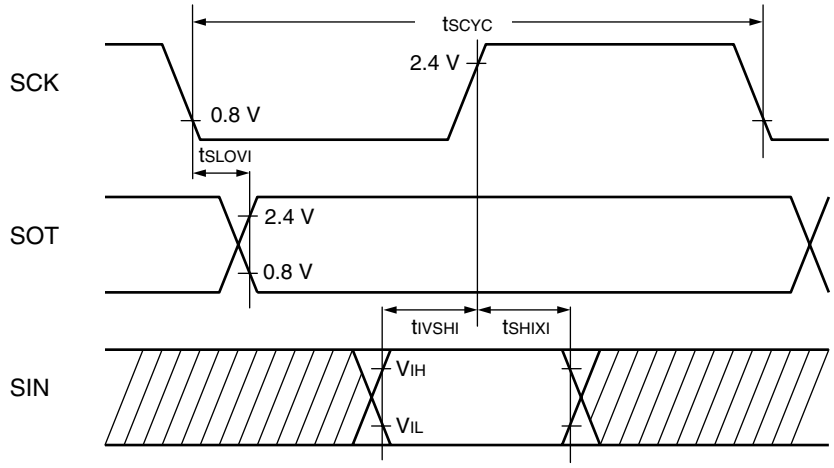
ESCR : SCES = 0, ECCR : SCDE = 0

(Vcc = 5.0 V, AVss = Vss = 0.0 V, T_A = –40 °C to + 85 °C)

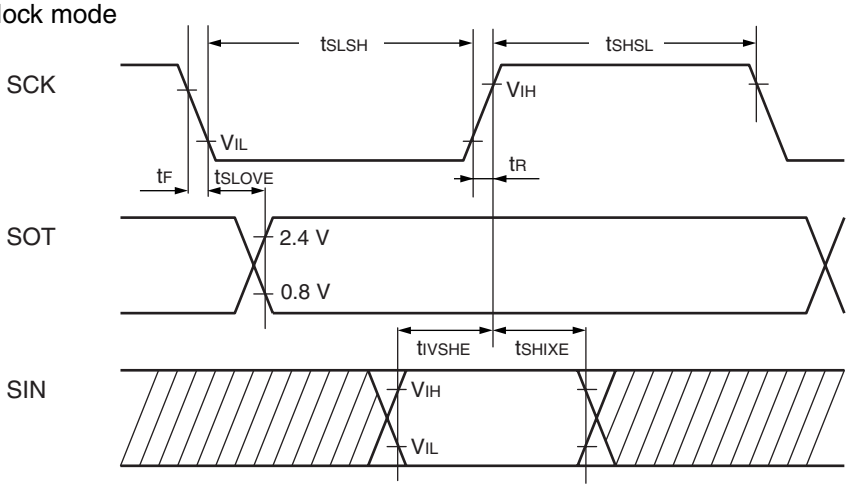
Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK	Internal clock operation output pin : C_L = 80 pF + 1 TTL.	5 MCLK*	—	ns
SCK ↑ → SOT delay time	t_{SLOVI}	SCK, SOT		–95	95	ns
Valid SIN → SCK ↑	t_{IVSHI}	SCK, SIN		MCLK* + 190	—	ns
SCK ↑→ valid SIN hold time	t_{SHIXI}	SCK, SIN		0	—	ns
Serial clock "L" pulse width	t_{SLSH}	SCK	External clock operation output pin : C_L = 80 pF + 1 TTL.	3 MCLK* – t_R	—	ns
Serial clock "H" pulse width	t_{SHSL}	SCK		MCLK* + 95	—	ns
SCK ↓ → SOT delay time	t_{SLOVE}	SCK, SOT		—	2 MCLK* + 95	ns
Valid SIN → SCK↑	t_{IVSHE}	SCK, SIN		190	—	ns
SCK ↑ → Valid SIN hold time	t_{SHIXE}	SCK, SIN		MCLK* + 95	—	ns
SCK fall time	t_F	SCK		—	10	ns
SCK rise time	t_R	SCK		—	10	ns

* : Refer to " (2) Source Clock/Machine Clock" for MCLK.

· Internal shift clock mode



· External shift clock mode



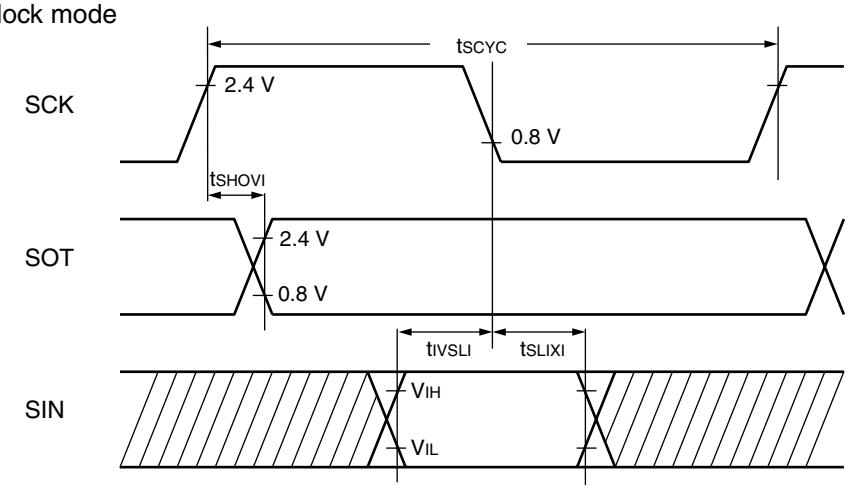
ESCR : SCES = 1, ECCR : SCDE = 0

(Vcc = 5.0 V, AVss = Vss = 0.0 V, T_A = –40 °C to + 85 °C)

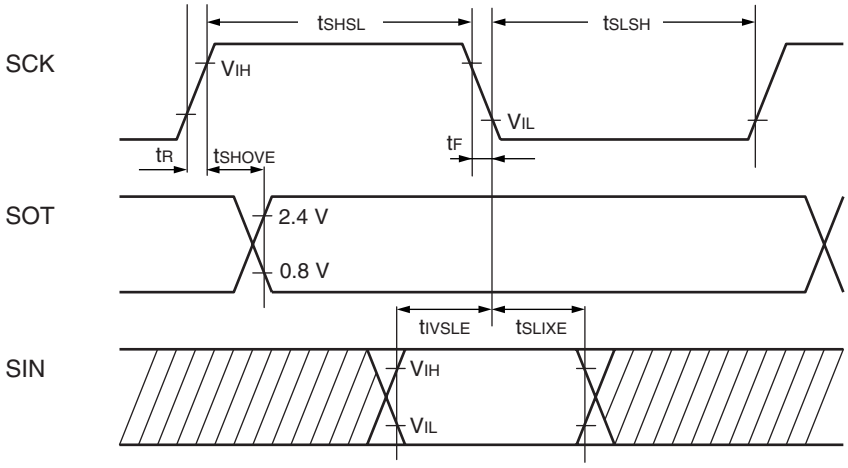
Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK	Internal clock operation output pin : C_L = 80 pF + 1 TTL.	5 MCLK*	—	ns
SCK ↑ → SOT delay time	t_{SHOVI}	SCK, SOT		–95	95	ns
Valid SIN → SCK ↓	t_{IVSLI}	SCK, SIN		MCLK* + 190	—	ns
SCK ↓ → Valid SIN hold time	t_{SLIXI}	SCK, SIN		0	—	ns
Serial clock "H" pulse width	t_{SHSL}	SCK	External clock operation output pin : C_L = 80 pF + 1 TTL.	3 MCLK* – t_R	—	ns
Serial clock "L" pulse width	t_{SLSH}	SCK		MCLK* + 95	—	ns
SCK ↑ → SOT delay time	t_{SHOVE}	SCK, SOT		—	2 MCLK* + 95	ns
Valid SIN → SCK ↓	t_{IVSLE}	SCK, SIN		190	—	ns
SCK ↓ → Valid SIN hold time	t_{SLIXE}	SCK, SIN		MCLK* + 95	—	ns
SCK fall time	t_F	SCK		—	10	ns
SCK rise time	t_R	SCK		—	10	ns

* : Refer to " (2) Source Clock/Machine Clock" for MCLK.

· Internal shift clock mode



· External shift clock mode

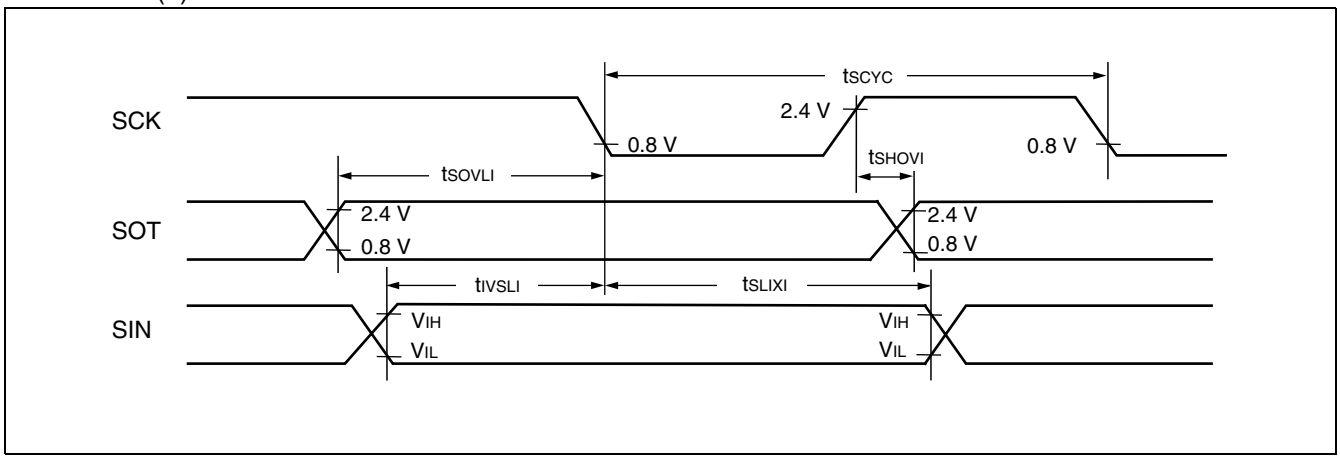


ESCR : SCES = 0, ECCR : SCDE = 1

(Vcc = 5.0 V, AVss = Vss = 0.0 V, T_A = –40 °C to + 85 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK	Internal clock operation output pin : C_L = 80 pF + 1 TTL.	5 MCLK*	—	ns
SCK ↑ → SOT delay time	t_{SHOVI}	SCK, SOT		–95	95	ns
Valid SIN→SCK↓	t_{IVSLI}	SCK, SIN		MCLK* + 190	—	ns
SCK ↓ → valid SIN hold time	t_{SLIXI}	SCK, SIN		0	—	ns
SOT → SCK ↓ delay time	t_{SOVLI}	SCK, SOT		—	4 MCLK*	ns

* : Refer to " (2) Source Clock/Machine Clock" for MCLK.

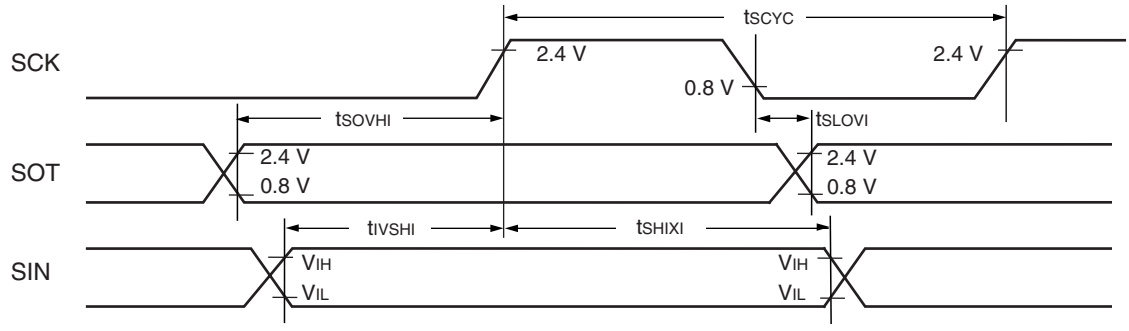


ESCR : SCES = 1, ECCR : SCDE = 1

(Vcc = 5.0 V, AVss = Vss = 0.0 V, T_A = –40 °C to + 85 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK	Internal clock operation output pin : C_L = 80 pF + 1 TTL.	5 MCLK*	—	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCK, SOT		–95	95	ns
Valid SIN → SCK ↑	t_{IVSHI}	SCK, SIN		MCLK* + 190	—	ns
SCK ↑ →valid SIN hold time	t_{SHIXI}	SCK, SIN		0	—	ns
SOT → SCK ↑ delay time	tS_{OVHI}	SCK, SOT		—	4 MCLK*	ns

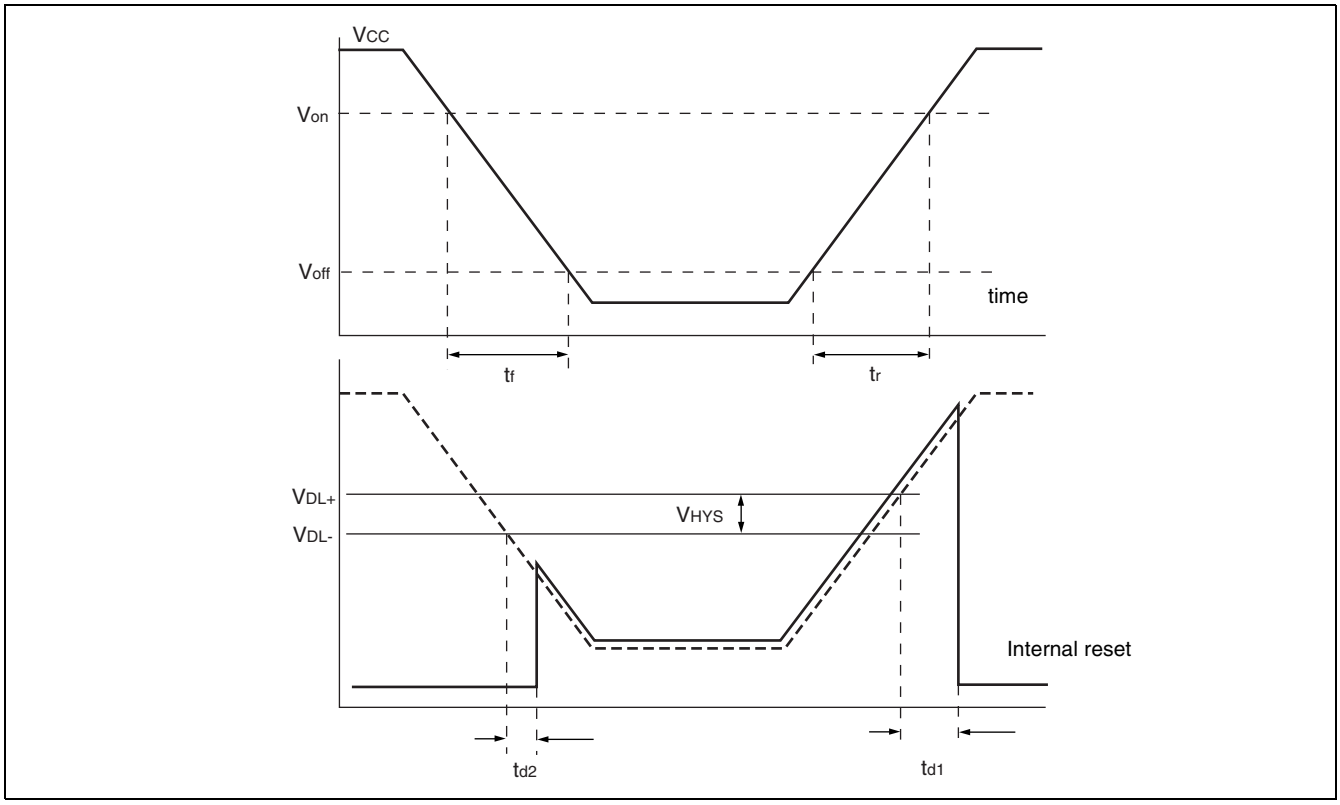
* : Refer to " (2) Source Clock/Machine Clock" for MCLK.



(9) Low Voltage Detection

(AVss = Vss = 0.0 V, T_A = –40 °C to + 85 °C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Release voltage	V_{DL+}	2.47	2.7	2.93	V	At power-supply rise
Detection voltage	V_{DL-}	2.37	2.6	2.83	V	At power-supply fall
Hysteresis width	V_{HYS}	70	100	—	mV	
Power-supply start voltage	V_{off}	—	—	2.3	V	
Power-supply end voltage	V_{on}	4.9	—	—	V	
Power-supply voltage change time (at power supply rise)	t_r	0.3	—	—	µs	Slope of power supply that reset release signal generates
		—	3000	—	µs	Slope of power supply that reset release signal generates within rating (V_{DL+})
Power-supply voltage change time (at power supply fall)	t_f	300	—	—	µs	Slope of power supply that reset detection signal generates
		—	300	—	µs	Slope of power supply that reset detection signal generates within rating (V_{DL-})
Reset release delay time	t_{d1}	—	—	400	µs	
Reset detection delay time	t_{d2}	—	—	30	µs	
Current consumption	—	—	38	50	µA	Current consumption only in low voltage detection circuit



(10) Clock Supervisor Clock

(Vcc = AVcc = 4.5 V to 5.5 V, AVss = Vss = 0.0 V, T_A = –40 °C to + 85 °C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Oscillation frequency	f_{OUT}	50	100	200	kHz	
Oscillation start time	t_{wk}	—	—	10	µs	
Current consumption	—	—	20	36	µs	Current consumption of internal CR oscillator At 100 kHz oscillation

5. A/D Converter

(1) A/D Converter Electrical Characteristics

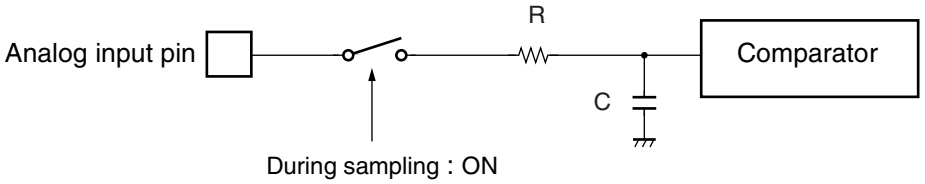
(AVcc = Vcc = 4.0 V to 5.5 V, AVss = Vss = 0.0 V, T_A = − 40 °C to + 85 °C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Resolution	—	—	—	10	bit	
Total error		− 3.0	—	+ 3.0	LSB	
Linearity error		− 2.5	—	+ 2.5	LSB	
Differential linear error		− 1.9	—	+ 1.9	LSB	
Zero transition voltage	V_{OT}	AVss − 1.5 LSB	AVss + 0.5 LSB	AVss + 2.5 LSB	V	
Full-scale transition voltage	V_{FST}	AVcc − 3.5 LSB	AVcc − 1.5 LSB	AVcc + 0.5 LSB	V	
Compare time	—	0.6	—	16,500	µs	4.5 V ≤ AVcc ≤ 4.5 V
		20	—	16,500	µs	4.0 V ≤ AVcc < 4.5 V
Sampling time	—	0.6	—	∞	µs	4.5 V ≤ AVcc ≤ 4.5 V external impedance < at 5.4 kΩ
		1.2	—	∞	µs	4.0 V ≤ AVcc < 4.5 V external impedance < at 2.4 kΩ
Analog input current	I_{AIN}	−0.3	—	0.3	µA	
Analog input voltage range	V_{AIN}	AVss	—	AVcc	V	
Reference voltage	—	AVss + 4.0	—	AVcc	V	AVcc pin
Reference voltage supply current	I_R	—	600	900	µA	AVcc pin, During A/D operation
	I_{RH}	—	—	5	µA	AVcc pin, at stop mode

(2) Notes on Using A/D Converter

- **About the external impedance of analog input and its sampling time**
  - A/D converter with sample and hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the internal sanple and hold capacitor is insufficient, adversely affecting A/D conversion precision.

- Analog input circuit model



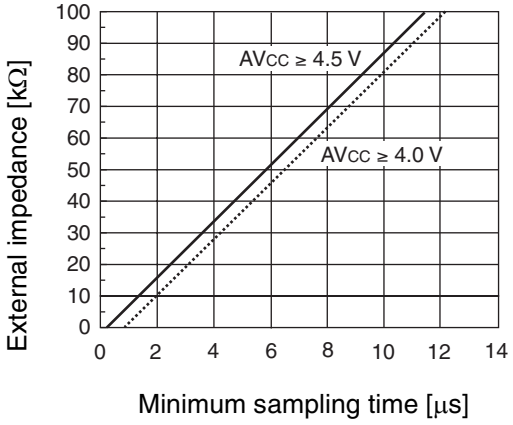
	R	C
4.5 V ≤ AVcc ≤ 5.5 V	2.0 kΩ (Max)	16 pF (Max)
4.0 V ≤ AVcc < 4.5 V	8.2 kΩ (Max)	16 pF (Max)

Note : The values are reference values.

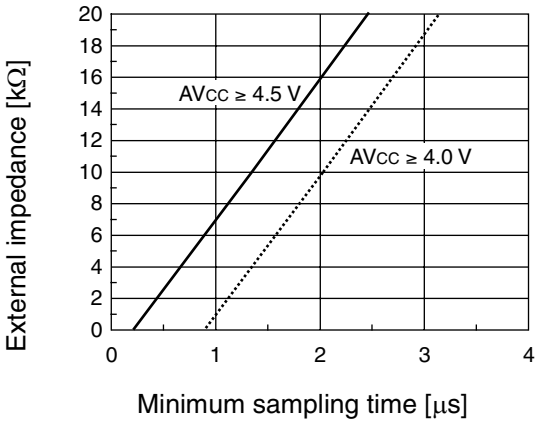
  - To satisfy the A/D conversion precision standard, consider the relationship between the external impedance and minimum sampling time and either adjust the resistor value and operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value.

- The relationship between external impedance and minimum sampling time

(External impedance = 0 kΩ to 100 kΩ)



(External impedance = 0 kΩ to 20 kΩ)



  - If the sampling time cannot be sufficient, connect a capacitor of about 0.1 µF to the analog input pin.

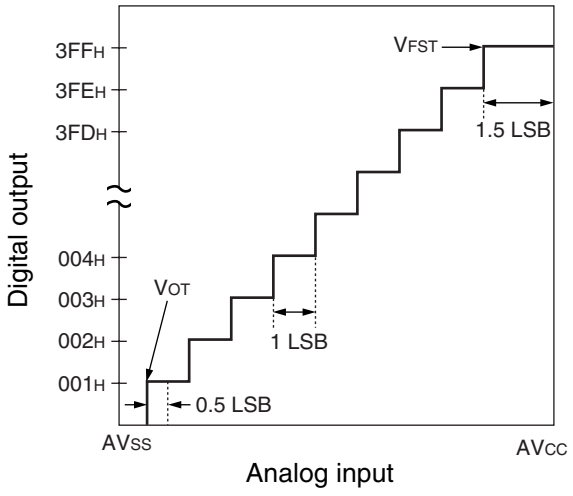
- **About errors**

As |AVCC – AVSS| becomes smaller, values of relative errors grow larger.

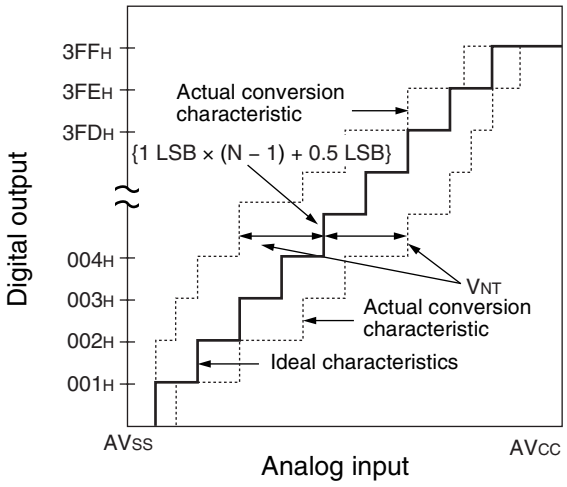
(3) Definition of A/D Converter Terms

- Resolution
  The level of analog variation that can be distinguished by the A/D converter.
  When the number of bits is 10, analog voltage can be divided into $2^{10} = 1024$.
- Linearity error (unit : LSB)
  The deviation between the value along a straight line connecting the zero transition point ("00 0000 0000" ← → "00 0000 0001") of a device and the full-scale transition point ("11 1111 1111" ← → "11 1111 1110") compared with the actual conversion values obtained.
- Differential linear error (Unit : LSB)
  Deviation of input voltage, which is required for changing output code by 1 LSB, from an ideal value.
- Total error (unit: LSB)
  Difference between actual and theoretical values, caused by a zero transition error, full-scale transition error, linearity error, quantum error, and noise.

Ideal I/O characteristics



Total error



$$1\ \text{LSB} = \frac{AV_{CC} - AV_{SS}}{1024}\ (\text{V})$$

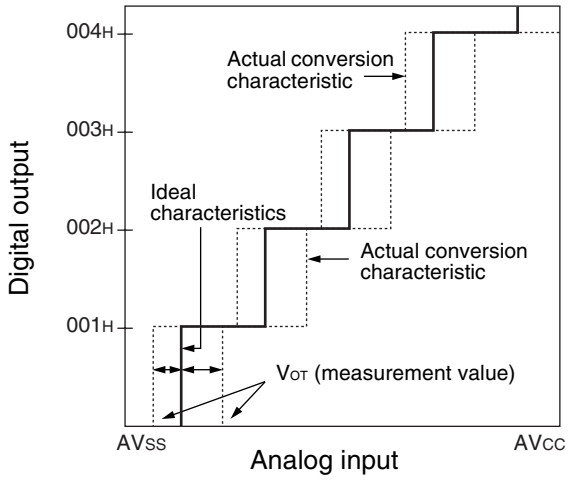
$$\text{Total error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1)\ + 0.5\ \text{LSB}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

V_{NT} : A voltage at which digital output transits from (N – 1) to N.

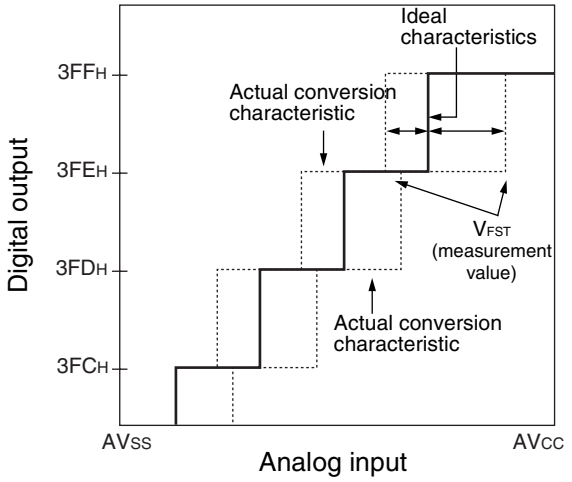
(Continued)

(Continued)

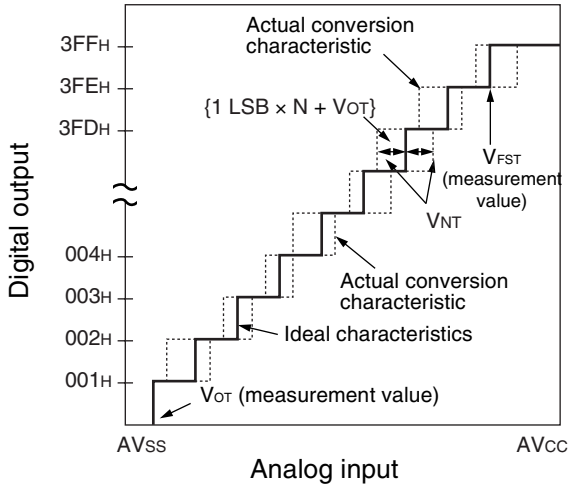
Zero transition error



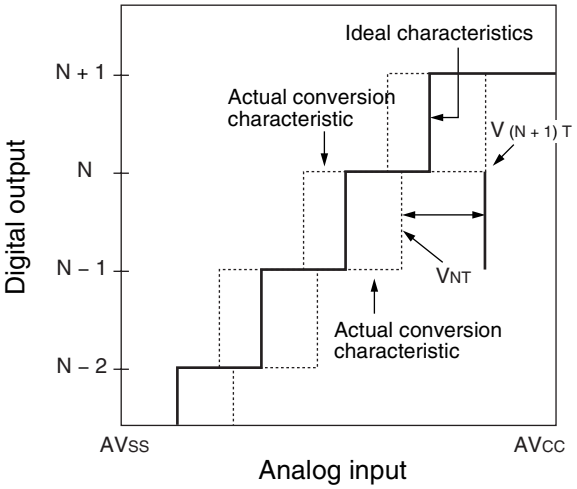
Full-scale transition error



Linearity error



Differential linear error



$$\text{Linear error in digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times N + V_{OT}\}}{1\ \text{LSB}}$$

$$\text{Differential linear error in digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1$$

V_{NT} : A voltage at which digital output transits from (N – 1) to N.
V_{OT} (Ideal value) = AV_{SS} + 0.5 LSB [V]
V_{FST} (Ideal value) = AV_{CC} – 1.5 LSB [V]

6. Flash Memory Program/Erase Characteristics

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Byte programming time	—	32	3600	μs	Excludes system-level overhead
Erase/program cycle	10,000	—	—	cycle	
Power supply voltage at erase/program	4.5	—	5.5	V	
Flash data retention time	20*3	—	—	year	Average T_A = +85 °C

*1 : T_A = + 25 °C, V_{CC} = 5.0 V, 10,000 cycles

*2 : T_A = + 85 °C, V_{CC} = 4.5 V, 10,000 cycles

*3 : This value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at +85 °C) .

■ MASK OPTIONS

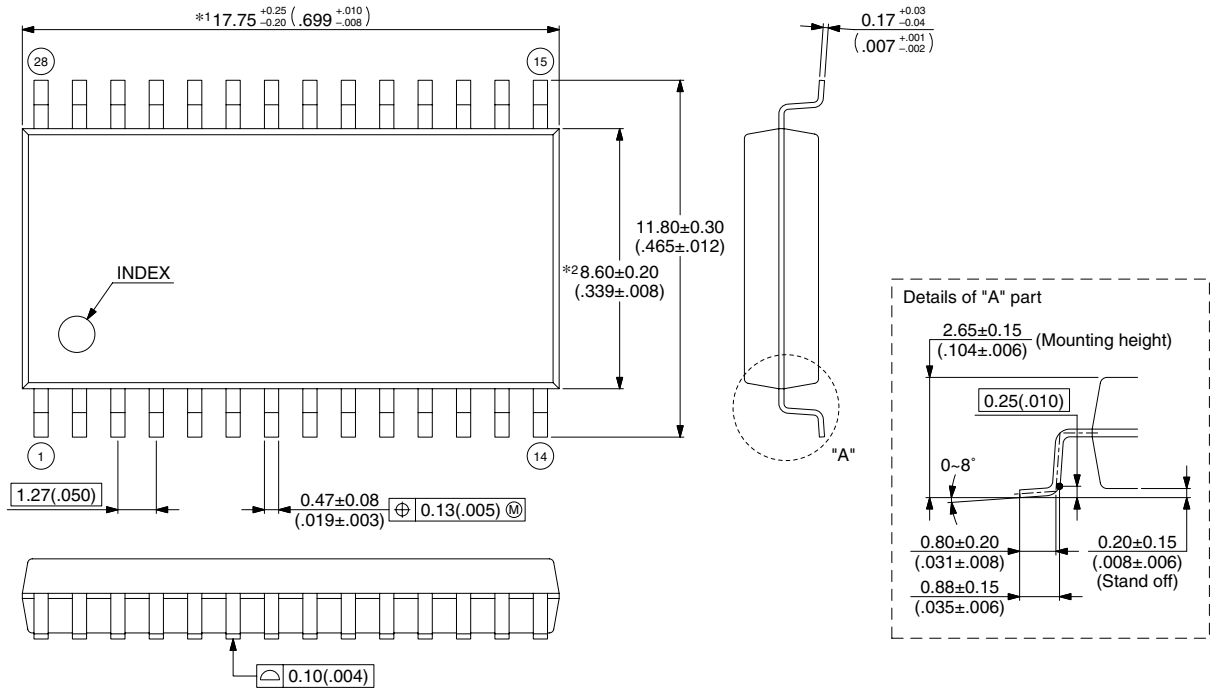
No	Part number	MB95F136HW MB95F136KW MB95F136TW	MB95FV100B-103
	Specifying procedure	Setting disabled	Setting disabled
1	Clock mode select • Single clock mode • Dual clock mode	Dual clock mode	Changing by the switch on MCU board
2	Selection of oscillation stabilization wait time • Selectable the initial value of main clock oscillation stabilization wait time	Fixed to oscillation stabilization wait time of $(2^{14}\text{-}2) / F_{CH}$	Fixed to oscillation stabilization wait time of $(2^{14}\text{-}2) / F_{CH}$
3	Low voltage detection (LVD)	MB95F136HW MB95F136TW	Changing by the switch on MCU board
4	Clock supervisor (CSV)	MB95F136KW	Changing by the switch on MCU board

■ ORDERING INFORMATION

Part number	Package	Remarks
MB95F136HWPF	28-pin plastic SOP (FPT-28P-M17)	
MB2146-303 (MB95FV100B-103PBT)	MCU board 244-pin plastic PFBGA (BGA-244P-M08)	

■ PACKAGE DIMENSIONS

28-pin plastic SOP
(FPT-28P-M17)



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

(Continued)

MEMO

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