

Designer's Data Sheet
Power Field Effect Transistor
N-Channel Enhancement-Mode
Silicon Gate TMOS

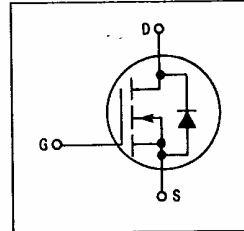
These TMOS Power FETs are designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS} , $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads



MTM3N60
MTP3N55
MTP3N60

TMOS POWER FETs
 3 AMPERES
 $r_{DS(on)} = 2.5$ OHMS
 550 and 600 VOLTS

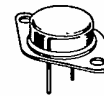


MAXIMUM RATINGS

Rating	Symbol	MTP3N55	MTM3N60 MTP3N60	Unit
		V_{DSS}	550	
Drain-Source Voltage	V_{DGR}	550	600	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \leq 50 \mu s$)	V_{GS}		± 20	Vdc
	V_{GSM}		± 40	Vpk
Drain Current Continuous	I_D		3	Adc
	I_{DM}		10	
Total Power Dissipation @ $T_C = 25^\circ C$ Derate above $25^\circ C$	P_D		75	Watts
			0.6	$W/^\circ C$
Operating and Storage Temperature Range	T_J, T_{stg}	-65 to 150		$^\circ C$

THERMAL CHARACTERISTICS

Thermal Resistance			$^\circ C/W$
Junction to Case	$R_{\theta JC}$	1.67	
Junction to Ambient	$R_{\theta JA}$	30	
		62.5	
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	$^\circ C$



MTM3N60
 CASE 1-06
 TO-204AA



MTP3N55
 MTP3N60
 CASE 221A-04
 TO-220AB

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
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OFF CHARACTERISTICS

Drain-Source Breakdown Voltage (V _{GS} = 0, I _D = 0.25 mA)	V _{(BR)DSS}	550 600	—	Vdc
Zero Gate Voltage Drain Current (V _{DS} = Rated V _{DSS} , V _{GS} = 0) (V _{DS} = 0.8 Rated V _{DSS} , V _{GS} = 0, T _J = 125°C)	I _{DSS}	—	0.2 1	mAdc
Gate-Body Leakage Current, Forward (V _{GSMF} = 20 Vdc, V _{DS} = 0)	I _{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V _{GSR} = 20 Vdc, V _{DS} = 0)	I _{GSSR}	—	100	nAdc

ON CHARACTERISTICS*

Gate Threshold Voltage (V _{DS} = V _{GS} , I _D = 1 mA) T _J = 100°C	V _{GS(th)}	2 1.5	4.5 4	Vdc
Static Drain-Source On-Resistance (V _{GS} = 10 Vdc, I _D = 1.5 Adc)	r _{DS(on)}	—	2.5	Ohms
Drain-Source On-Voltage (V _{GS} = 10 V) (I _D = 3 Adc) (I _D = 1.5 Adc, T _J = 100°C)	V _{DS(on)}	—	9 7.5	Vdc
Forward Transconductance (V _{DS} = 15 V, I _D = 1.5 A)	g _{FS}	1.5	—	mhos

DYNAMIC CHARACTERISTICS

Input Capacitance	V _{DS} = 25 V, V _{GS} = 0, f = 1 MHz See Figure 11	C _{iss}	—	1000	pF
Output Capacitance		C _{oss}	—	300	
Reverse Transfer Capacitance		C _{rss}	—	80	

SWITCHING CHARACTERISTICS* (T_J = 100°C)

Turn-On Delay Time	V _{DD} = 25 V, I _D = 0.5 Rated I _D R _{gen} = 50 ohms See Figures 9, 13 and 14	t _{d(on)}	—	50	ns
Rise Time		t _r	—	100	
Turn-Off Delay Time		t _{d(off)}	—	180	
Fall Time		t _f	—	80	
Total Gate Charge	V _{DS} = 0.8 Rated V _{DSS} , I _D = Rated I _D , V _{GS} = 10 V See Figure 12	Q _g	16 (Typ)	18	nC
Gate-Source Charge		Q _{gs}	8 (Typ)	—	
Gate-Drain Charge		Q _{gd}	8 (Typ)	—	

SOURCE DRAIN DIODE CHARACTERISTICS*

Forward On-Voltage	I _S = Rated I _D V _{GS} = 0	V _{SD}	1.1 (Typ)	—	Vdc
Forward Turn-On Time		t _{on}	Limited by stray inductance		
Reverse Recovery Time		t _{rr}	165 (Typ)	—	ns

INTERNAL PACKAGE INDUCTANCE (TO-204)

Internal Drain Inductance (Measured from the contact screw on the header closer to the source pin and the center of the die)	L _d	6 (Typ)	—	nH
Internal Source Inductance (Measured from the source pin, 0.25" from the package to the source bond pad)	L _s	12.5 (Typ)	—	nH

INTERNAL PACKAGE INDUCTANCE (TO-220)

Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25" from package to center of die)	L _d	3.5 (Typ) 4.5 (Typ)	—	nH
Internal Source Inductance (Measured from the source lead 0.25" from package to source bond pad.)	L _s	7.5 (Typ)	—	nH

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.



TYPICAL ELECTRICAL CHARACTERISTICS

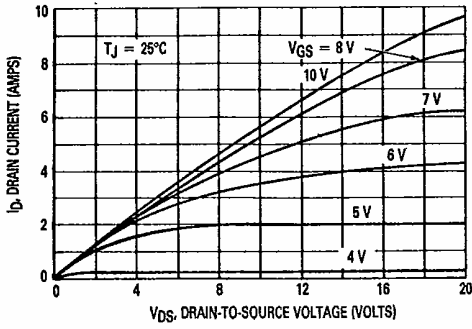


Figure 1. On-Region Characteristics

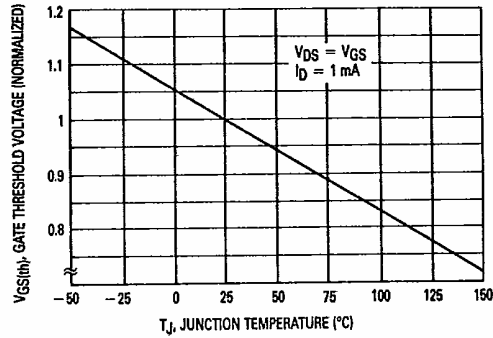


Figure 2. Gate-Threshold Voltage Variation With Temperature

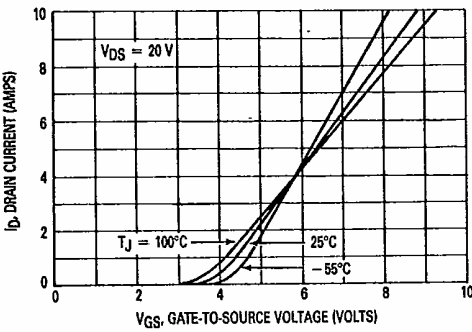


Figure 3. Transfer Characteristics

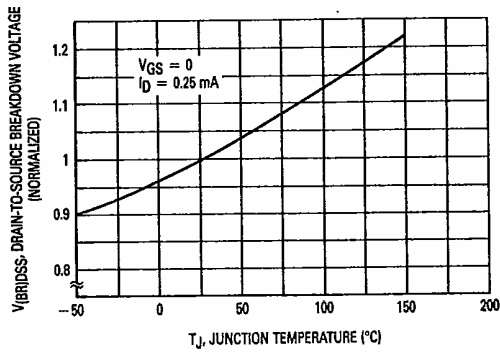


Figure 4. Breakdown Voltage Variation With Temperature

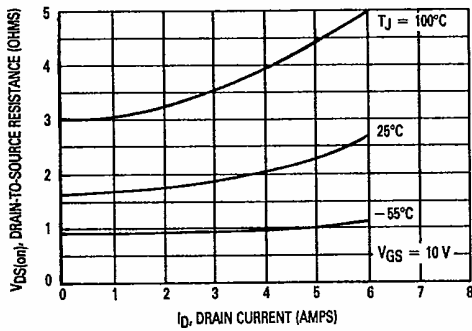


Figure 5. On-Resistance versus Drain Current

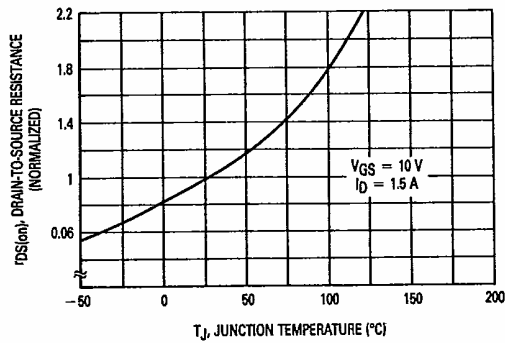


Figure 6. On-Resistance Variation With Temperature

SAFE OPERATING AREA INFORMATION

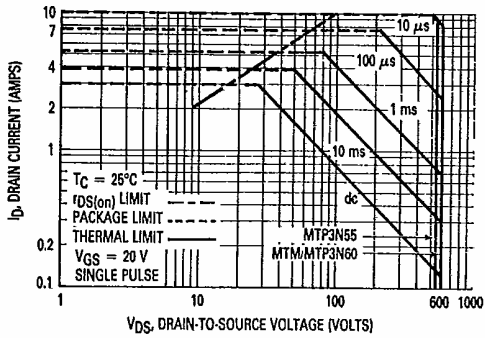


Figure 7. Maximum Rated Forward Biased Safe Operating Area

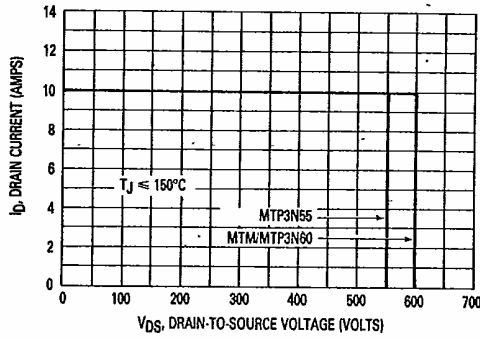


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_J(\max) - T_C}{R_{\theta JC}}$$

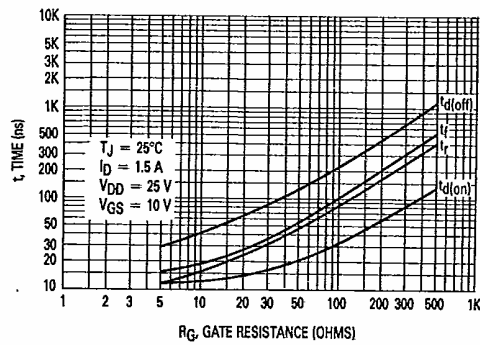


Figure 9. Resistive Switching Time Variation versus Gate Resistance

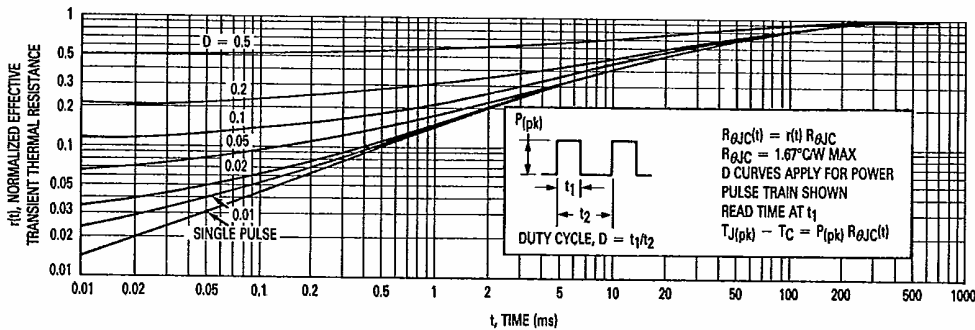


Figure 10. Thermal Response

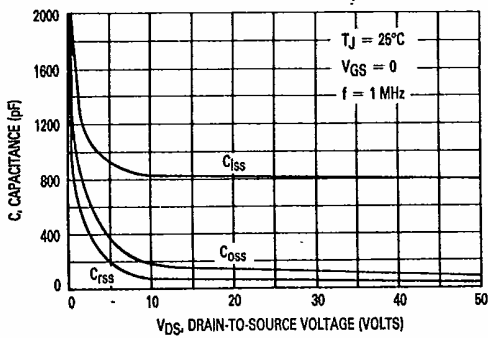


Figure 11. Capacitance Variation

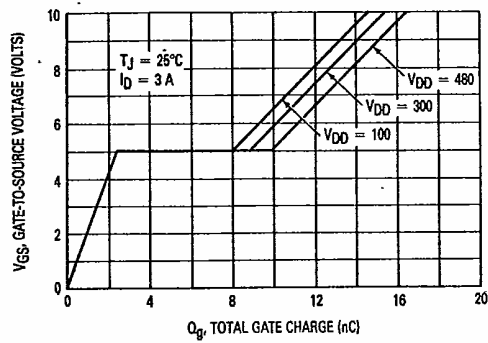


Figure 12. Gate Charge versus Gate-to-Source Voltage

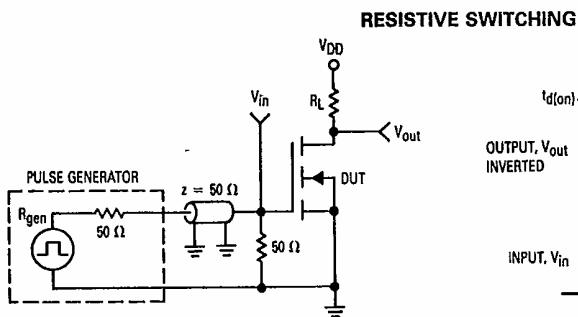


Figure 13. Switching Test Circuit

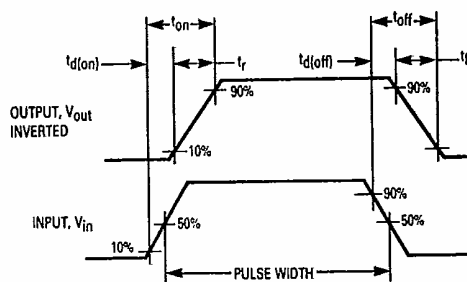


Figure 14. Switching Waveforms

OUTLINE DIMENSIONS

**CASE 1-06
TO-204AA**

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	8.25	0.250	0.325
D	0.97	1.09	0.038	0.043
E	1.40	1.77	0.055	0.070
F	30.15 BSC	—	1.187 BSC	—
G	19.92 BSC	—	0.783 BSC	—
H	5.48 BSC	—	0.215 BSC	—
J	16.83 BSC	—	0.665 BSC	—
K	11.18	12.19	0.440	0.480
Q	3.84	4.19	0.151	0.165
R	—	28.57	—	1.125
U	4.83	5.33	0.190	0.210
V	3.84	4.19	0.151	0.165

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.3M, 1987.
2. CONTROLLING DIMENSION INCH.
3. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO 204AA OUTLINE SHALL APPLY.

STYLE 3:
PIN 1. GATE
2. SOURCE
CASE DRAIN

**CASE 221A-04
TO-220AB**

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.48	15.25	0.570	0.600
B	6.08	10.74	0.240	0.425
C	4.07	4.82	0.160	0.190
D	6.64	6.86	0.261	0.270
F	3.81	3.73	0.150	0.147
G	2.42	2.86	0.095	0.113
H	3.80	3.83	0.150	0.151
J	6.38	6.55	0.251	0.258
K	12.28	14.27	0.520	0.562
L	1.15	1.28	0.045	0.051
M	4.83	5.33	0.190	0.210
Q	2.54	3.54	0.100	0.139
R	2.54	3.78	0.100	0.149
S	1.15	1.28	0.045	0.051
T	3.81	4.47	0.150	0.176
U	6.08	6.77	0.240	0.267
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.3M, 1987.
2. CONTROLLING DIMENSION INCH.
3. DIM Z DEFINES A DIMENSION WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN