

Designer's Data Sheet

Power Field Effect Transistor

N-Channel Enhancement-Mode

Silicon Gate TMOS

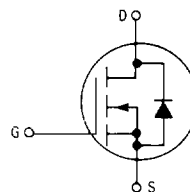
These TMOS Power FETs are designed for high voltage, high speed power switching applications such as switching regulators, converters, high voltage power supplies and grid drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS} , $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads



MTM3N75
MTM3N80
MTP3N75
MTP3N80

TMOS POWER FETs
3 AMPERES
 $r_{DS(on)} = 7 \text{ OHMS}$
750 and 800 VOLTS

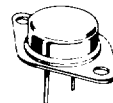


MAXIMUM RATINGS

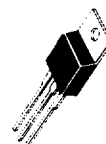
Rating	Symbol	MTM3N75	MTM3N80	Unit
		MTP3N75	MTP3N80	
Drain-Source Voltage	V_{DSS}	750	800	Vdc
Drain-Gate Voltage ($R_{GS} = 1 \text{ M}\Omega$)	V_{DGR}	750	800	Vdc
Gate-Source Voltage — Continuous	V_{GS}	± 20		Vdc
— Non-repetitive ($t_p \leq 50 \mu s$)	V_{GSM}	± 40		Vpk
Drain Current — Continuous	I_D	3		Adc
— Pulsed	I_{DM}	8		
Total Power Dissipation in $T_C = 25^\circ\text{C}$	P_D	75		Watts
Derate above 25°C		0.6		W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	-65 to 150		°C

THERMAL CHARACTERISTICS

Thermal Resistance		$R_{\theta JC}$	1.67	°C/W
Junction to Case				
Junction to Ambient				
	TO-204	$R_{\theta JA}$	30	
	TO-220		62.5	
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	T_L		275	°C



MTM3N75
MTM3N80
CASE 1-06
TO-204AA



MTP3N75
MTP3N80
CASE 221A-04
TO-220AB

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

MTM/MTP3N75, 80

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
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OFF CHARACTERISTICS

Drain-Source Breakdown Voltage (V _{GS} = 0, I _D = 0.25 mA)	MTM:MTP3N75 MTM:MTP3N80	V _{(BR)DSS}	750 800	— —	V _{dc}
Zero Gate Voltage Drain Current (V _{DS} = Rated V _{DSS} , V _{GS} = 0) (V _{DS} = 0.8 Rated V _{DSS} , V _{GS} = 0, T _J = 125°C)		I _{DSS}	— —	0.2 1	mAdc
Gate-Body Leakage Current, Forward (V _{GSF} = 20 V _{dc} , V _{DS} = 0)		I _{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V _{GSR} = 20 V _{dc} , V _{DS} = 0)		I _{GSSR}	—	100	nAdc

ON CHARACTERISTICS*

Gate Threshold Voltage (V _{DS} = V _{GS} , I _D = 1 mA) T _J = 100°C		V _{GS(th)}	2 1.5	4.5 4	V _{dc}
Static Drain-Source On-Resistance (V _{GS} = 10 V _{dc} , I _D = 1.5 Adc)		r _{DS(on)}	—	7	Ohms
Drain-Source On-Voltage (V _{GS} = 10 V) (I _D = 3 Adc) (I _D = 1.5 Adc, T _J = 100°C)		V _{DS(on)}	— —	21 21	V _{dc}
Forward Transconductance (V _{DS} = 15 V, I _D = 1.5 A)		g _{FS}	0.5	—	mhos

DYNAMIC CHARACTERISTICS

Input Capacitance	(V _{DS} = 25 V, V _{GS} = 0, f = 1 MHz) See Figure 11	C _{iss}	—	1200	pF
Output Capacitance		C _{oss}	—	300	
Reverse Transfer Capacitance		C _{rss}	—	80	

SWITCHING CHARACTERISTICS* (T_J = 100°C)

Turn-On Delay Time	(V _{DD} = 125 V, I _D = 0.5 Rated I _D R _{gen} = 50 ohms) See Figures 9, 13 and 14	t _{d(on)}	—	50	ns
Rise Time		t _r	—	150	
Turn-Off Delay Time		t _{d(off)}	—	200	
Fall Time		t _f	—	100	
Total Gate Charge	(V _{DS} = 0.8 Rated V _{DSS} , I _D = Rated I _D , V _{GS} = 10 V) See Figure 12	Q _g	35 (Typ)	50	nC
Gate-Source Charge		Q _{gs}	20 (Typ)	—	
Gate-Drain Charge		Q _{gd}	15 (Typ)	—	

SOURCE DRAIN DIODE CHARACTERISTICS*

Forward On-Voltage	(I _S = Rated I _D V _{GS} = 0)	V _{SD}	1 (Typ)	1.6	V _{dc}
Forward Turn-On Time		t _{on}	Limited by stray inductance		
Reverse Recovery Time		t _{rr}	420 (Typ)	—	ns

INTERNAL PACKAGE INDUCTANCE (TO-204)

Internal Drain Inductance (Measured from the contact screw on the header closer to the source pin and the center of the die)	L _d	5 (Typ)	—	nH
Internal Source Inductance (Measured from the source pin, 0.25" from the package to the source bond pad)	L _s	12.5 (Typ)	—	

INTERNAL PACKAGE INDUCTANCE (TO-220)

Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25" from package to center of die)	L _d	3.5 (Typ) 4.5 (Typ)	— —	nH
Internal Source Inductance (Measured from the source lead 0.25" from package to source bond pad.)	L _s	7.5 (Typ)	—	

*Pulse Test: Pulse Width ≤ 300 μs. Duty Cycle ≤ 2%.

TYPICAL ELECTRICAL CHARACTERISTICS

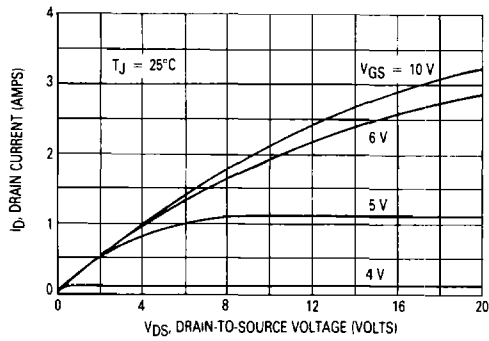


Figure 1. On-Region Characteristics

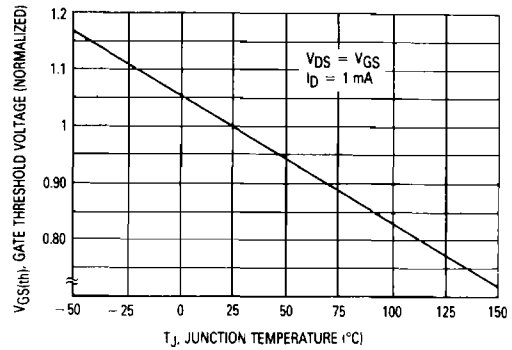


Figure 2. Gate-Threshold Voltage Variation With Temperature

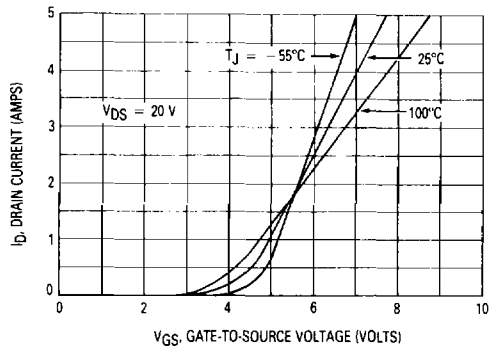


Figure 3. Transfer Characteristics

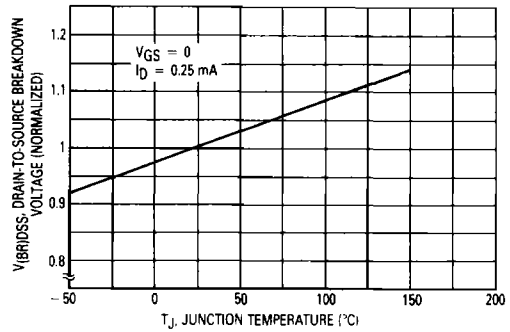


Figure 4. Breakdown Voltage Variation With Temperature

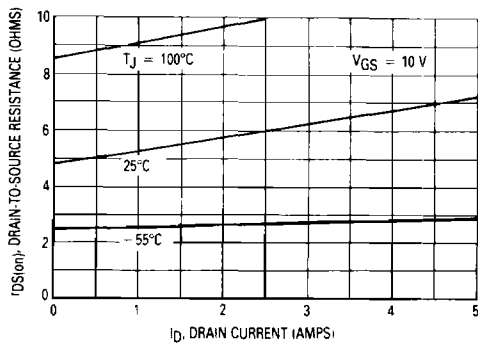


Figure 5. On-Resistance versus Drain Current

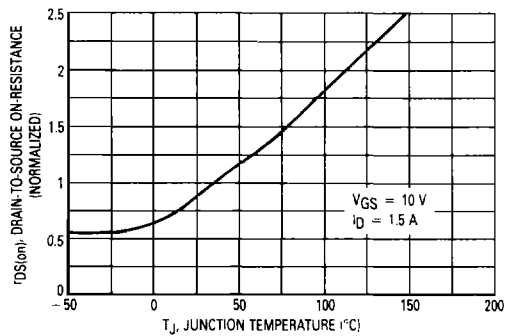


Figure 6. On-Resistance Variation With Temperature

SAFE OPERATING AREA INFORMATION

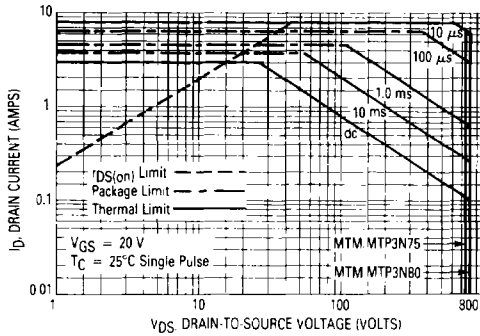


Figure 7. Maximum Rated Forward Biased Safe Operating Area

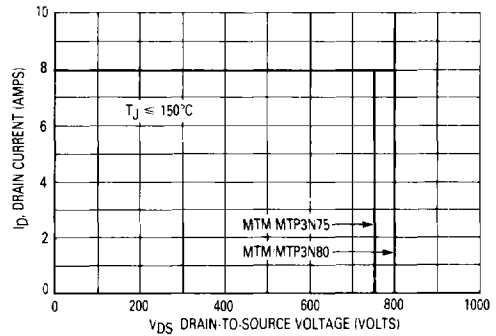


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

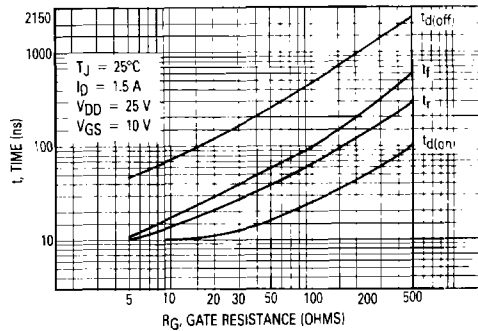


Figure 9. Resistive Switching Time Variation versus Gate Resistance

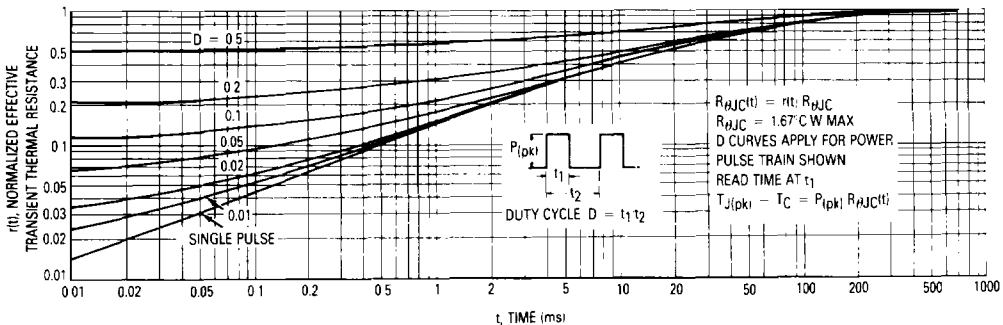


Figure 10. Thermal Response

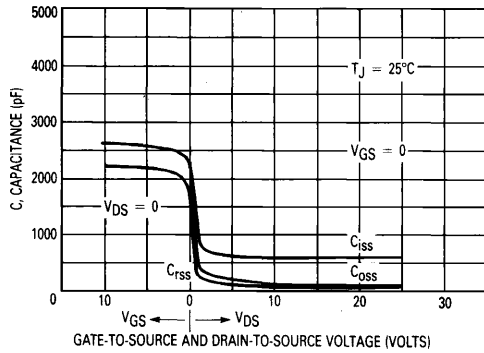


Figure 11. Capacitance Variation

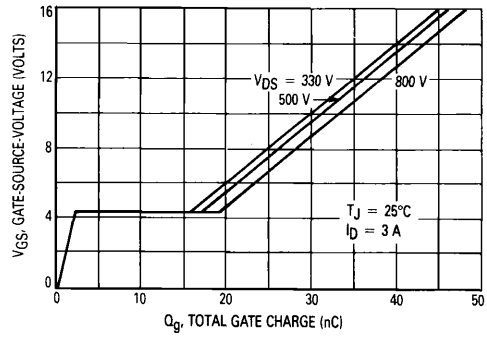


Figure 12. Gate Charge versus Gate-to-Source Voltage

RESISTIVE SWITCHING

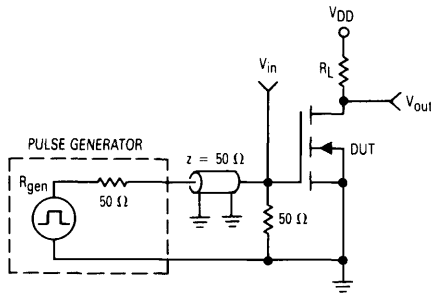


Figure 13. Switching Test Circuit

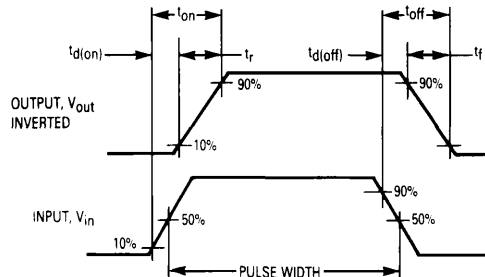


Figure 14. Switching Waveforms

OUTLINE DIMENSIONS

