

Designer's Data Sheet

Power Field Effect Transistor

P-Channel Enhancement-Mode

Silicon Gate TMOS

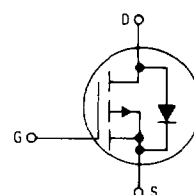
These TMOS Power FETs are designed for medium voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS} , $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads



MTM5P18
MTM5P20
MTP5P18
MTP5P20

TMOS POWER FETs
5 AMPERES
 $r_{DS(on)} = 1 \text{ OHM}$
180 and 200 VOLTS

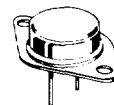


MAXIMUM RATINGS

Rating	Symbol	MTM or MTP		Unit
		5P18	5P20	
Drain-Source Voltage	V_{DSS}	180	200	Vdc
Drain-Gate Voltage ($R_{GS} = 1 \text{ M}\Omega$)	V_{DGR}	180	200	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \leq 50 \mu s$)	V_{GS}	± 20		Vdc
	V_{GSM}	± 40		Vpk
Drain Current Continuous Pulsed	I_D	5		Adc
	I_{DM}	20		
Total Power Dissipation @ $T_C = 25^\circ C$ Derate above $25^\circ C$	P_D	75	0.6	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	-65 to 150		°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case Junction to Ambient	$R_{\theta JC}$	1.67	°C/W
		30	
	$R_{\theta JA}$	62.5	
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	°C



MTM5P18
MTM5P20
CASE 1-04
TO-204AA



MTP5P18
MTP5P20
CASE 221A-04
TO-220AB

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
----------------	--------	-----	-----	------

OFF CHARACTERISTICS

Drain-Source Breakdown Voltage ($V_{GS} = 0$, $I_D = 0.25\text{ mA}$)	MTM/MTP5P18 MTM/MTP5P20	$V_{(BR)DSS}$	180 200	— —	Vdc
Zero Gate Voltage Drain Current ($V_{DS} = \text{Rated } V_{DSS}$, $V_{GS} = 0$) ($V_{DS} = \text{Rated } V_{DSS}$, $V_{GS} = 0$, $T_J = 125^\circ\text{C}$)		I_{DSS}	— —	10 100	μAdc
Gate-Body Leakage Current, Forward ($V_{GSF} = 20\text{ Vdc}$, $V_{DS} = 0$)		I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse ($V_{GSR} = 20\text{ Vdc}$, $V_{DS} = 0$)		I_{GSSR}	—	100	nAdc

ON CHARACTERISTICS*

Gate Threshold Voltage ($V_{DS} = V_{GS}$, $I_D = 1\text{ mA}$) $T_J = 100^\circ\text{C}$		$V_{GS(th)}$	2 1.5	4.5 4	Vdc
Static Drain-Source On-Resistance ($V_{GS} = 10\text{ Vdc}$, $I_D = 2.5\text{ Adc}$)		$r_{DS(on)}$	—	1	Ohm
Drain-Source On-Voltage ($V_{GS} = 10\text{ V}$) ($I_D = 5\text{ Adc}$) ($I_D = 2.5\text{ Adc}$, $T_J = 100^\circ\text{C}$)		$V_{DS(on)}$	— —	5 4	Vdc
Forward Transconductance ($V_{DS} = 15\text{ V}$, $I_D = 2.5\text{ A}$)		g_{FS}	2	—	mhos

DYNAMIC CHARACTERISTICS

Input Capacitance	($V_{DS} = 25\text{ V}$, $V_{GS} = 0$, $f = 1\text{ MHz}$) See Figure 10	C_{iss}	—	1000	pF
Output Capacitance		C_{oss}	—	250	
Reverse Transfer Capacitance		C_{rss}	—	75	

SWITCHING CHARACTERISTICS* ($T_J = 100^\circ\text{C}$)

Turn-On Delay Time	($V_{DD} = 25\text{ V}$, $I_D = 0.5\text{ Rated } I_D$ $R_{gen} = 50\text{ ohms}$) See Figures 11 and 12	$t_{d(on)}$	—	40	ns
Rise Time		t_r	—	50	
Turn-Off Delay Time		$t_{d(off)}$	—	90	
Fall Time		t_f	—	60	

SOURCE DRAIN DIODE CHARACTERISTICS*

Forward On-Voltage	($I_S = \text{Rated } I_D$ $V_{GS} = 0$)	V_{SD}	2 (Typ)	4	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	(Typ)	—	ns

INTERNAL PACKAGE INDUCTANCE (TO-204)

Internal Drain Inductance (Measured from the contact screw on the header closer to the source pin and the center of the die)	L_d	5 (Typ)	—	nH
Internal Source Inductance (Measured from the source pin, 0.25" from the package to the source bond pad)	L_s	12.5 (Typ)	—	

INTERNAL PACKAGE INDUCTANCE (TO-220)

Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25" from package to center of die)	L_d	3.5 (Typ) 4.5 (Typ)	— —	nH
Internal Source Inductance (Measured from the source lead 0.25" from package to source bond pad.)	L_s	7.5 (Typ)	—	

*Pulse Test: Pulse Width $\leq 300\text{ }\mu\text{s}$, Duty Cycle $\leq 2\%$.

TYPICAL ELECTRICAL CHARACTERISTICS

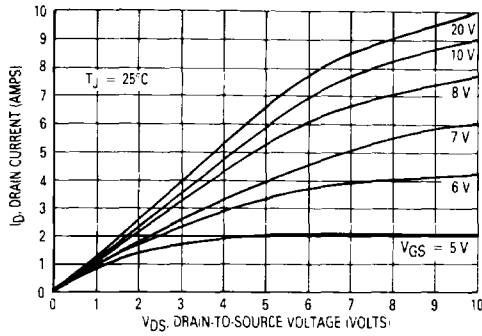


Figure 1. On-Region Characteristics

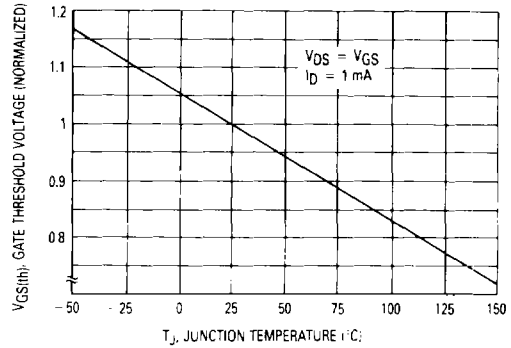


Figure 2. Gate-Threshold Voltage Variation With Temperature

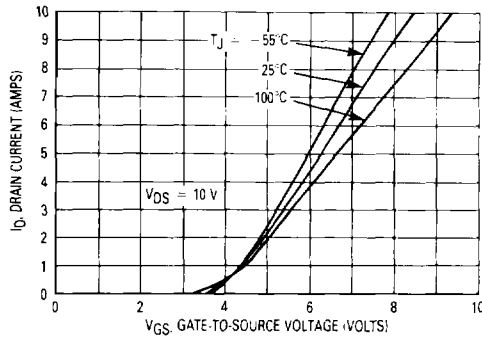


Figure 3. Transfer Characteristics

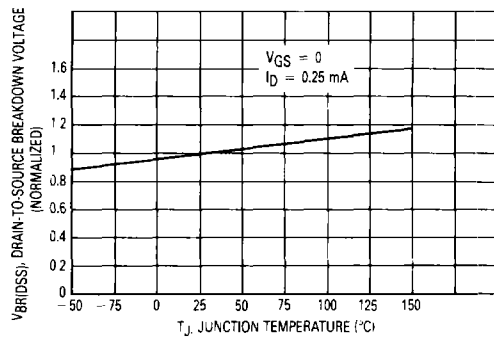


Figure 4. Normalized Breakdown Voltage versus Temperature

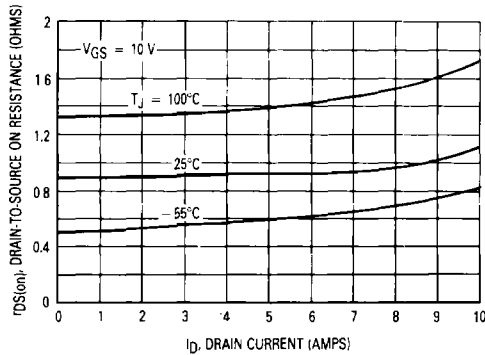


Figure 5. On-Resistance versus Drain Current

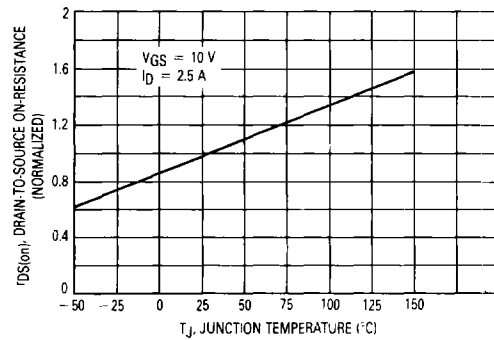


Figure 6. On-Resistance Variation With Temperature

SAFE OPERATING AREA INFORMATION

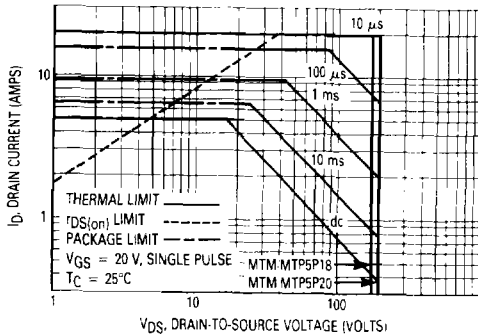


Figure 7. Maximum Rated Forward Biased Safe Operating Area

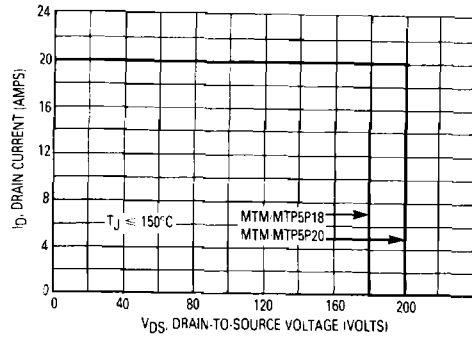


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The dc data of Figure 7 is based on a case temperature (T_C) of 25°C and a maximum junction temperature ($T_{J(max)}$) of 150°. The actual junction temperature depends on the power dissipated in the device and its case temperature. For various pulse widths, duty cycles, and case temperatures, the peak allowable drain current (I_{DM}) may be calculated with the aid of the following equation:

$$I_{DM} = I_D(25^\circ\text{C}) \left[\frac{T_{J(max)} - T_C}{P_D \cdot R_{\theta JC} \cdot r(t)} \right]$$

where

$I_D(25^\circ\text{C})$ = the dc drain current at $T_C = 25^\circ\text{C}$ from Figure 6.

$T_{J(max)}$ = rated maximum junction temperature.

T_C = device case temperature.

P_D = rated power dissipation at $T_C = 25^\circ\text{C}$.

$R_{\theta JC}$ = rated steady state thermal resistance.
 $r(t)$ = normalized thermal response from Figure 9.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 7 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

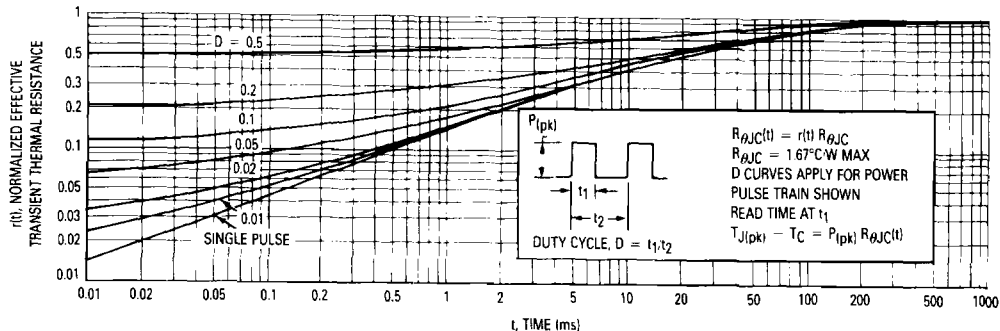


Figure 9. Thermal Response

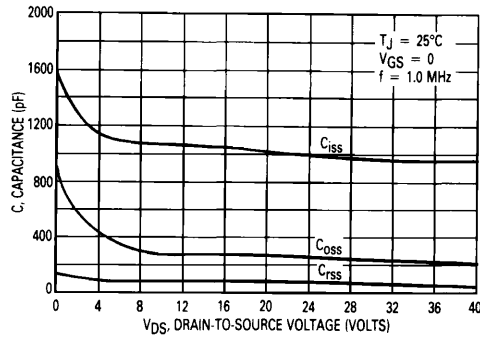


Figure 10. Capacitance Variation

RESISTIVE SWITCHING

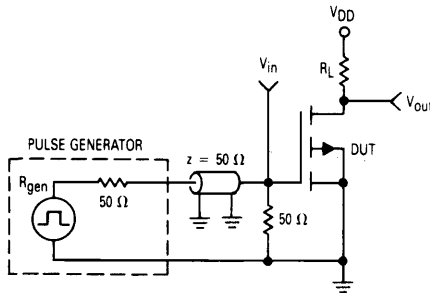


Figure 11. Switching Test Circuit

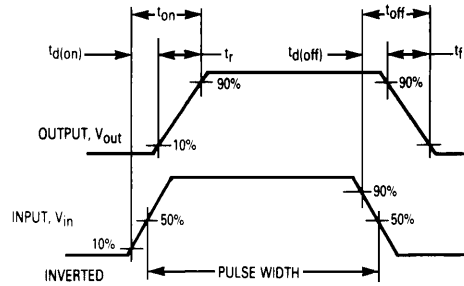


Figure 12. Switching Waveforms

OUTLINE DIMENSIONS

